Issues Inherent in the Design of a CISC Processor

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Microprocessor design as it is traditionally taught uses RISC (reduced instruction set computer) architectures to illustrate the principles behind chip design. While such chips are useful tools for instruction, they are absent from nearly all mainstream computers; CISC (complex instruction set computer) architectures such as those in the Pentium family of processors dominate the market. This project will examine some of the issues not present in the design of RISC processors but which are present in CISC processors. The most important such issue which will be examined will be the implementation of instructions which perform multiple RISC-like operations per instruction (such as looping instructions or instructions such as the x86 `enter` and `leave` which modify multiple registers). Other possible issues for examination include variable-length instructions, complex arithmetic operations, the pipelining necessary in all implementations of CISC to support reading and modifying multiple registers or memory locations simultaneously, and CISC-to-RISC instruction translation as used in all modern x86 processors to efficiently implement the x86 instruction set.