Final Project

- Schedule, Organization
- Choosing a topic
- Example projects
- Grading
- Design Suggestions

Final Project: Schedule

- Choose project teams (email gim ASAP)
  - Teams of two or three. A single person project requires approval of lecturer.
- Project Abstract (due Fri Oct 21, submit on-line)
  - Start discussing ideas now with 6.111 staff
  - About 1 page long, a list of team members, and a one paragraph description of the project itself.
- Proposal Conference with staff mentor (by Fri, Oct 28)
  - Bring your proposal with you *and* submit on-line
- Block Diagram Conference with mentor (by Fri, Nov. 4)
  - Review major components and overall design approach
  - Specify the device components you need to acquire (*small* budget allocated for each project if component does not exist in the stock room). Get approval and will contact John Sweeney to obtain the parts.

Schedule (cont'd.)

- Project Design Presentation to class (Nov 10 & 12 2:30-5p 1-190)
  - Each group will make a 10-15 min electronic presentation (~10 slides) dividing presentation among team members
  - Submit PDF on-line, will be posted on website
  - Example: F2011 Recursive Augmented Reality
  - Required attendance (3% grade)
- Project Checkoff Checklist to staff (by Nov 18)
  - Each group in discussion with mentor creates a checklist of deliverables (i.e., what we can expect each team member to demonstrate). Submit PDF on-line. Three groups:
    - Commitment – minimum goals; complexity 2x lab 4
      "Stuff we need in order to have not failed completely."
    - Expected – needed for successful project
      "Stuff we need in order to succeed"
    - Stretch goal – stands out in complexity, innovation, risks
      "Stuff we need in order to be awesome"

Schedule (cont'd.)

- Final Project Demo/Checkoff/Videotape (Dec 12 & 13)
  - Videotaped and posted on-line with your permission
- Final Project Report (Wed, Dec 14 5PM)
  - Submit PDF on-line, will be posted on website
  - Sorry, <u>no late checkoffs or reports</u> will be accepted

2016 End of Term Crunch

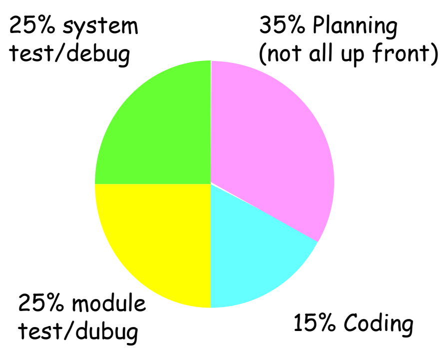
Oct 17	L11: Project kickoff; proposals and presentations	L12: Memories: on-chip, SRAM, DRAM, Flash Project abstract due Lab #5 checkoff
Oct 24	L13: Potpourri: FFT, FPGAs, RFID, Tools Proposal Conferences Work on Project Proposal	L14: VLSI and power Proposal Conferences Work on Project Proposal
Oct 31	Project Proposal Draft due	Project Block Diagram Meeting by 11/04 (Fri) by 5pm
Nov 07	Project Design Presentations (2:30-5PM room TBD) - attendance required	Project Design Presentations (2:30-5PM room TBD) - attendance required
Nov 14	Project Checklist Meeting with Staff Revised Project Proposals due 11/18 (Fri) by 5pm	Final project Project Checklist Meeting with Staff by 11/18 (Fri) by 5pm
Nov 21	Final project Short week	*Thanksgiving*
Nov 28	Final project integrtion and debugging - finishing touches! Two weeks remaining!	
Dec 05	Final project - finishing touches!	Final project - polishing! ...
Dec 12	Project Checkoff/Video recording Mon/Tue Return tool kits Tue	Wed project Report due 12/14@ 5PM (Wed) Tie up loose ends

Team Organization

- Most importantly, you need one
- Key decisions made jointly
  - Requirements
  - High level design
  - Schedule
  - Who will work on what, who'll take the lead
  - Response to slippage
- Lower level design exchanged for examination
  - Everyone responsible for everything
  - Design reviews tremendously helpful
    - Try it, you'll like it
- Communicate with each other early and often

Controlling Schedule

- First, you must have one
- Need verifiable milestones
- Some non-verifiable milestones
  - 90% of coding done,
  - 90% of debugging done,
  - Design complete
- Need 100% events
  - Module 100% coded,
  - Unit testing complete
- Need critical path chart
  - Know effects of slippage
  - Know what to work on when



Provide a 4-7 day contingency to deal with unforeseen issues (you'll use it all!)

Choosing A Topic

- You only have 6 weeks total (once your proposal abstract is turned in) to do this project.
  - It is important to complete your project.
  - It is very difficult to receive an "A" in the class without having something working for the final project.
- The complexity for each team member should 3 times the complexity of the lab assignments.
- Some projects include analog building blocks or mechanical assemblies (infrared, wireless, motors, etc.). However, keep in mind that this is a digital design class and your design will be evaluated on its digital design aspects.
- Complexity, risk and innovation factor.
  - We will give credit to innovative applications, design approaches
  - More complex is not necessarily better
- Look through previous projects for inspiration (see website)

Sample Projects

- Live Action Mario Kart
  - Brad Gross, Jono Matthews, Nate Rodman
- Cryptographically Protected Telephone System
  - Andres Erbsen, Adam Yedidia
- Virtual Drum
  - Luis Fernandez, Rishi Naidu
- A Hardware-based Image Perspective Correction System
  - Matthew Hollands, Patrick Yang

Final Project Ideas

- **Gadgets, digital systems**
  - FPGA Function Generator with laser display
  - Multimeter with voice output
  - Analog Voltmeter
  - FPGA Fitbit
  - MIT ID reader
  - Remote control hand movement
  - Virtual golf
  - Virtual basketball
  - Camera based arcade game
  - Motion tracker alarm system

- **Graphics/Video**
  - Star Wars Virtual Light Saber
  - 3D fly by
  - Movement tracker/playback
  - Real time animation with camera
  - Airplane console
  - Wire frame editor/display
  - Camera with blue screen
  - Virtual postcard
  - 3D display (two cameras – tough!)
- Audio, music, lighting
  - Music synthesizer
  - FPGA phone system
  - DJ Control system
  - Light panel control system
  - Virtual surround sound
  - Time stretching audio or Time domain harmonic scaling (not for faint of heart)

Some Suggestions

- Be ambitious!
  - But choose a sequence of milestones that are increasingly ambitious (that way at least part of your project will work and you can debug features incrementally).
  - But don't expect 400Mhz operating frequencies, etc.
- It's motivating if there's something to see or hear
  - Video and graphics projects are fun (and with the labkit basic video input and output are pretty straightforward which means you can concentrate on the processing)
  - Audio/Music is low-bandwidth, so it's easy to do interesting processing in real-time (real-time is harder with video).
- Memories are often the limiting factor
  - Figure out how you'll use memory blocks early-on
- Be prepared for unpleasant surprises. Unlike the labs, there may be no solution for a particular design approach!

More Suggestions

- Be modular!
  - Figure out how test your modules incrementally (good for debugging and checkoff!)
  - Be clear about what information is passed between modules (format, timing)
- Don't be caught by the mañana principle
  - Six weeks goes by quickly: have a weekly task list.
  - How does a project run late: one day at a time!
  - Effort is not the same as progress: "Written but not tested" only means you've made a start
  - Tasks will take longer than you think
  - Final integration will uncover bugs/thinkos so test module-to-module interactions as early as you can

Design Suggestions

- Use hierarchical design
  - Partition your design into small subsystems that are easier to design and test.
  - Design each sub-system so they can be tested individually.
  - When appropriate, use Major/Minor FSMs.
- Use the same clock edge for all edge-triggered flip-flops
  - Beware of clock skew, don't gate the clock
  - If you have multiple clock domains, think very carefully about how you transfer information from one to another
- Avoid problems from 'glitches'.
  - Always assume that combinational logic glitches
  - Never drive a critical asynchronous control signal (register clock, write enable) from the output of combinational logic.
  - Ensure a stable combinational output before it is sampled by CLK.
  - When needed, create glitch-free signals by registering outputs.

Design Suggestions (cont'd.)

- Avoid tri-state bus contention by design
- Synchronize all asynchronous signals
  - Use two back-to-back registers
- Use asynchronous memories properly
  - Avoid high Z address to SRAM when CE is asserted.
  - Avoid address changes when WE is true.
  - Make sure your write pulse is glitch free.
- Use care when incorporating external devices
  - Use bypass capacitors on external components to deal with noise
  - I/O pads are slow, not all signals have the same delay
- Chip-to-chip communication
  - Beware of noise (inductance)
  - Might need to synchronize signals
  - Can also use "asynchronous" protocols

Project Grading (35% Total)

- Deadlines and effort (8 %)
- Problem Definition and Relevance, Architecture, Design methodology (10%)
  - What is the problem
  - Why is it important or interesting
  - System architecture and partitioning
  - Design choices and principles used
  - Style of coding
  - All of the above should be stated in the project and report
- Functionality (8 %)
  - Did you complete what you promised (i.e., graded by the checklist)
- Complexity, Innovation, Risk (9 %)

Project Grading

- Functionality grading
  - It works in simulation: grade 0%
  - Unable to demo/test because my partners' module isn't working: grade 0%
- General project grading guidelines
  - approximately 2x hardest lab: grade 10-19
  - demonstrates a superior understanding to digital systems and implementing complex systems - perhaps with multiple time domains, interface to external devices, flash memory, audio, etc. 20-29
  - a top notch project that really stands outs with complexity, innovation and risk 30-35

Presentation & Report Grading (13%)

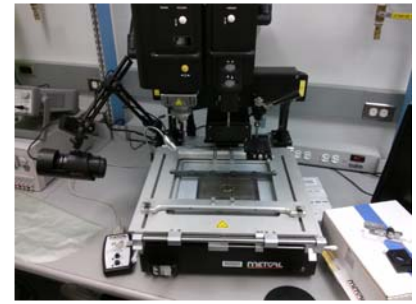
- Project Proposal (2%)
- Class Presentation (6%)
- Final report (5% technical)

Required Attendance (3%)

- Design presentations 2:30-5:00p
  Tue Nov 8, Thur Nov 10

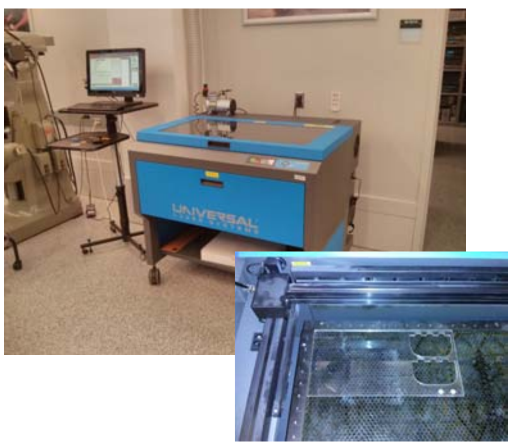
Electronic Design Studio (EDS)

Surface mount solder stations (4)



Surface mount placement

Electronic Design Studio (EDS)

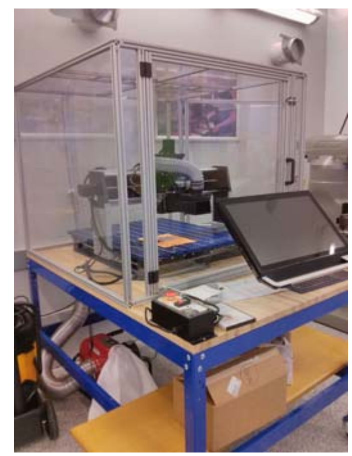


Laser cuter – PSL6.75 with 75W laser
Part size: 32" x 18" x 9"
Cut by "printing"

Bridgeport NC Milling Machine

Electronic Design Studio (EDS)

Bridgeport NC Milling Machine



NC Router