

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

6.111 Introductory Digital Systems Laboratory
Fall 2016

Lecture PSet #2
Due: Thu, 09/15/16

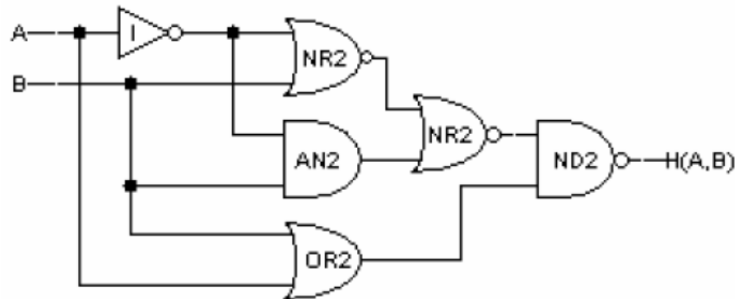
Problem 1. A certain function F has the following truth table:

| A | B | C | $F(A,B,C)$ |
|---|---|---|------------|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

- (A) Write a sum-of-products expression for F .
- (B) Write a minimal sum-of-products expression for F (use Karnaugh maps). Show a combinational circuit that implements F using only INV and NAND gates (make sure that you use the right gate symbols with bubbles placed so that inversions are cancelled).
- (C) Implement $F(A,B,C)$ using only the 4-to-1 multiplexer with following signals available as inputs: the constants 0 and 1; signals A , B , C , or their inversions.
- (D) Write a product-of-sums expression for F and minimize using Karnaugh maps

Problem 2.

Consider the following circuit that implements the 2-input function $H(A,B)$:

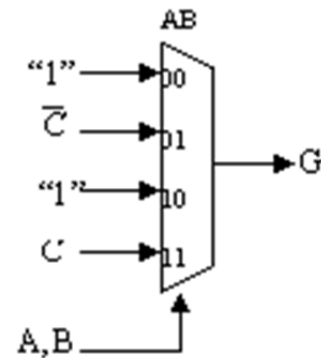


(see other side)

- (A) Write a truth table for this circuit
- (B) Give a sum-of-products expression that corresponds to the truth table in (A) (the expression does not have to be minimal sum-of-products) and check if it is minimal using a Karnaugh map. If not, provide a minimized sum-of-products.
- (C) Using the following table of timing specifications for each component (roughly corresponding to a 45nm CMOS technology – state of the art circa 2014: 14nm), what are t_{CD} and t_{PD} for the circuit shown above? (Write-out the delays that contribute to each of the two.)

| Gate | t_{CD} [ps] | t_{PD} [ps] |
|------|---------------|---------------|
| I | 5 | 15 |
| ND2 | 7 | 25 |
| AN2 | 8 | 45 |
| NR2 | 9 | 35 |
| OR2 | 11 | 55 |

Problem 3. A certain 3-input function $G(A,B,C)$ has the implementation shown to the right. Give a minimal sum-of-products expression for G .



Problem 4. Implement the 2-bit adder function (i.e., 2-bit binary number AB plus 2-bit binary number CD yields a 3-bit result XYZ) using 4:1 multiplexers.

- (A) Give the truth table showing the values for the outputs X , Y and Z given all possible combinations of the inputs A , B , and C , D .
- (B) Show how to implement X , Y and Z using the minimal number of 4:1 multiplexers. You can assume you have only the constants 0 and 1; the inputs (but not its complements) and 4:1 multipliers. How many 4:1 multiplexers are needed?