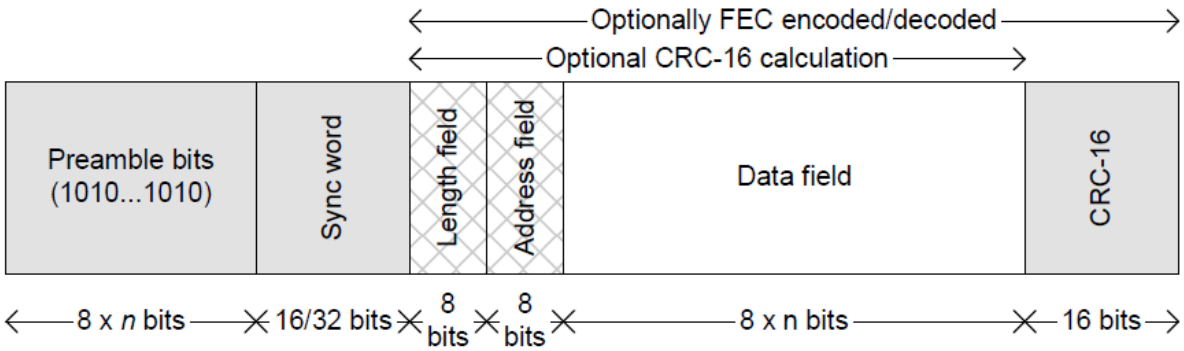
M A S S A C H U S E T T S I N S T I T U T E O F T E C H N O L O G Y
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

6.111 Introductory Digital Systems Laboratory

Fall 2016
Lecture PSet #6
Due: Wed 10/5/2016 upload by 14:30

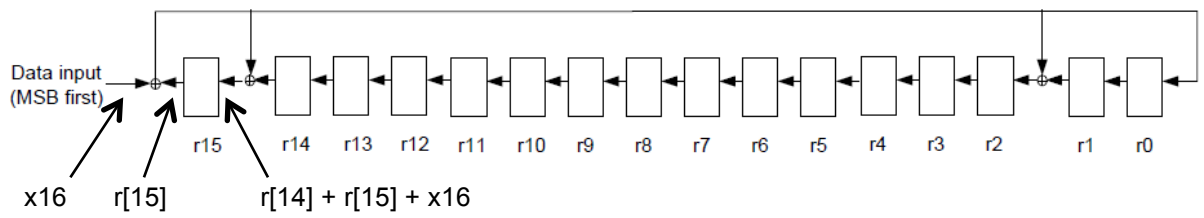
This LPset requires ISE. The LPset is based on an actual FPGA implementation for a low power wireless ECG monitor attached to a patient. In this application, the ECG data is transmitted to a receiver at a base station located at a nurse's station.

A typical transmitted data packet is show below:



The preamble bits and sync word are used by the receiver for synchronization. For this problem, you will only be concerned with the three blocks of data consisting of the Length Field, Address Field and Data Field. FEC is forward error correction, a technique that allows a receiver to correct errors in a received packet by convolving the data and sending the parity bits. More on FEC in Lpset #7.

Cyclic Redundancy Check (CRC) is used to detect errors in data transmission and is capable of detecting all single and double errors and many multiple errors with a small number of bits. CRC is generated by a modulo 2 division with a generator polynomial. The remainder is the CRC. For our application, the generator polynomial is CRC16 (x16 + x15 + x2 + 1) with the CRC register initialized to all 1's prior to calculating the CRC. [CRC16 is the generator polynomial for data packets in the USB: http://www.usb.org/developers/docs/whitepapers/crcdes.pdf.] Initializing to all 1's ensures that leading 0s in front of a packet are protected by the CRC. The figure below shows the shift register implementation for the CRC.



In the shift register implementation, each "r" is a register, all clocked with a common clock. The common clock is NOT shown. The small round circles with the plus sign in the diagram are adders implemented with XOR gates. As shown, for register r15, the input is the sum of r[14], r[15] and data input x16; and the output is r[15] .

You can see from the location of the XOR gates (input to r15, r2 and r0) in the shift register configuration how CRC16 (x16 + x15 + x2 + 1) is implemented. The data input is x16 with the most significant ***bit*** (MSB) shifted in first. With each clock pulse, the next data bit is provided to x16. Using this hardware will give the following result:

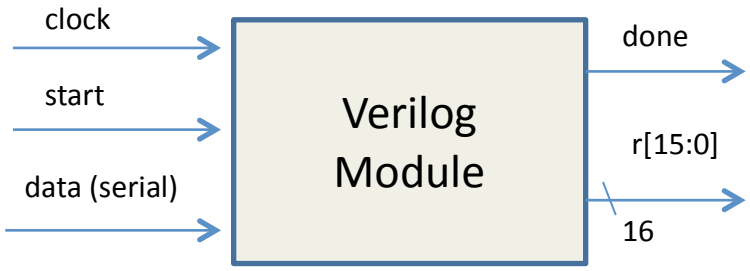
Input: [4 bytes] **03 01 02 03**
Appended with CRC: [6 bytes] **03 01 02 03 30 3A**

In this example the first six data bits sent to x16 are six zero followed by two ones [**03].** After 32 bits are shifted in, the value in r[15:0] is the CRC [30 3A].

The CRC calculation is such that sending the data and appended CRC (6 bytes) through the same hardware used to generate the CRC will give a CRC of [00]. (Engineers are clever!)

Problem: Write a Verilog module that takes the data, run it through the CRC generator and calculates the CRC. The input **start** pulses high for one clock cycle when data is available. When CRC calculation is completed, done is asserted with r[15:0] containing the CRC for the incoming data. Since the data input has the CRC appended, the resultant CRC is [00]. Be sure to initialize r[15:0] to 16'hFFFF at the start. For performance, done must be assert as soon as the all 48 bits are processed (i.e. same clock edge).

data input 48'h03_01_02_03_30_3A



Getting started:
Step 1: Using ISE, create a new Verilog module with inputs and outputs as shown above.
Step 2: The Verilog module: when **start** is asserted, reset your FSM; reset counters and other registers; and load any initial values. When **start** is deasserted, with each clock pulse, begin the CRC calculation. Assert **done** when 48 bits are processed. The module should use only one clock domain always @(posedge clock).
Step 3: Using ISE and the attached test bench (also posted on the course website) verify your design with a simulation using the process outlined in Lab 2 exercise 1(b). The test bench includes a 5ns clock. Note the syntax [@posedge] for a test bench is slightly different than a Verilog module. The input data is 48'h03_01_02_03_30_3A and sent one bit at time. The first eight bits sent to the Verilog module are six zero followed by two ones corresponding to hex [03]. You may modify the test bench if needed for your implementation (generally not the

case). In the actual FPGA ECG implementation, the data length is variable and processed one byte at a time.

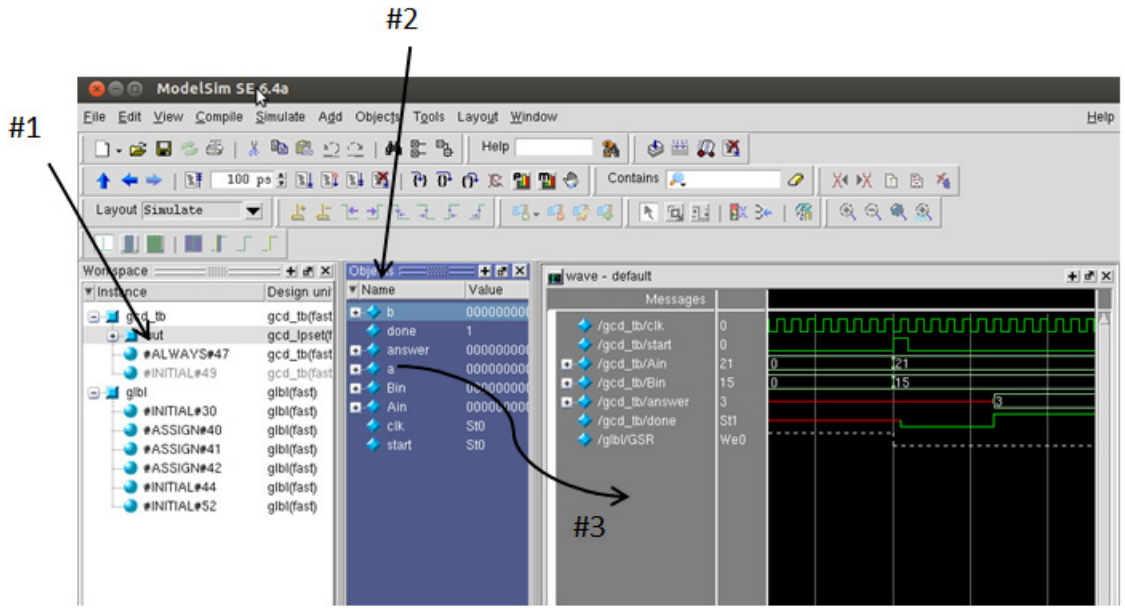
Step 4: Take a screen shot showing r[15:0] after 32 bits are shifted in and a screen shot showing r[15:0] when **done** is asserted. Use hex radix for r[15:0]. Include the Verilog and screen shots in one pdf file. Upload to the course website.

Lpset grading rubric

Grading	
1	Easy to read & formatted Verilog (See "Verilog Editors" tab for help.)
1	Correct use of blocking/non-blocking assignments
1	Comments in Verilog when needed
3	Functional Verilog & test bench
2	Screen Shot 1 r[15:0] after 32 bits are shifted in
2	Screen Shot 2 r[15:0] when **done** is asserted
10	**Total Grade**

In simulation, state values are unknown unless explicitly set. (Unknown values are shown in red during simulation. Outputs not defined are shown in blue.) For a simulation to run correctly, state variables must be initialized or set to some value at some point in the simulation. This can be accomplished by using a reset (recommended) or other input. For the CRC you can use the **start** pulse to initialize the CRC:

In simulation, by default, only inputs and outputs from the unit under test are displayed in the Wave window. It may be useful to display internal wires in your module that are not inputs nor outputs, for example, a bit counter. After running the initial simulation, to display the internal wires, click "uut" (unit under test) in the Workspace window (#1). This will display the internal signals in the Object window (#2). Drag the desired signals to the Wave window (#3).



To display the additional signals, rerun the simulation. In the Transcript window, type

```
restart -f     // force a restart
run 2000ns     // run simulation for 2000ns (longer if needed)
```

```
`timescale 1ns / 1ps
////////////////////////////////////////////////////////////////////////////////
//
// lpset CRC test bench
//
////////////////////////////////////////////////////////////////////////////////

module crc_tf;

      // Inputs
      reg clock;
      reg start;
      reg data;

      // Outputs
      wire done;
      wire [15:0] r;

   // Instantiate the Unit Under Test (UUT)
   lpset_crc uut (
      .clock(clock),
      .start(start),
      .data(data),
      .done(done),
      .r(r)
   );

   // this is the input data
   reg [47:0] input_data = 48'h03_01_02_03_30_3A;

   integer i;                       // required for "for" loop
   always #5 clock = !clock;
   initial begin
      // Initialize Inputs
      clock = 0;
      start = 0;
      data = 0;

      // Wait 100 ns for global reset to finish
      #100;

      // Add stimulus here
      start=1;
      #10 start = 0;

       for (i=0; i<48; i=i+1)
       begin
         data = input_data[47];
         // at each clock, left shift the data
         // note syntax for test bench "for" loop - no "always"
         // note the blocking assignment (immediate)
         @(posedge clock) input_data = {input_data[46:0],1'b0};
       end

   $stop; // Pause simulation

   end

   endmodule
```