USING FLASH IN LABKIT

Flash Memory – Nitty Gritty

- Flash memory limitations
  - Can be read or written byte a time
  - Can only be erased block at a time
  - Erasure sets bits to 1.
  - Location can be re-written if the new bit is zero.

Flash is slow, cache to RAM for fast read speed

- Labkit has 128Mbits of memory in 1Mbit blocks.
  - 3 Volt Intel StrataFlash® Memory (28F128J3A)
  - 100,000 min erase cycle per block
  - Block erasures takes one second
  - 15 minutes to write entire flash ROM

http://www.embeddedintel.com/special_features.php?article=124

Flash Verilog

- flash_int.v - does the very low level manipulation.
- test_fsm.v - does the medium level manipulation (heavily modified from the test code linked above)
  - NOTE: modify parameter MAX_ADDRESS = 23'h030000 if more memory is needed
- flash_manager.v - does the high level manipulation. This is the ONLY Verilog in the top-level labkit (instantiates a flash_int and test_fsm)

Flash control lines

- writemode: // if true then write mode
- doread: // high does a read at current address
- dowrite: //putting this high tells the flash manager it has data, write it
- reset: // used for block erase
- busy: // flash in use; no “done” signal

To Reset

writemode = 1
dowrite = 0
doread = 0
reset = 1 (pulse)

Flash Hints & Idiosyncrasies

- use simply Verilog to characterize flash
  - Write known pattern and verify with read
- flash reads/writes cycle time varies – use busy signal
- full flash erasure takes 15 minutes; use minimum to reduce time
- read and read again
  http://web.mit.edu/6.111/www/f2016/projects/diana96_Project_Final_Report.pdf
- flash_manager.v make sure startup state = 2
  reg[2:0] state=2;