Debugging hints

- It's easiest to debug if the recorder/playback or IR sampling module is created as a separate module for simulation. Otherwise all the other labkit signals will be displayed in the waveform window. In addition, you will need to comment out the first line with `` `default_nettype none `` if you choose to simulate the entire labkit.v. With `default_nettype none` Modelsim requires each signal to be declared as a wire.

- The AC97 ready signal occurs every 27,000,000/48,000 times. To shorten the simulation, use the following in your test fixture:

```
always #5 clock_27mhz=!clock_27mhz;
always begin
#5 ready = 1;  // ready occurs every 14 cycles
#10 ready = 0;
#115;
end


initial begin // Initialize Inputs
clock_27mhz = 0;
ready = 0; . .
```

- For the IR lab, it takes many clock_27mhz cycles before each sampling of the signal. You can use the same technique from above to shorten simulation time.