M A S S A C H U S E T T S I N S T I T U T E O F T E C H N O L O G Y
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

6.111 Introductory Digital Systems Laboratory
Fall 2017

Lecture PSet #2
Due: Thu, 09/14/17

Problem 1 (4 pts). [Unlike MIT lpsets where the problem is clearly and neatly structured, in the real world, necessary information for the task is there but typically scattered across multiple sources. This problem is a sample of what you might encounter as an engineer.]

One way to transfer data from the 6.111 labkit to a PC is to use a serial to USB adapter. One approach (as you will see in lab 2) is to transfer data from the labkit to PC via the RS232 port on the labkit using a CH340g serial to USB IC. For this transfer, there are two signals used: transmit data (TXD), received data (RXD), and a common ground, so three wires total.

The labkit RS232 port is implemented using the MAX32222 IC
http://web.mit.edu/6.111/www/f2017/serial/max3222.pdf

The schematic of the labkit with the RS232 port details are provided in
http://www-mtl.mit.edu/Courses/6.111/labkit/labkit_schematic.pdf

Based on the above information,

(a) As a design engineer using good engineering practice, what would you specify as the maximum data transfer rate to be published in a "*labkit datasheet*"? When cable capacitance is taken into account the real transfer rate will be further reduced. In practice, RS232 cables have capacitance (17 pF/ft. https://www.lammertbies.nl/comm/info/RS-232_specs.html) that limits the maximum cable length and transfer rate. Assume a perfect cable for this spec.

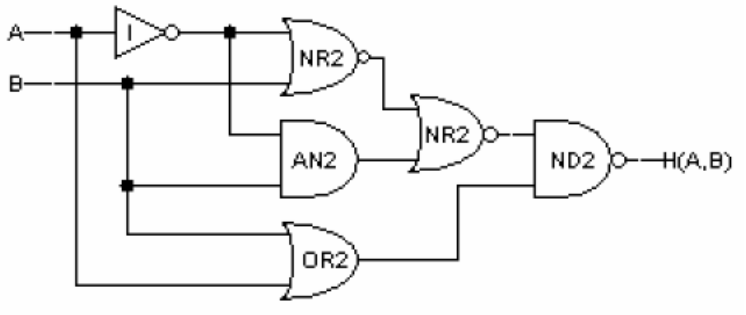
(b) As a student hacking on a project, what could you hope to achieve as the maximum transfer from the labkit? Explain your reasoning.

(c) In order to reduce cost and effort, you wire the CH340g directly to the RS232 port without line drivers. (This may be the case with very inexpensive adapters on ebay.) Are the voltage specifications compatible? It not describes the problems. The specifications for the CH340g IC are show in the datasheet
http://web.mit.edu/6.111/www/f2017/serial/ch340g.pdf

(see other side)

Problem 2 (3 pts).

Consider the following circuit that implements the 2-input function H(A,B):



(A) Write a truth table for this circuit

(B) Give a sum-of-products expression that corresponds to the truth table in (A) (the expression does not have to be minimal sum-of-products) and check if it is minimal using a Karnaugh map. If not, provide a minimized sum-of-products.

(C) Using the following table of timing specifications for each component (roughly corresponding to a 45nm CMOS technology – state of the art circa 2014: 14nm), what are t_{CD} and t_{PD} for the circuit shown above? (Write-out the delays that contribute to each of the two.)

Gate	t_{CD} [ps]	t_{PD} [ps]
I	5	15
ND2	7	25
AN2	8	45
NR2	9	35
OR2	11	55

Problem 3 (3 pts). [In ancient, pre-FPGA, times when you run out of certain IC's for a project, you must be resourceful and use what's available. This problem gives you a taste of the those days.]

Implement the 2-bit adder function (i.e., 2-bit binary number AB plus 2-bit binary number CD yields a 4-bit result XYZ) using 4:1 multiplexers.

(A) Give the truth table showing the values for the outputs X, Y and Z given all possible combinations of the inputs A, B, and C, D.

(B) Show how to implement X, Y and Z using the minimal number of 4:1 multiplexers. You can assume you have only the constants 0 and 1; the inputs (but not its complements) and 4:1 multipliers. How many 4:1 multiplexers are needed?