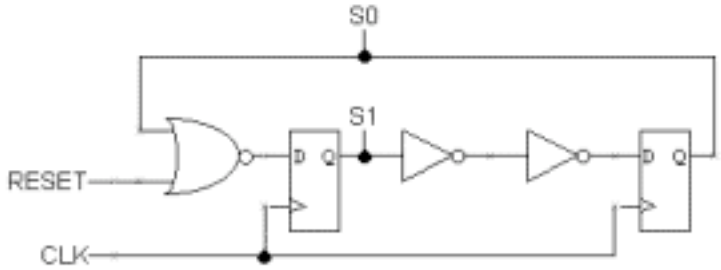
M A S S A C H U S E T T S I N S T I T U T E O F T E C H N O L O G Y
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

6.111 Introductory Digital Systems Laboratory
Fall 2017

Lecture PSet #4
Due: Upload as PDF by 14:30 - Thu, 09/21/2017
Note: Please type your solutions; no credit for hand written solutions

Problem 1. Consider the following circuit diagram with signals S0 and S1:



inverter: t_{CD}=1ns, t_{PD}=2ns
nor2: t_{CD}=1.5ns, t_{PD}=2ns
D register: t_{CD}=0ns, t_{PD}=2ns, t_H=1ns, t_S=3ns

(A) What is the smallest clock period for which the circuit still operates correctly?

(B) A sharp-eyed student suggests optimizing the circuit by removing the pair of inverters and connecting the Q output of the left register directly to the D input of the right register. If the clock period could be adjusted appropriately, would the optimized circuit operate correctly? If yes, explain the adjustment to the clock period that would be needed.

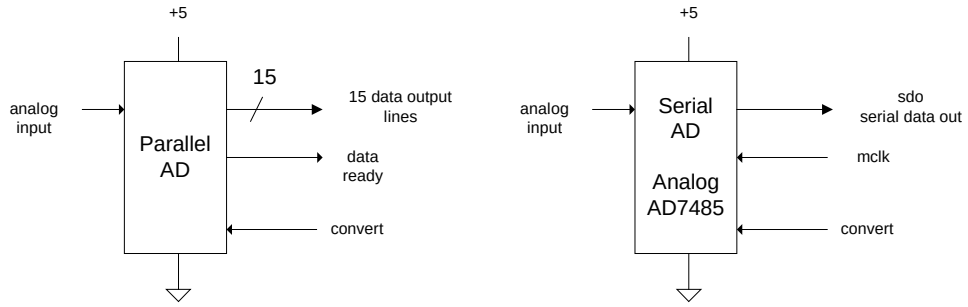
(C) When the RESET signal is set to "1" for several cycles, what values are loaded into the registers? (Give values for S0 and S1.)

(D) Assuming the RESET signal has been set to "0" and will stay that way, what value will with the registers have after the next clock edge assuming the current values are S0=1 and S1=1?

(E) Now suppose there is skew in the CLK signal such that the rising edge of CLK always arrives at the left register exactly 1ns before it arrives at the right register. What is the smallest clock period for which the FSM still operates correctly?

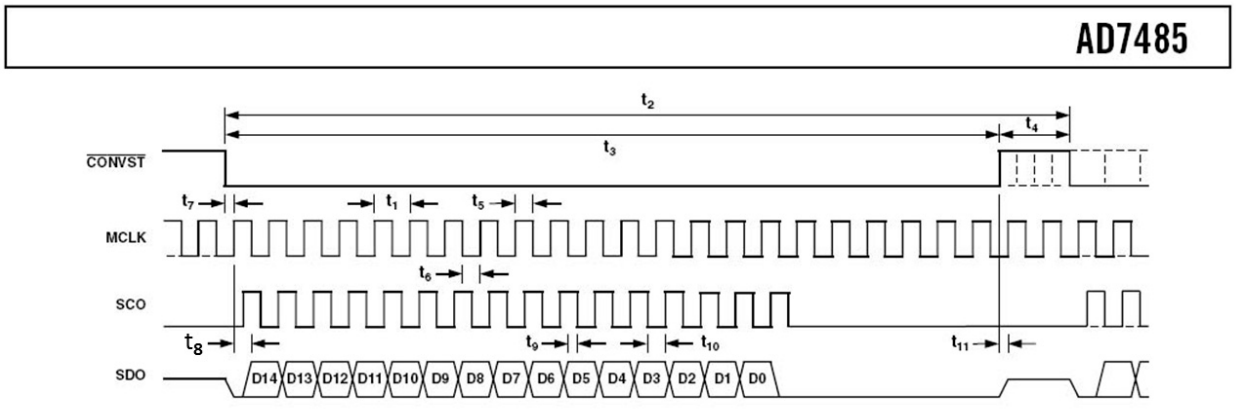
(see other side)

Problem 2. [This problem is another example you might face as an engineer or in your final project. *The questions are not intended to be tricky or required long analysis.]* Analog to digital converters (ADCs) are used to provide data input to digital systems for processing. The analog signals are converted to binary data with resolution ranging from 8 to 24 plus bits. ADCs are available with parallel or serial digital outputs. The advantage of serial output is fewer wires and interconnects but requires the added complexity of a serial to parallel conversion on the digital side. This is something to consider at project time should your project require an ADC: wires vs Verilog! One performance metric for ADCs is samples per second. Parallel output ADCs are faster - i.e. more samples per second. The following is a simplified diagram of each type of ADC.



An example of a serial ADC is the Analog Devices AD7485, a 14 bit AD converter with serial output. The AD7485 uses a system clock, MCLK, provided by the user. To start the AD conversion, assert CONVST_bar (bar = line above CONVST) low. SCO is system clock out which you can ignore for this exercise.

SDO, serial data out, consists of 15 bits of data. The over range bit (D14) is latched out first, then 14 bits of data (MSB first) followed by a trailing zero.



(see other side)

All timing parameters are provided in terms of t_1.
For the AD7485, $40ns < t_1 < 100{,}000ns$
$t_{2\ (min)} = t_1 \times 24$
$t_{3\ (min)} = t_1 \times 22$. All other timing parameters can be ignored for this problem.

(a) What is the maximum number of samples per second for this device?

(b) The labkit 27mhz system clock has a period of 37ns which is beyond the spec for t_1. A 13.5mhz clock is created by simply dividing the clock by 2. What is the sampling rate of the ADC using a 13.5mhz clock? [In lab 3, you will learn about using the digital clock manager, DCM, to create other clock frequencies.]

[Analog Devices was founded by Ray Stata, the major contributor to the Stata Center. Analog Devices provides free samples of their products for use in 6.111 final projects.]