

Massachusetts Institute of Technology  
Department of Electrical Engineering and Computer Science

**6.111 – Introductory Digital Systems Laboratory**

**General Information**

**In-charge**

Prof. Anantha Chandrakasan, Room 38-107, 258-7619, [anantha@mtl.mit.edu](mailto:anantha@mtl.mit.edu)

**Lecturers**

Prof. Anantha Chandrakasan, Room 38-107, 258-7619, [anantha@mtl.mit.edu](mailto:anantha@mtl.mit.edu)

Prof. Donald E. Troxel, Room 36-287, 3-2570, [troxel@mit.edu](mailto:troxel@mit.edu)

**Secretary**

Margaret Flaherty, Room 38-107, 3-0016, [meg@mtl.mit.edu](mailto:meg@mtl.mit.edu)

**TAs**

Cemal Akcaba ([akcabac@mit.edu](mailto:akcabac@mit.edu), 38-600, 3-7350)

Jia Fu Cen ([jjafu@mit.edu](mailto:jjafu@mit.edu), 38-600, 3-7350)

David Milliner ([d1m@mit.edu](mailto:d1m@mit.edu), 38-600, 3-7350)

**Recommended Reading** (Purchase is NOT required).

**Logic Design:**

- Randy H. Katz, Contemporary Logic Design, Addison Wesley, MA, 1993 .

**Verilog:** there are plenty of good Verilog books. We strongly recommend that you get a Verilog book. A couple of suggestions are given below:

- Samir Palnitkar, Verilog HDL, Pearson Education (2<sup>nd</sup> edition).
- Donald Thomas, Philip Moorby, The Verilog Hardware Description Language, Fifth Edition, Kluwer Academic Publishers.

*(Quantum Books, located at 4 Cambridge Center, Kendall Square, Phone: (617) 494-5042, [www.quantumbooks.com](http://www.quantumbooks.com)).*

**6.111 Homepage** <http://web.mit.edu/6.111/www/s2004/>

**Component Pinouts/Data**

Pinouts for most components easily available through the web (e.g., do a google search to locate the appropriate data sheet). We will post most of the relevant sheets needed for the labs on the course web site.

**Drawing Template**

You do not have to use a template for drawing logic diagrams on the quiz. **All** logic diagrams submitted in this subject **must** be drawn with a template or on a computer, except for the quiz, where all that is required is that logic diagrams be legible. For homework and lab preparation,

you may use a drawing template, though it is likely that you will use a computer-based drawing package. Preferred templates: MIL-STD-806C, in 1/2, 3/8 or 3/4 size, Koh-I-Noor No. 830544 or equivalent in Rapid Design or Pickett. (*Templates are available at University Stationery (311 Massachusetts Ave.) and perhaps at the COOP (at Kendall Square).*)

**Conduct of the Subject** (minor changes may be made):

### **Classes**

In the first couple of weeks the term, there will be lectures on Friday (to quickly ramp up on material needed for lab 1). Then, Fridays will be used for recitations (three parallel recitation sections from 1-2pm). Lectures and recitations are discontinued at the end of the term so you can focus on the final project (see course schedule for details). We will meet you frequently in the laboratory. We will meet in the lecture hall (34-101) for project group presentations after the block diagram conferences. Notification of particulars of the project presentations will be sent by email to 6.111students@mit.edu.

### **Problem Sets**

Three sets will be issued and your solutions will be graded; these are based on the lectures and recitations. The goal of the problem sets is to reinforce lecture/recitation material and help prepare you for the labs.

### **Laboratory Assignments**

All laboratory exercises must be completed; these are intended to prepare you for the term project. In doing these exercises, each student works individually.

### **Quiz**

There will be one quiz during the term before Drop Date.

### **Term Project**

The most important assignment is the Term Project, about which you will receive more detailed instruction later. In doing this assignment, you will work with one or, at most, two partners. You should begin finding your partner(s) early in the term.

### **Grading Policy**

Late work will be penalized. Late homework will not be accepted. Lateness of the lab assignments will result in a 20% per day penalty for work completed 1-5 working days after the due date. No point credit will be given for unexcused lateness exceeding 5 days.

The Lab 1 Checkoff sheet is to be initialed by a TA or LA and included with your report. Note that the checkoff sheet is NOT the report. Lab 1 report template is posted on the web site.

Lab 2 report will be used for part of the CIM requirement. More details will be provided in lecture. Lab 2 checkoff and final report are due on the same day.

Lab 3 has an intermediate checkoff and the final checkoff and report are due on the same day. There is virtually no modification required to a report depending on the working of your lab implementation. However, reports with no lab effort will receive a zero.

The term project requirements *must* be completed in accordance with the schedule given in the instructions. You must make a presentation of your part of your project to the rest of the class

after the logic diagram conference. You must demonstrate (i.e., present) your term project even if it does not fully function, and you must submit the written report in order to receive a passing grade.

The assignment of letter grades (A,B,C,D,F) is an inherently subjective process. We do, however, make use of numerical data. A single number is computed by weighting graded assignments. The following weights will be used:

Quiz	10%
Writing (Lab 2 revision- part of CIM requirement)	10%
3 Problem Sets (emphasis on lab concepts)	5%
Participation (lecture, recitation, labs)	5%
3 Lab Exercises	
Lab 1	10%
Lab 2	10%
Lab 3	15%
Final Project	35%

We construct a histogram of these summary numbers and proceed to discuss individual performances of virtually all students. Some of the factors considered are:

1. Diligence as measured by completion of most of the problem sets and by presence in the laboratory during final project time.
2. Completion of Labs 2 and 3. Past history has been that it is extremely rare for a student to receive an A without completing Lab 3. Of course, it is possible to get a grade lower than an A even if Lab 3 is done.
3. Project performance.
  - a) Any student who does not turn in a final project report will receive an F.
  - b) Students who do not construct a project will receive an F.
  - c) Project complexity is an important factor in discriminating between an A and a B. An A is rarely given if the final project is not as complicated as the last Lab.
  - d) **It is extremely difficult for a student to receive an A without completing the final project.** Of course, it is possible to get a grade lower than an A even if the final project is completed.

Although 6.111 has a significant classroom component, it is *primarily* a lab subject. Accomplishments in the lab tend to be weighted more heavily than other components. The classroom component is viewed as supportive of the lab components. Some material covered in lectures will be related to advanced topics (power dissipation, mapping to ASICs, testing, etc.). Some the concepts might not be applicable to your final project but are important emerging digital system issues in industry today.

Traditionally, both average grade levels and average performance have been quite high in 6.111. A large number of students do "A" level work and are, indeed, rewarded with a grade of

A. The corollary to this is that, since average performance levels are so high, punting any part of the subject, even the problem sets, can lead to a disappointing grade. It is important that you keep up with the work.

Finally, and unfortunately, it is important for us to outline our expectations for academic honesty in 6.111. We do this not because we expect any of you to be dishonest, nor to insult your intelligence or character, but to avoid any misunderstandings.

First, the quiz is to be an individual effort. The problem sets and lab exercises are also to be individual efforts; however, it is okay to ask questions, get help from us, fellow students, or anyone else. But then, do them by yourself. Indications of collaboration such as incidents of identical code or copied figures are unacceptable and are liable to be dealt with in a seemingly harsh fashion. The TA's will be asking you about your solutions to make sure you really do understand what you have done.

The Final Project is a different story. We do expect you to collaborate, with the course staff and with your fellow students, especially with your lab partner. Joint or individual reports are acceptable, but in the case of joint reports it is important that responsibility for each section of the work be indicated.

### **Laboratory**

The laboratory facilities are located on the sixth floor of Building 38. Read the General Laboratory Information handout. **PUT YOUR NAME ON ANYTHING THAT YOU BUILD IN THE LABORATORY AND LEAVE UNATTENDED. OTHERWISE, IT MAY BE GONE WHEN YOU RETURN.**

### **Schedule**

The schedule of the lectures and assignments is in this packet. The schedule of the lectures and assignments is posted (and will be updated regularly) on the course website. Staying on schedule is very important in this subject, in order to be prepared to do the term project, which is the single most important assignment in 6.111. It will be an enjoyable experience if you are properly prepared.

### **Extra Units for 6.111**

Many 6.111 students spend more hours per week than warranted by the 12 unit rating. Primarily this is due to large final projects. It is now possible to register for 6.905 and gain an additional 6 units of credit for 6.111. Your grade for 6.905 will be the same as your grade for 6.111. Your grade for 6.111 is not influenced by registration for 6.905.

Our motivation for enabling the availability of these extra units is two-fold. Foremost is our desire to convince 6.111 students that they need *not* do a project which is bigger and more complicated than ever done in the past. Secondly, recognizing that many students will continue to do ambitious projects, we would like to credit 6.111 students with units appropriate to work expended. Procedures for registering for the extra units by DROP date will be announced later on in the term.

Both the determination of grades and the project time requirements are inherently subjective. The last Lab provides some guidance to the evaluation of project size and complexity. A reasonable guideline as to size of 6.111 projects is that it not require more than a kit and a proto board per person.

6.111 student projects often become too large because of a desire to effect computations in parallel and at high speed. Data paths are often unnecessarily wide and redundant. It is generally far better to minimize the type and extent of the data paths even though this results in more complicated control circuitry.

FSMs implemented with PALs and FPGAs allow implementation of complicated control. Please remember that massive data paths that enable computation at speeds far faster than needed do not represent a good design! It is almost always better to spend more time thinking and less time wiring.