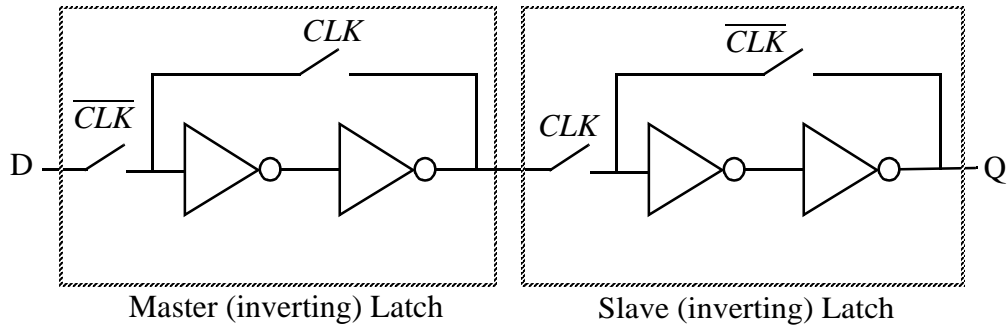


6.111 Spring 2004
In-class Exercise #1

Student Name:

TA:

Consider the following implementation of a register. Assume that an inverter has a delay of 1 and that the switch is ideal.



(a) What type of register is shown above (positive edge-triggered or negative edge-triggered)?

(b) What is the setup time (t_{su}), hold time (t_{hold}), and propagation (t_{cq}) delay. Assume that CLK and \overline{CLK} are ideal (i.e., the delay to derive \overline{CLK} from CLK is zero).

(c) For each of the following memory elements, specify the critical edge from which the setup time and hold time are computed. For each element below, circle one edge.

- | | | |
|--------------------------------------|---------------------|---------------------|
| (1) positive edge-triggered register | positive clock edge | negative clock edge |
| (2) negative edge-triggered register | positive clock edge | negative clock edge |
| (3) positive latch | positive clock edge | negative clock edge |
| (4) negative latch | positive clock edge | negative clock edge |