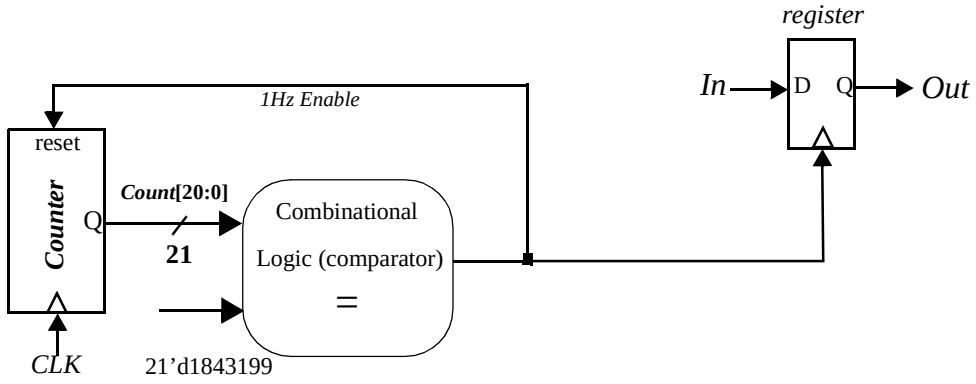
MIT 6.111 Spring 2004 - In-Class Exercise #2

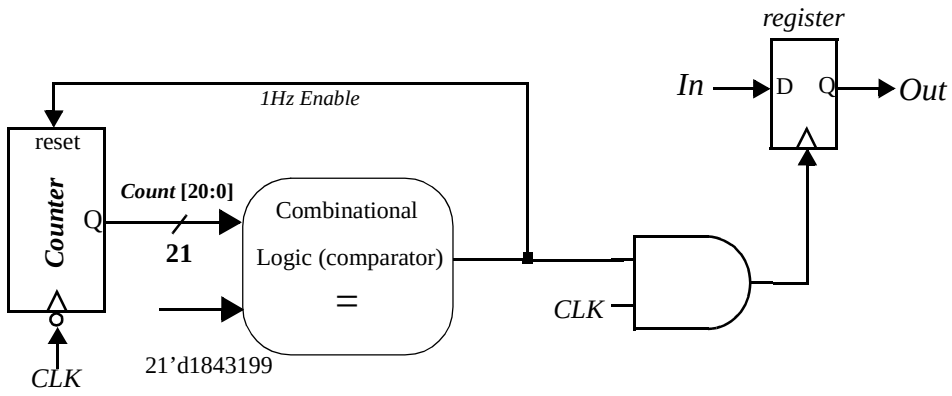
Name:

TA:

(a) Consider the one second clock from lab2. The 1Hz enable is derived from the circuit below (the clock is the 1.8432Mhz clock). Assume that a global reset signal puts the count to 0 (the circuit is not shown here). Suppose the 1Hz enable is used to clock other circuits that need to be updated once per second (e.g., the register shown below). Identify the main problem with this circuit.



(b) The following is a simple modification that is proposed to solve the problem of part (a). The counter is negative edge-triggered and the AND gate is introduced before the register clock. Assume that the AND gate is ideal (i.e., has zero delay). Does this circuit fix the problem of part (a)? If so, under what conditions does this circuit function properly? If not, explain why.



(c) The solution of (b) is not a synchronous one (i.e., a single global clock to every register). Propose a fix to the problem in part (a) using a single clock (CLK). That is, both the counter and register are clocked from the same clock (CLK). You may add additional components in the diagram below.