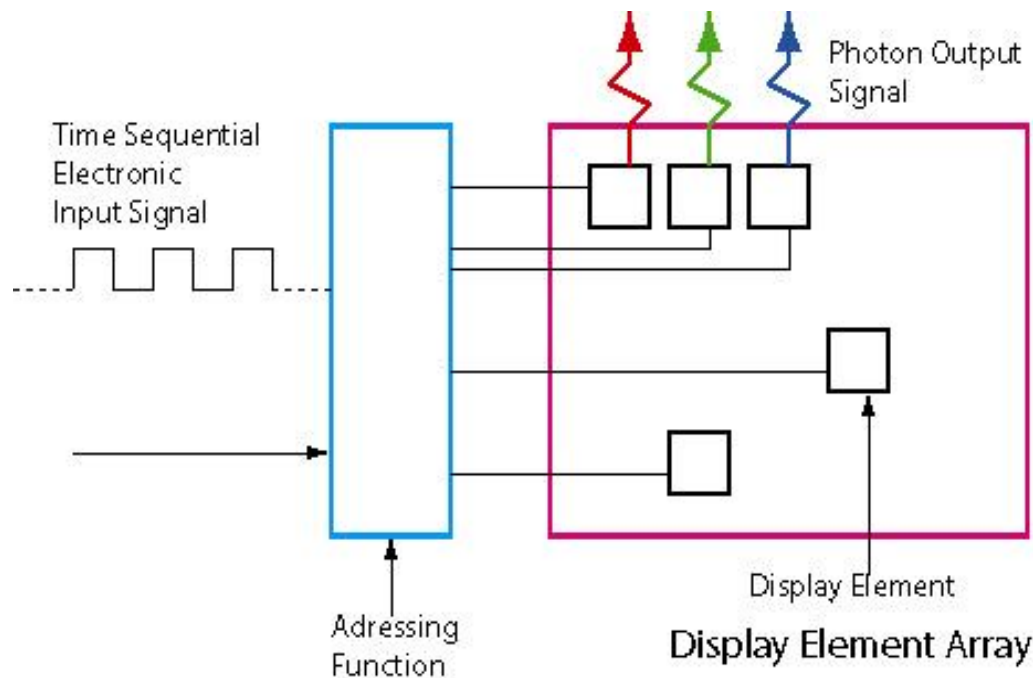# L13 - Video

Slides 2-10 courtesy of Tayo Akinwande
   Take the graduate course, 6.973 – consult Prof. Akinwande
Some modifications of these slides by D. E. Troxel

How Do Displays Work?

- **Electronic display is a "Language Translator" that converts "Time Sequential Electrical Signals" into spatially and temporally configured light signal (images) useful to the viewer.**

- **Translation Function carried out by two intertwined sub-functions**
  - **Display element address wherein electrical signals are appropriately routed to the various display elements (similar to memory addressing)**
  - **Display element (pixel) converts the routed electrical signal at its input into light of certain wavelength and intensity (inverse of image capture)**

Emissive Displays

Emissive Displays **generate photons from electrical excitation of the picture element (pixels).**

- ☐ **Can generate energy by**
  - ● **UV absorbed by a phosphor**
  - ● **injection by a PN junction**
  - ● **Electron Beam hitting a phosphor**

- ☐ **This energy causes excitation followed by excitation relaxation.**
  - ● **Hole & Electron recombination**
  - ● **Exiton formation and annihilation**
  - ● **Relaxation of excited ions or radicals in a plasma**

- ☐ **Sometimes the energy first goes to a dopant and then to photons, especially when changing the wavelength of the emitted light.**

- ☐ **Examples of Emissive Flat Panel Displays**
  - ● **Electroluminescence (Light Emitting Diode),**
  - ● **Cathodoluminescence (Cathode Ray Tube)**
  - ● **Photoluminescence (PLasma Displays)**

Light Valve Displays

Light Valve Displays **spatially and temporally modulate the intensity pattern of the picture elements (pixels)**

- **Displays that "spatially and temporally" modulate ambient lighting or a broad source of lighting and redirect it to the eye.**
  - □ **The display element changes the intensity of the light using**
    - ● **Refraction**
    - ● **Reflection**
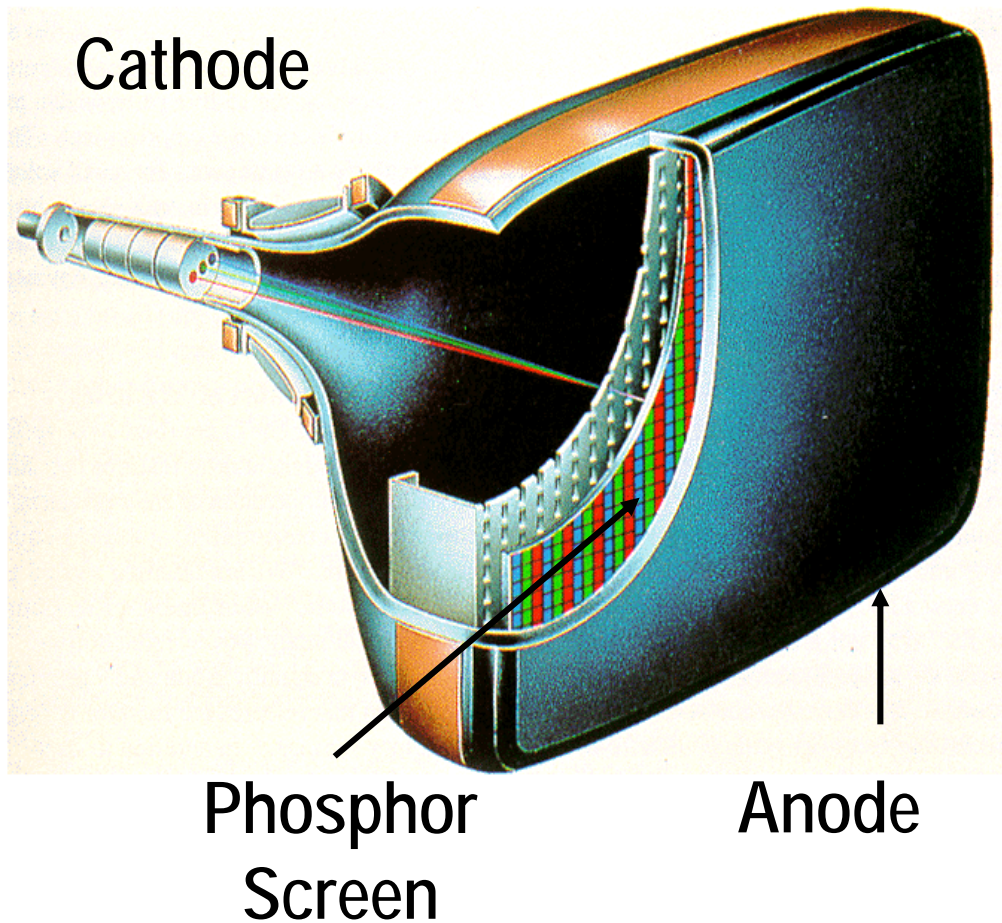   - ● **Polarization change**

- **Examples of Light Valve Displays**
  - □ **Liquid Crystal Displays (active & passive matrix)**
  - □ **Deformable Mirror Displays**
  - □ **Membrane Mirror Displays**
  - □ **Electrophoretic Displays (E-Ink)**

Cathode Ray Tube

CRT Display

Cathode

Phosphor Screen

Anode

Courtesy of PixTech

Displays in the lab available for projects are CRT displays.

An electron beam "boiled off a metal" by heat (**thermionic emission**) is sequentially scanned across a phosphor screen by magnetic deflection. The electrons are accelerated to the screen acquiring energy and generate light on reaching the screen (**cathodoluminescence**)

Flat Panel Displays

- **Time sequential electrical signals describing an image need to be routed to the appropriate picture element (pixel).**

- **Typical flat panel displays are two-dimensional arrays of picture elements (pixels) that are individually addressed from the perimeter or the back. Methods of scanning include**
  - ☐ **Sequential addressing (CRT)**
  - ☐ **Row scan addressing (Thin-CRT, Plasma, Mirror, LCD)**

- **Row scanning of a matrix of pixels requires picture elements with non-linear Luminance – Voltage (L-V) characteristics.**
  - ☐ **If the L-V characteristics is linear (or is not non-linear enough), a non linear switch element is required in series with the pixel.**

Thin-CRT

Cathode

One Pixel

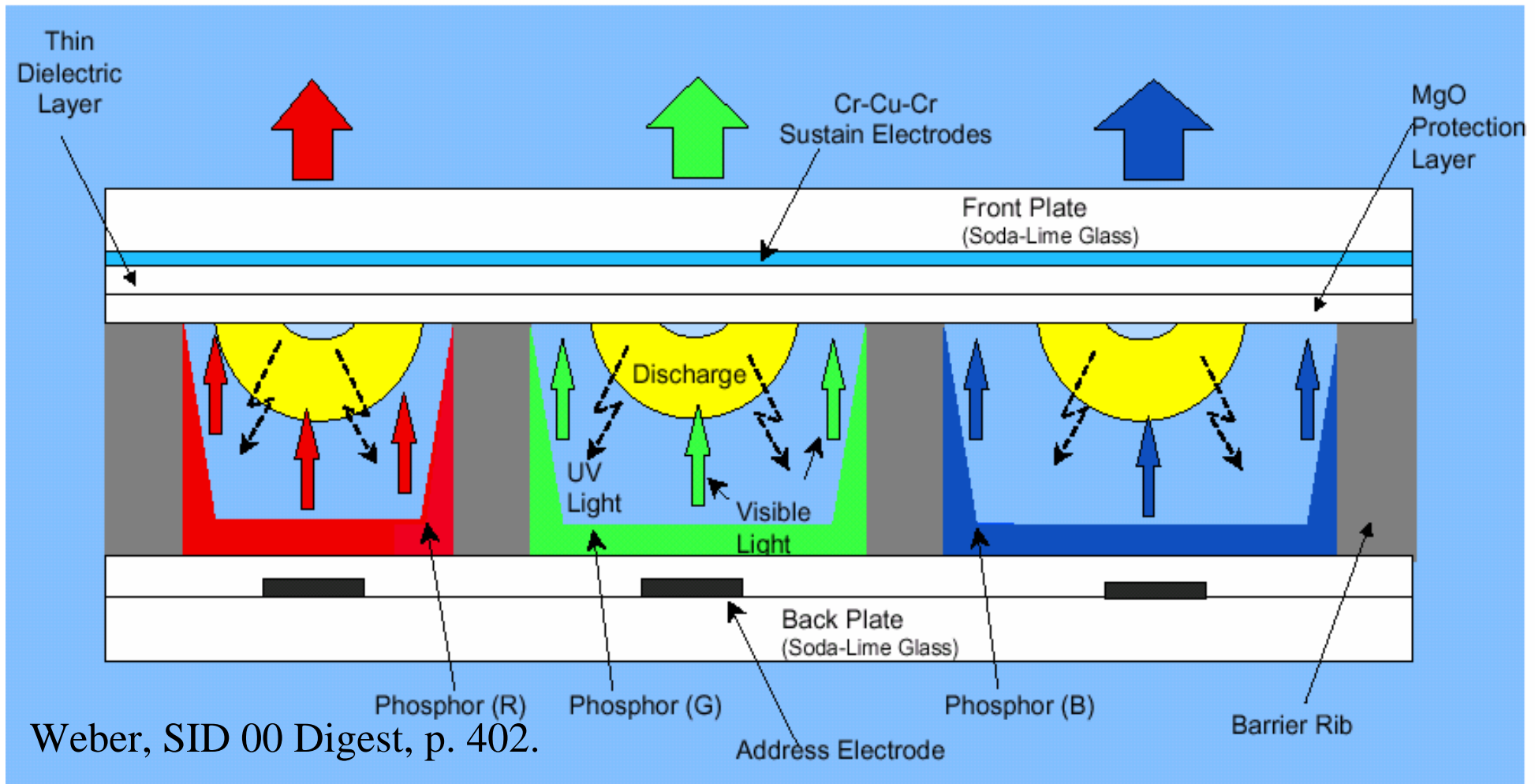Field Emission Device (FED) Display

Phosphors

Anode
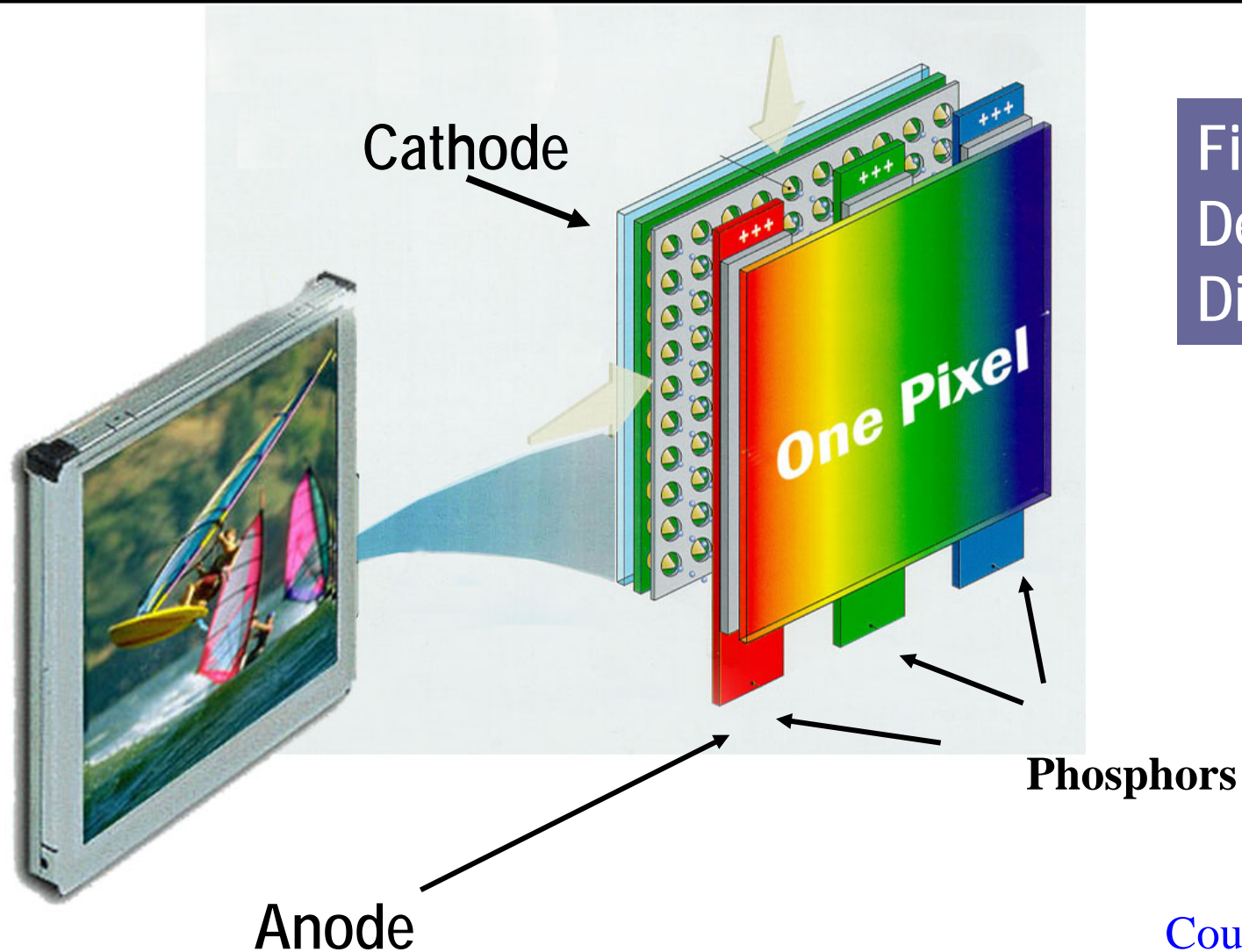
Courtesy of PixTech

In principle similar to the CRT except that it uses a **two-dimensional array of electron sources (field emission arrays)** which are matrix addressed allowing the vacuum package to be thin

Thin Dielectric Layer

Cr-Cu-Cr Sustain Electrodes

MgO Protection Layer

Front Plate (Soda-Lime Glass)

Discharge

UV Light

Visible Light

Phosphor (R)   Phosphor (G)   Phosphor (B)

Back Plate (Soda-Lime Glass)

Address Electrode

Barrier Rib

Weber, SID 00 Digest, p. 402.

- **Electrons are accelerated by voltage and collide with gasses resulting in ionization and energy transfer.**
- **Excited ions or radicals relax to give UV photons.**
- **UV photons cause hole-electron generation in phosphor and visible light emission.**
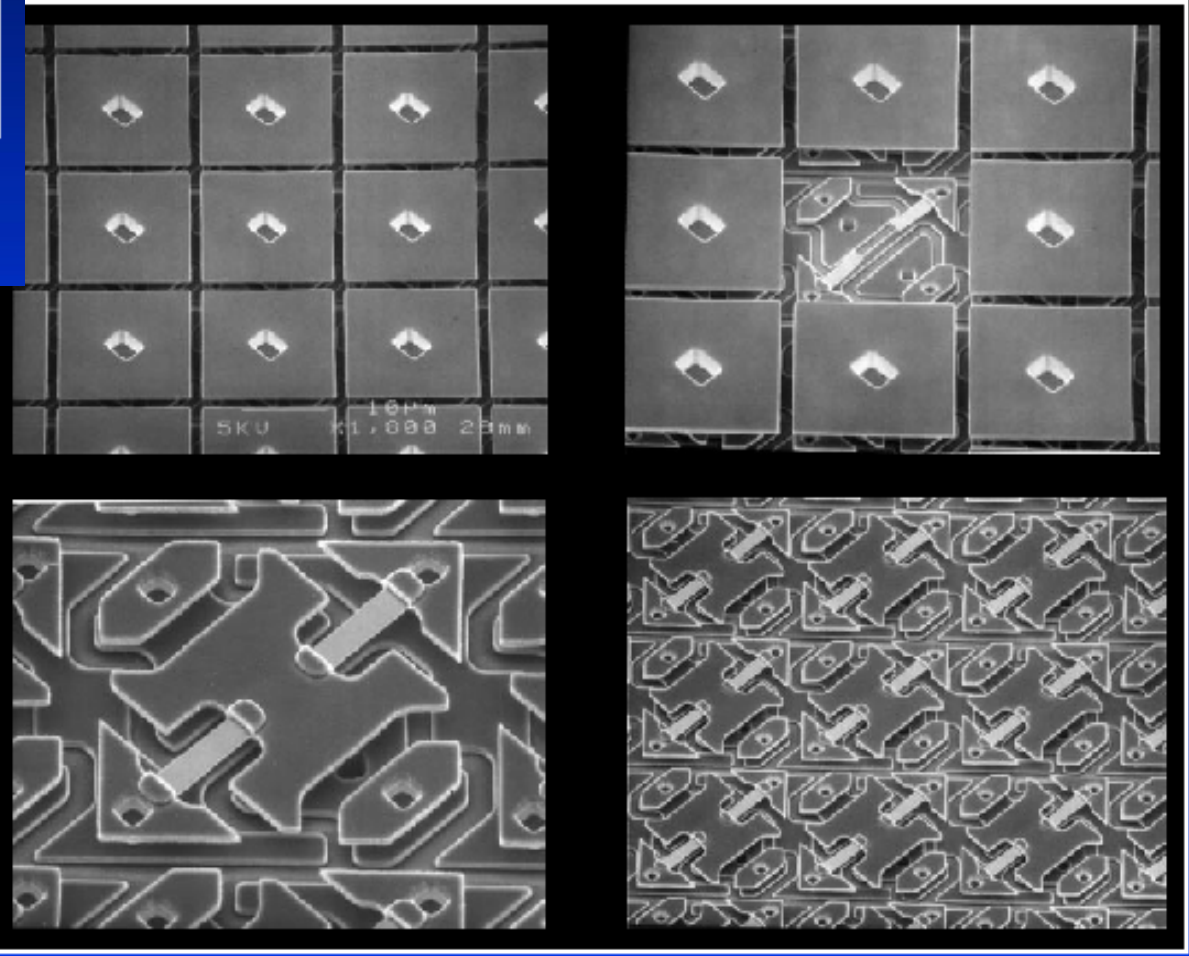
Digital Mirror Device
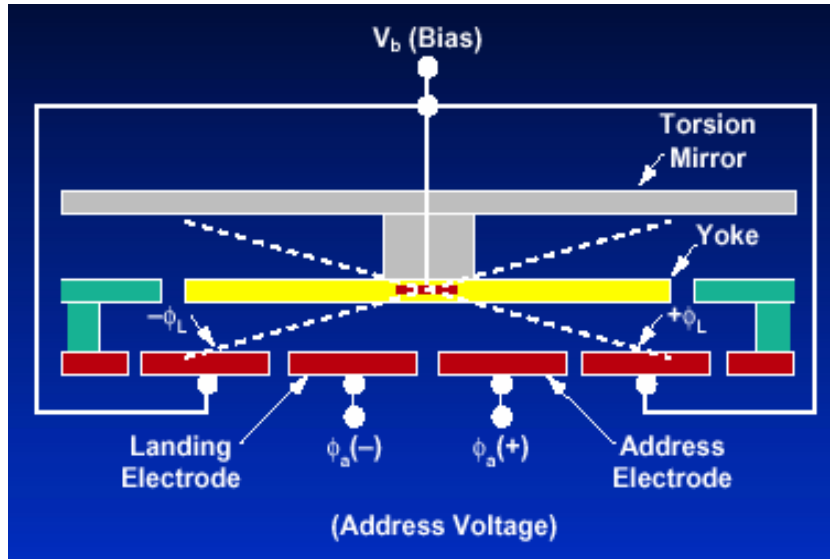
Courtesy of Texas Instruments

Applied voltage deflects
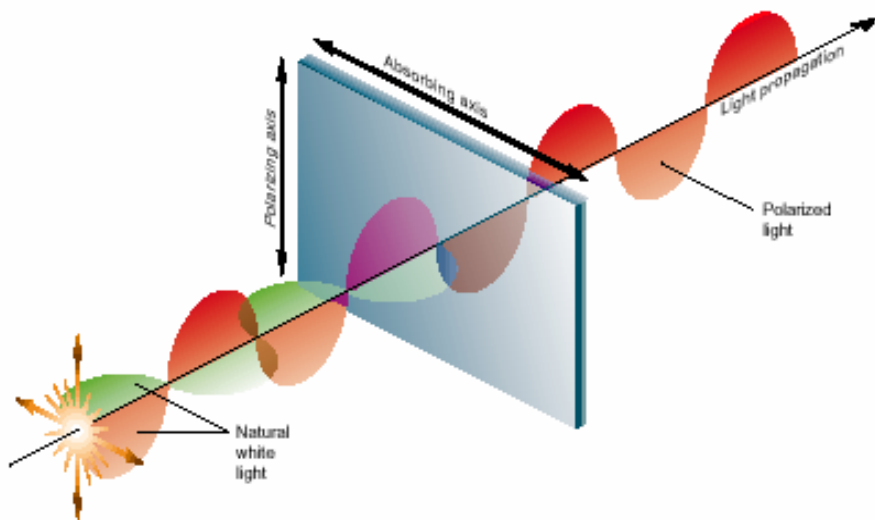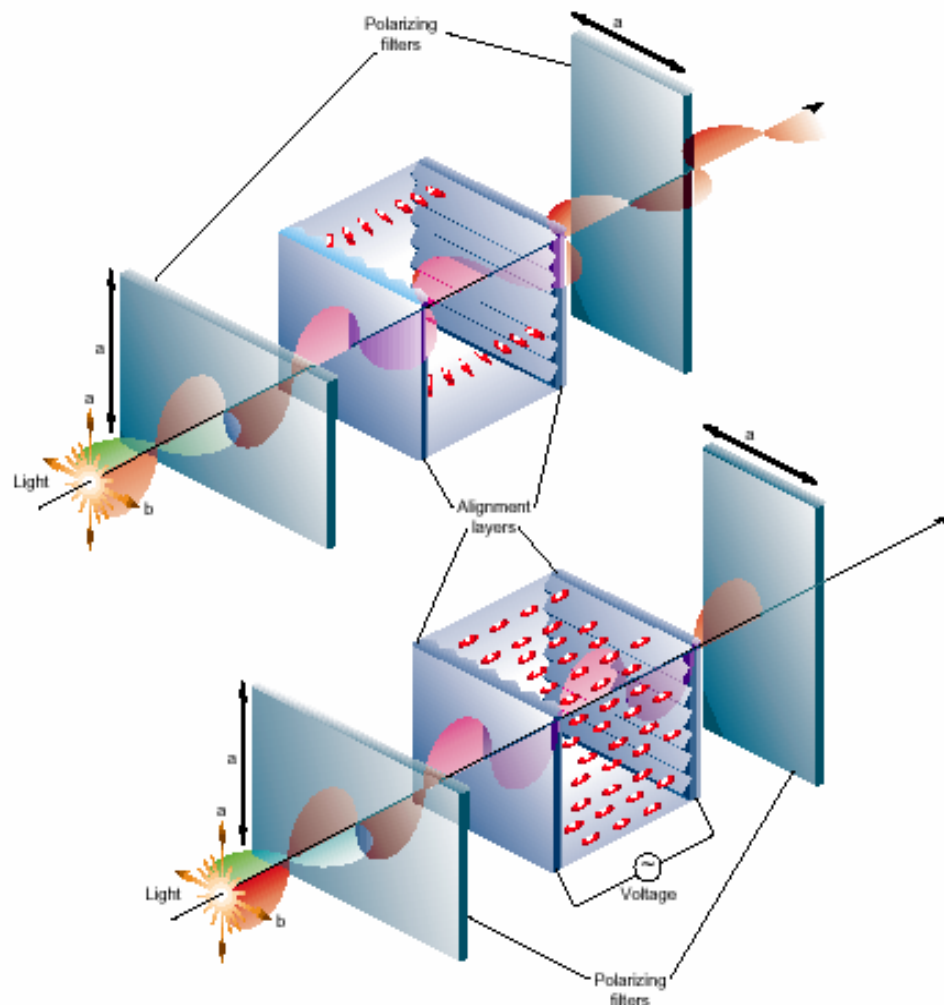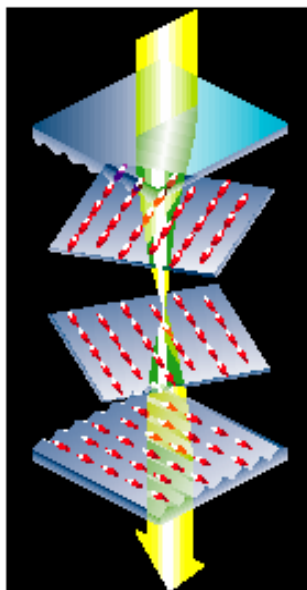Mirror and hence direct light

Liquid Crystal Displays

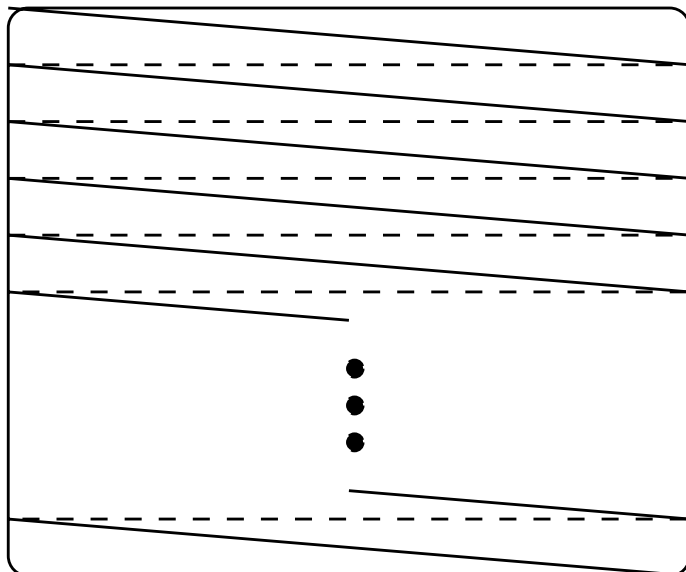Liquid Crystals rotate the plane of polarization of light when a voltage is applied across the cell
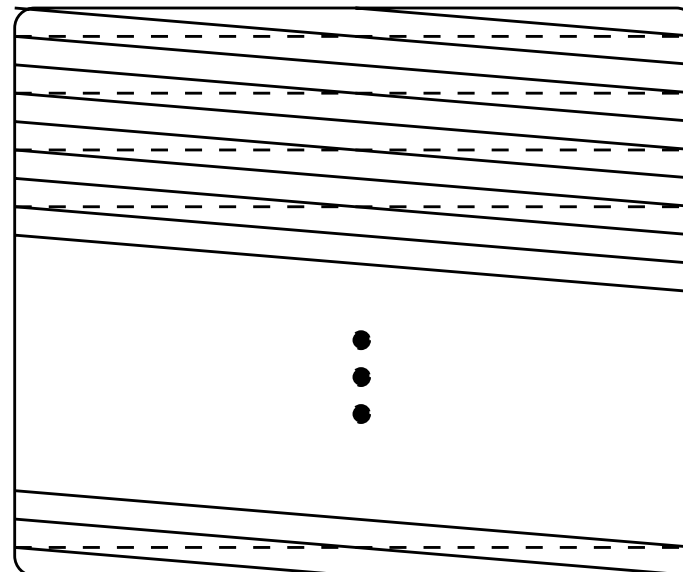

Courtesy of Silicon Graphics

- **Television and most computer displays use raster scan.**

Non−Interlaced: Frame rate may be 60, 72, etc. frames/sec.

————— Scan line

- - - - - - - Retrace line

Interlaced: Frames alternate. This is like television: 60 half frames/sec.

Electron beam "scans" tube. Beam location is shown here. Beam current determines brightness of display.

- **The 'frame' is a single picture (snapshot).**
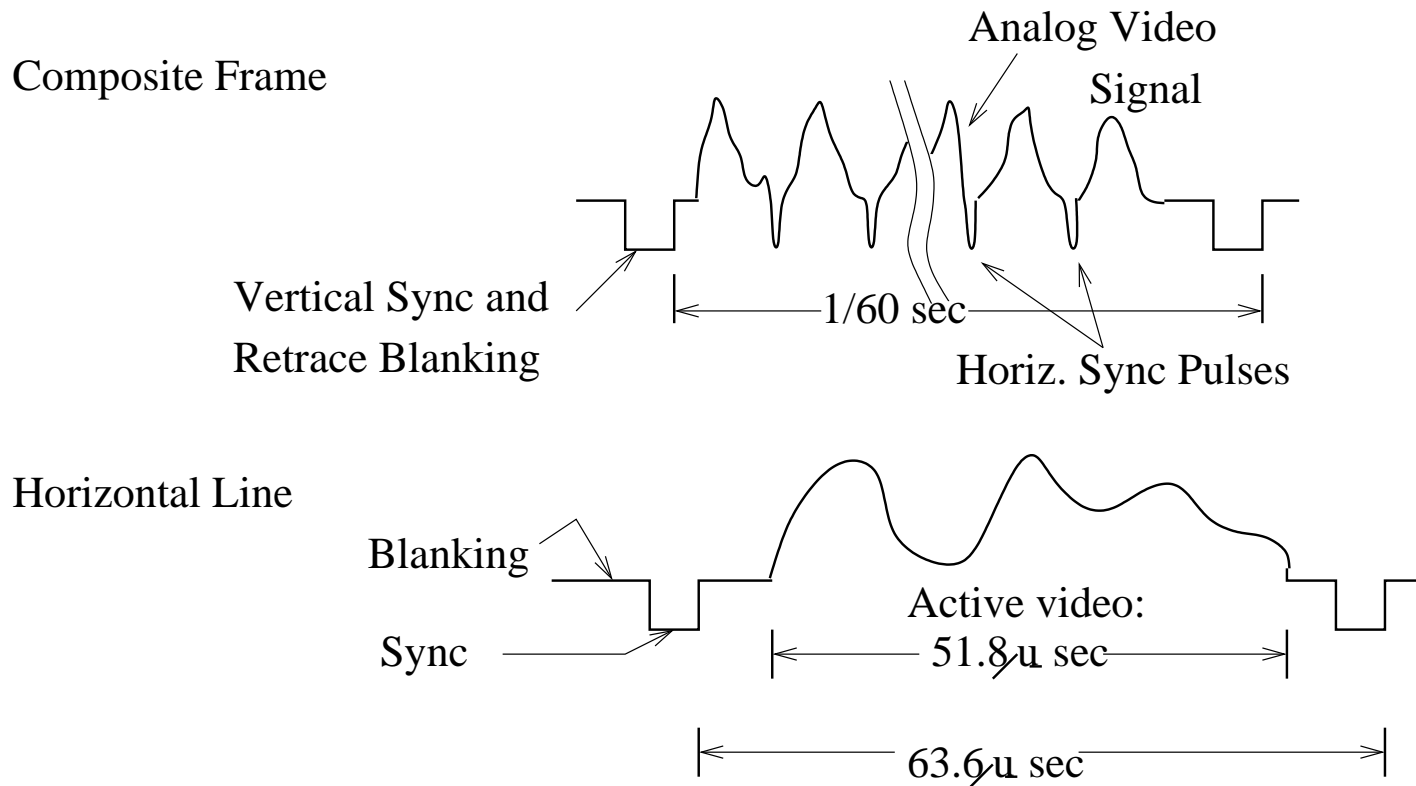 - ☐ **It is made up of many lines.**
  - ☐ **Each frame has a synchronizing pulse (vertical sync).**
  - ☐ **Each line has a synchronizing pulse (horizontal sync).**
  - ☐ **Brightness is represented by a positive voltage.**
  - ☐ **Horizontal and Vertical intervals both have blanking so that retraces are not seen (invisible).**
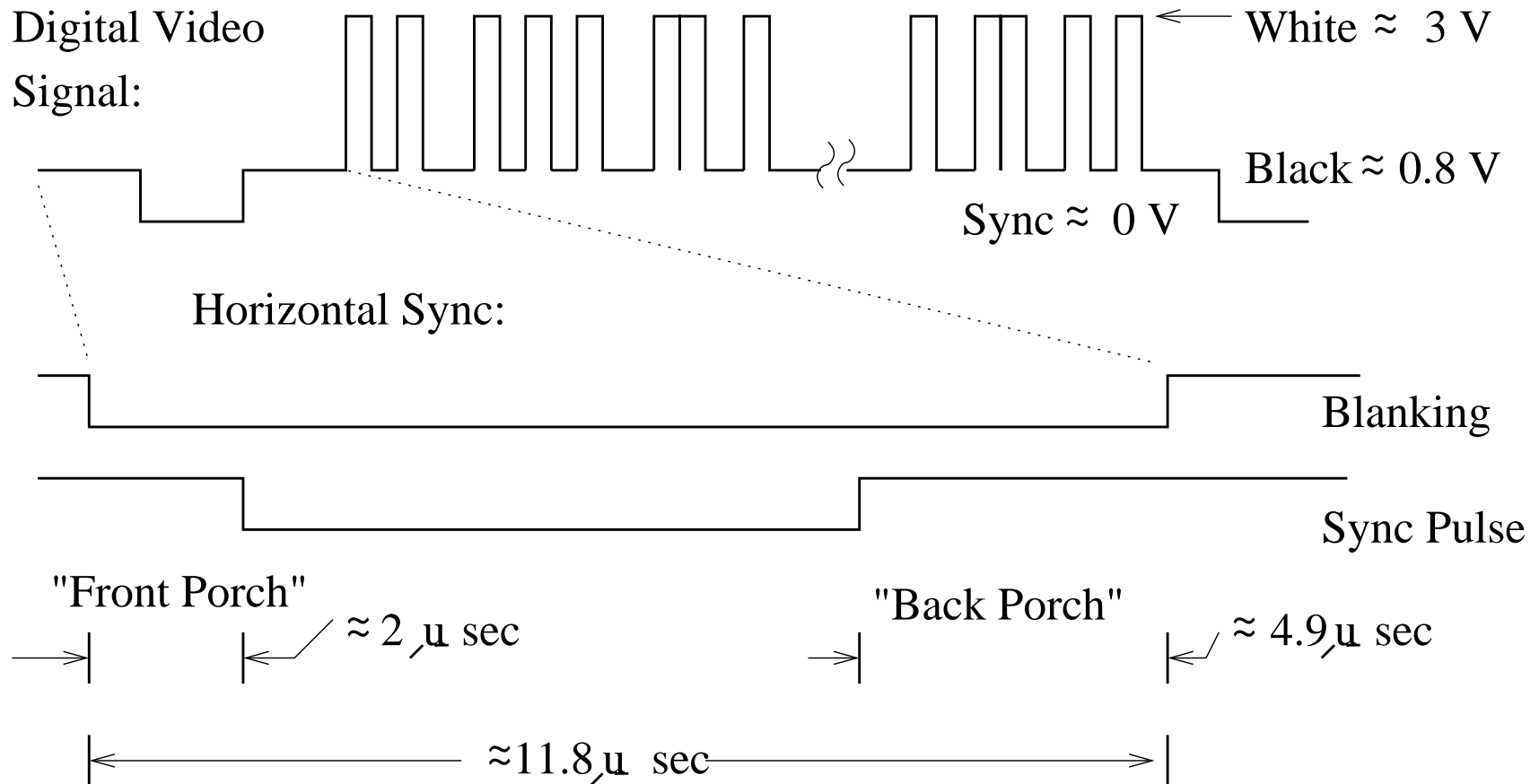

Composite Frame

Analog Video Signal

Vertical Sync and Retrace Blanking

1/60 sec

Horiz. Sync Pulses

Horizontal Line

Blanking

Sync

Active video: 51.8 u sec

63.6 u sec

Horizontal Synchronization

- **The picture consists of white dots on a black screen.**
  - **White is the highest voltage.**
  - **Black is a low voltage.**
  - **Sync is below the black voltage.**

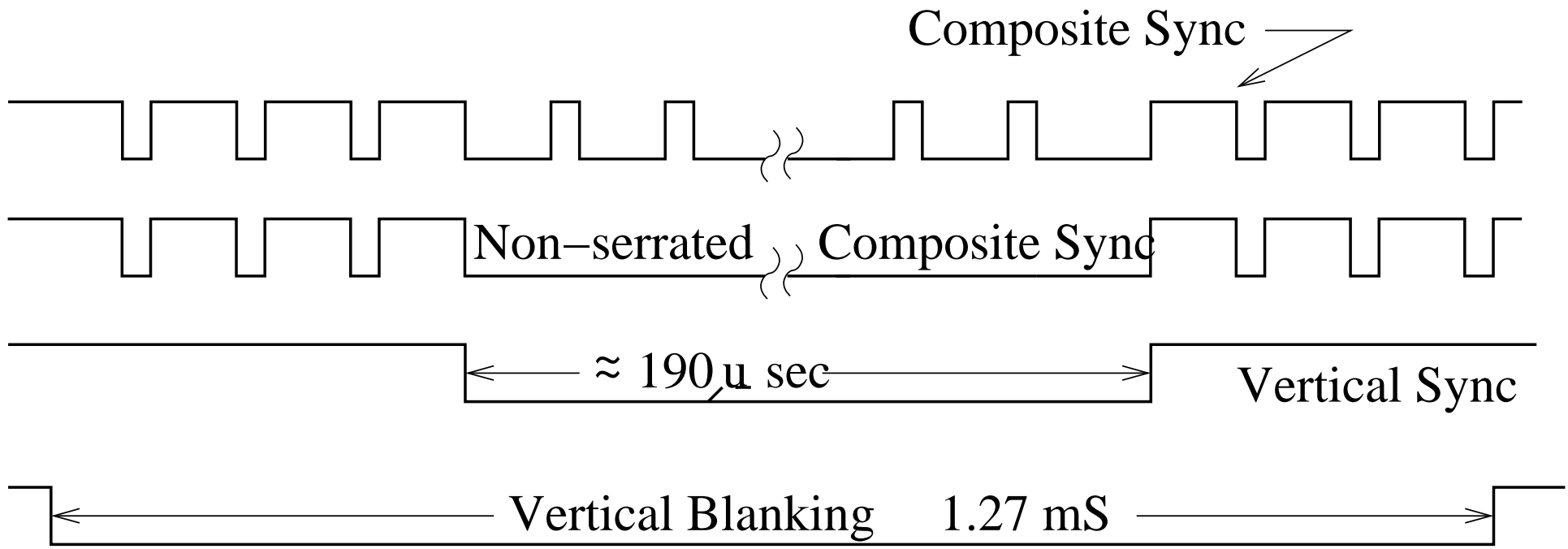- **Sync pulses are surrounded by the blanking interval so one doesn't see the retrace.**

Digital Video Signal:

White ≈ 3 V

Black ≈ 0.8 V

Sync ≈ 0 V

Horizontal Sync:

Blanking

Sync Pulse

"Front Porch" ≈ 2 μ sec

"Back Porch" ≈ 4.9 μ sec

≈11.8 μ sec

Composite Synchronization

- **Horizontal sync coordinates lines.**

- **Vertical sync coordinates frames.**

- **They are similar except for the time scales and they are superimposed on each other. The numbers are for TV-like displays.**
  - **What purpose is there for serrated sync?**

Composite Sync

Non–serrated Composite Sync

$\approx 190 \, \mu$ sec

Vertical Sync

Vertical Blanking   1.27 mS

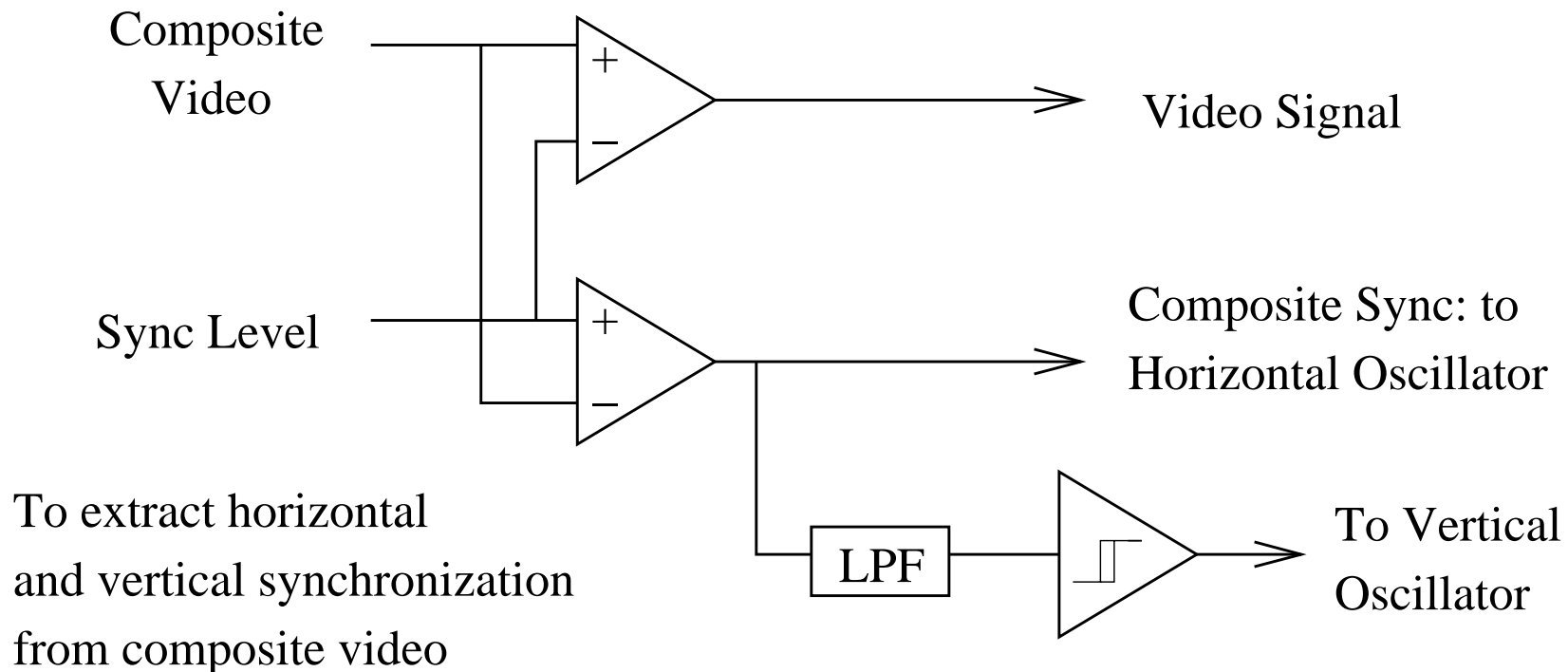# (Conceptual) Recovery of Signals

- **Composite video has picture data and both syncs.**
  - ☐ **Picture data (video) is above the sync level.**
  - ☐ **Simple comparators extract video and composite sync.**

- **Composite sync is fed directly to the horizontal oscillator.**

- **A low-pass filter is used to separate the vertical sync.**
  - ☐ **The edges of the low-passed vertical sync are squared up by a Schmidt trigger.**

Composite
Video

Video Signal

Sync Level

Composite Sync: to
Horizontal Oscillator

To extract horizontal
and vertical synchronization
from composite video

LPF

To Vertical
Oscillator

Sync Separator

- **A sync separator is used to recover sync from a composite video signal.**
    - GS4981 generates composite sync from video.
        - It also generates separated sync signals.

- **The sync separator is not easy to implement in an HDL as its input is an analog signal.**

- **However, your pixel clock must be synchronized with the recovered horizontal sync.**
    - If you do this synchronization with the pixel clock signal directly, then the pixel clock used will "crawl" a whole pixel time.
    - It is better to use a faster clock, say 4 times faster, to do the synchronization and then the "crawl" will only be ¼ of a pixel time (distance).

**From Camera** → **GS4981** →
- **Composite Sync**
- **Vertical Sync**
- **Horizontal Sync**
- **Back Porch**
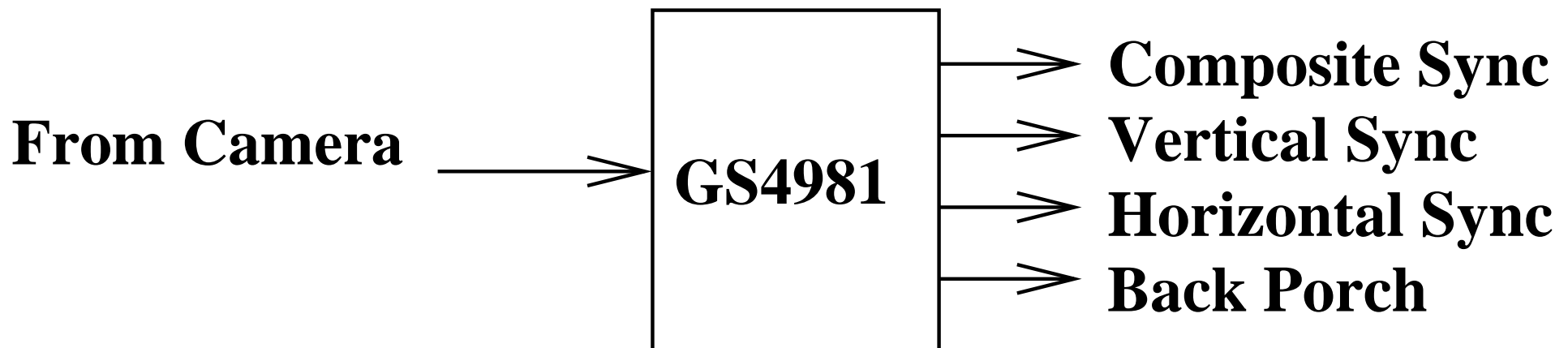
- **Assume one bit per pixel and provide for reverse video.**

- **This is a simple 'D/A' to generate monochrome composite video.**
  - **The 'S38 is an open collector part so the voltages are determined by the resistor network. The output resistance is ~ 75 ohms.**
  - **What signals should be glitch free?**
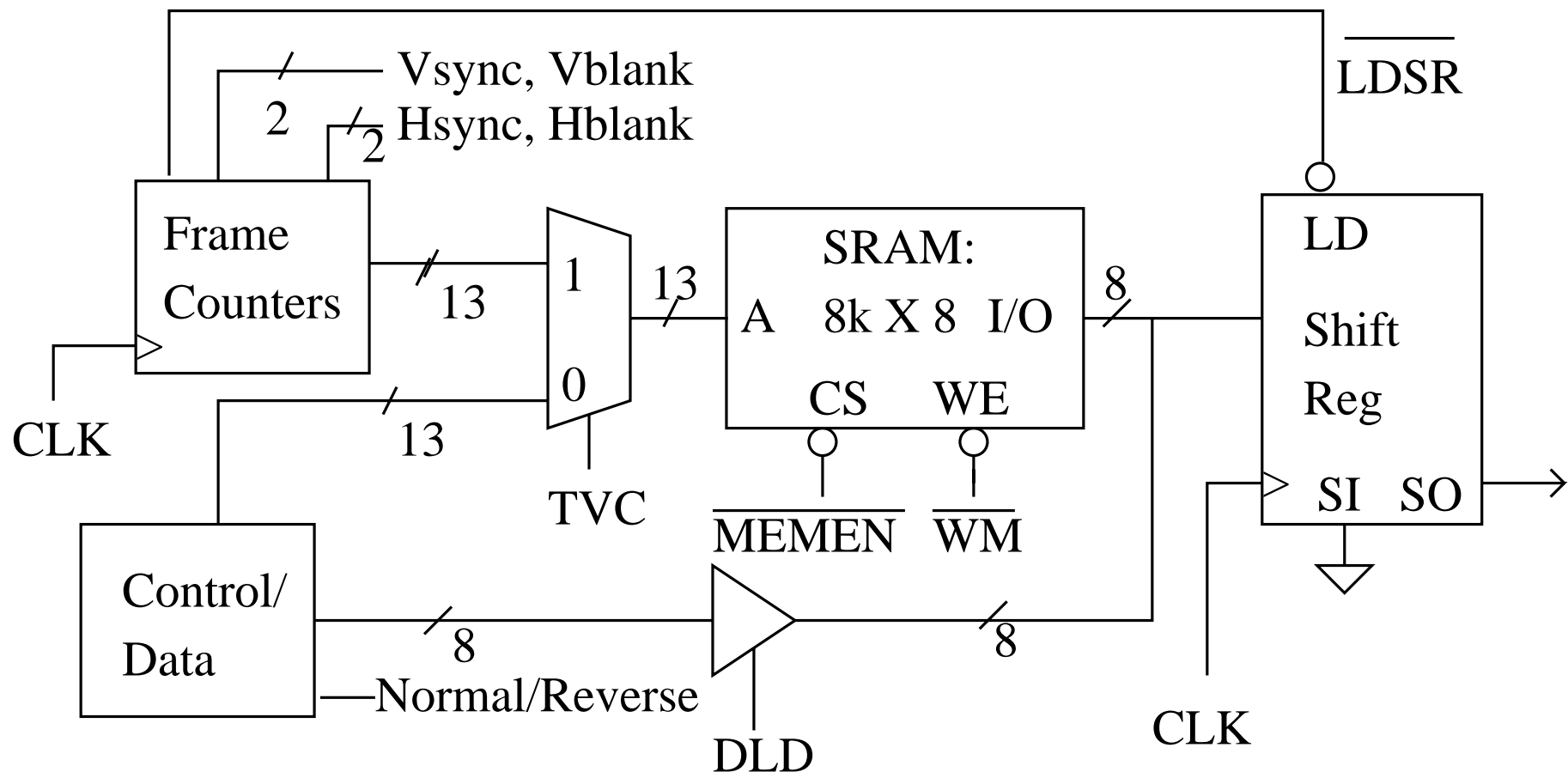 - **Vblank, Hblank, Vsync, Hsync, /LDSR, Normal/Reverse**
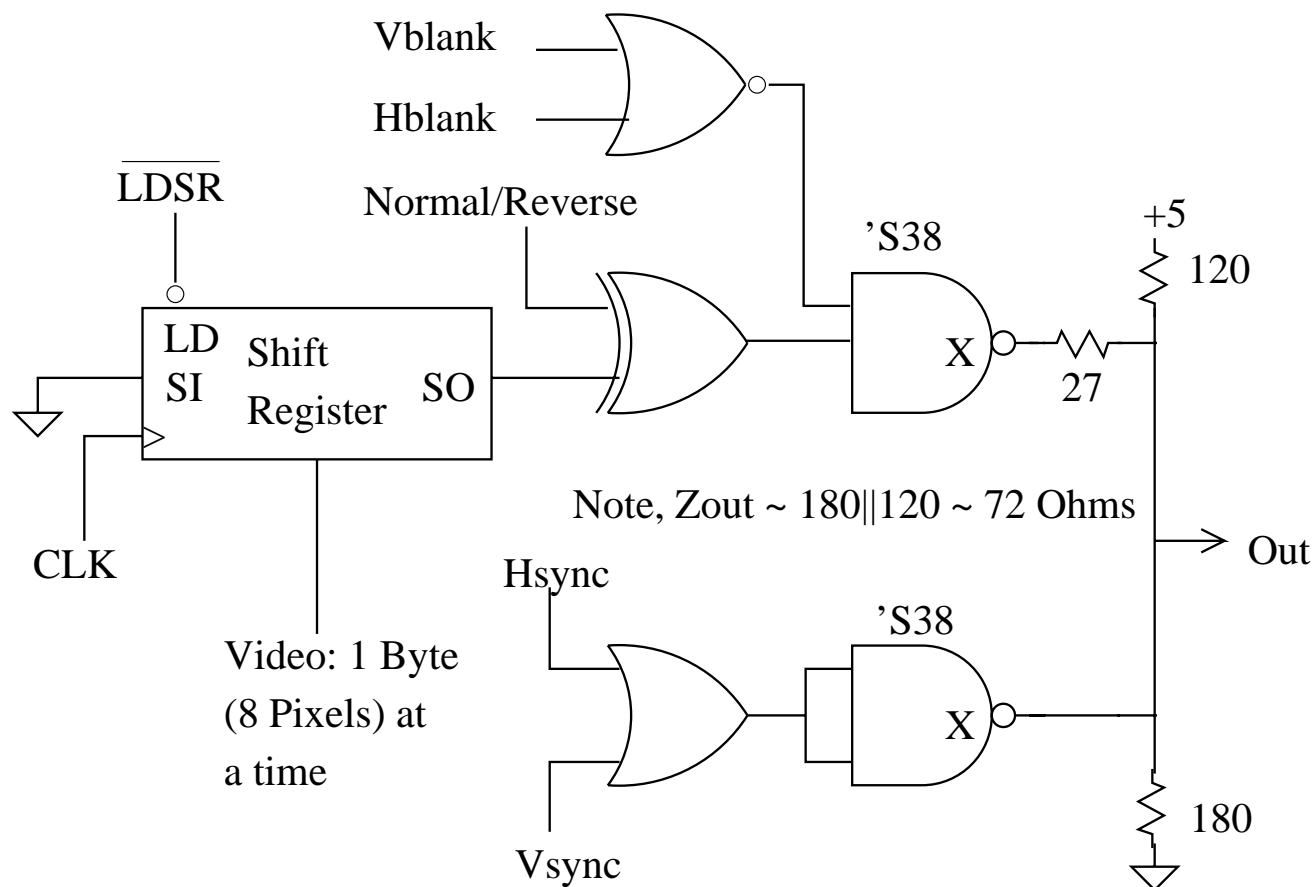
Store bit-mapped video in a RAM with pixels packed into bytes.
Half the time, the video subsystem accesses the data to drive the TV monitor.
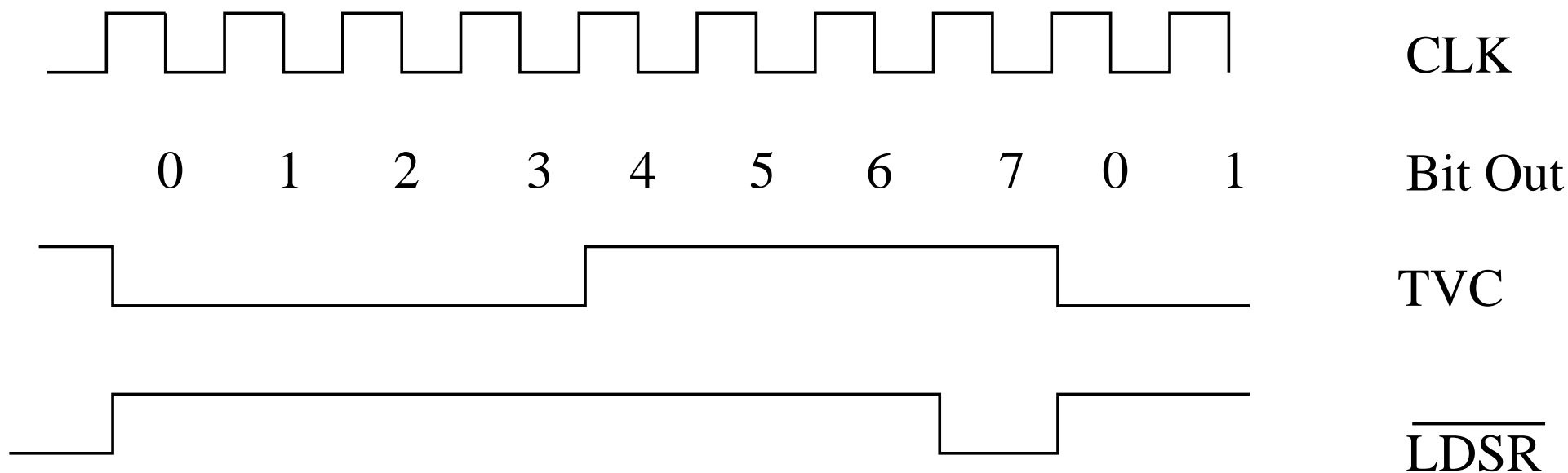**Half the time, the project can modify (update) the bits in the RAM.**

Timing of Control Signals

- **Data is loaded into a shift register and shifted out to generate the video signal.**
  - CLK is at the pixel rate.
  - TVC divides access to the SRAM giving half the time to get data to load into the shift register .
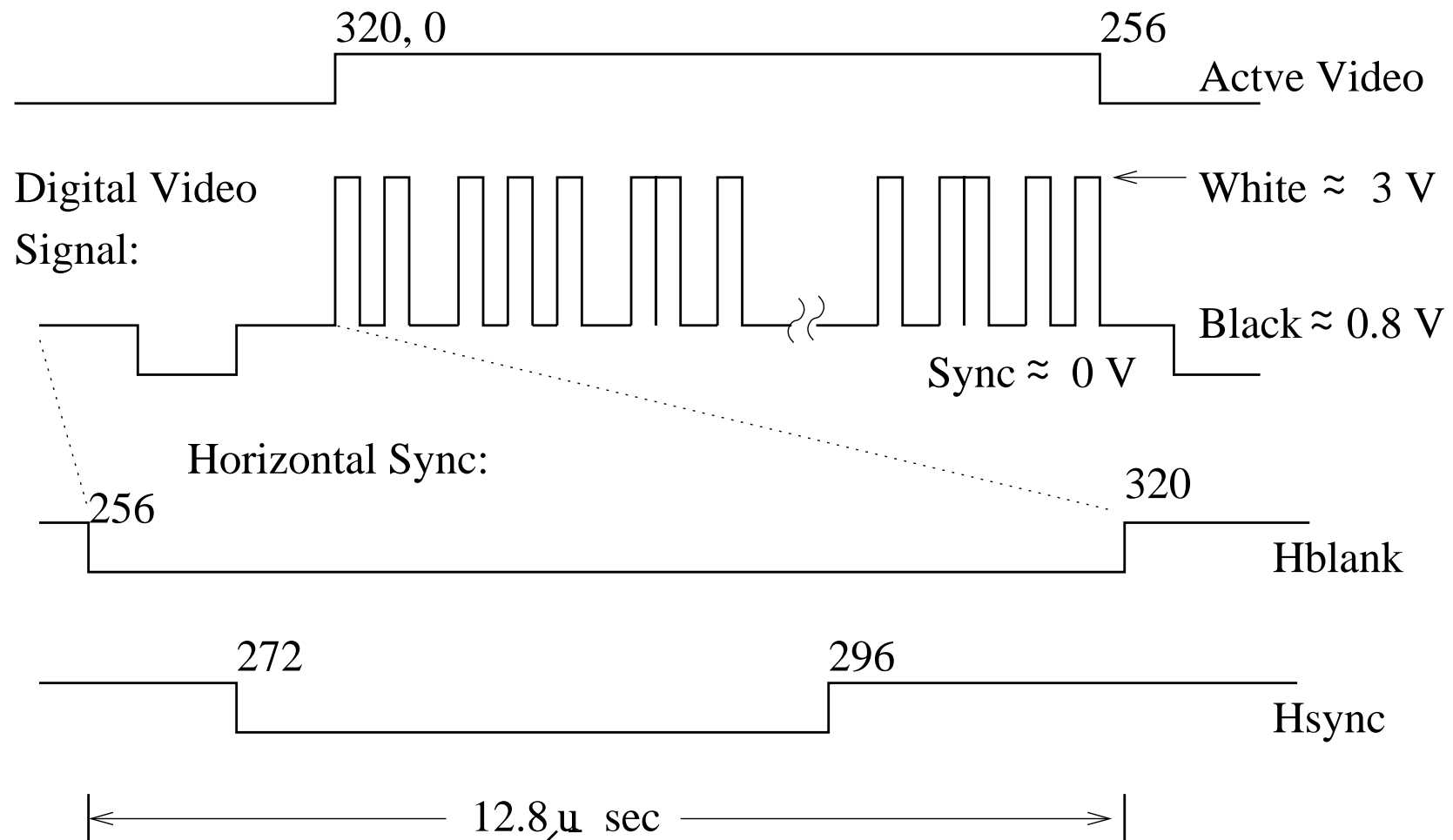

CLK

Bit Out   0   1   2   3   4   5   6   7   0   1

TVC

$\overline{LDSR}$

System Access to SRAM

Horizontal Sync Timing

- **We choose this display format.**
  - ☐ **256 pixels X 192 rows**
  - ☐ **10 MHz clock => 200 nanoseconds per pixel**
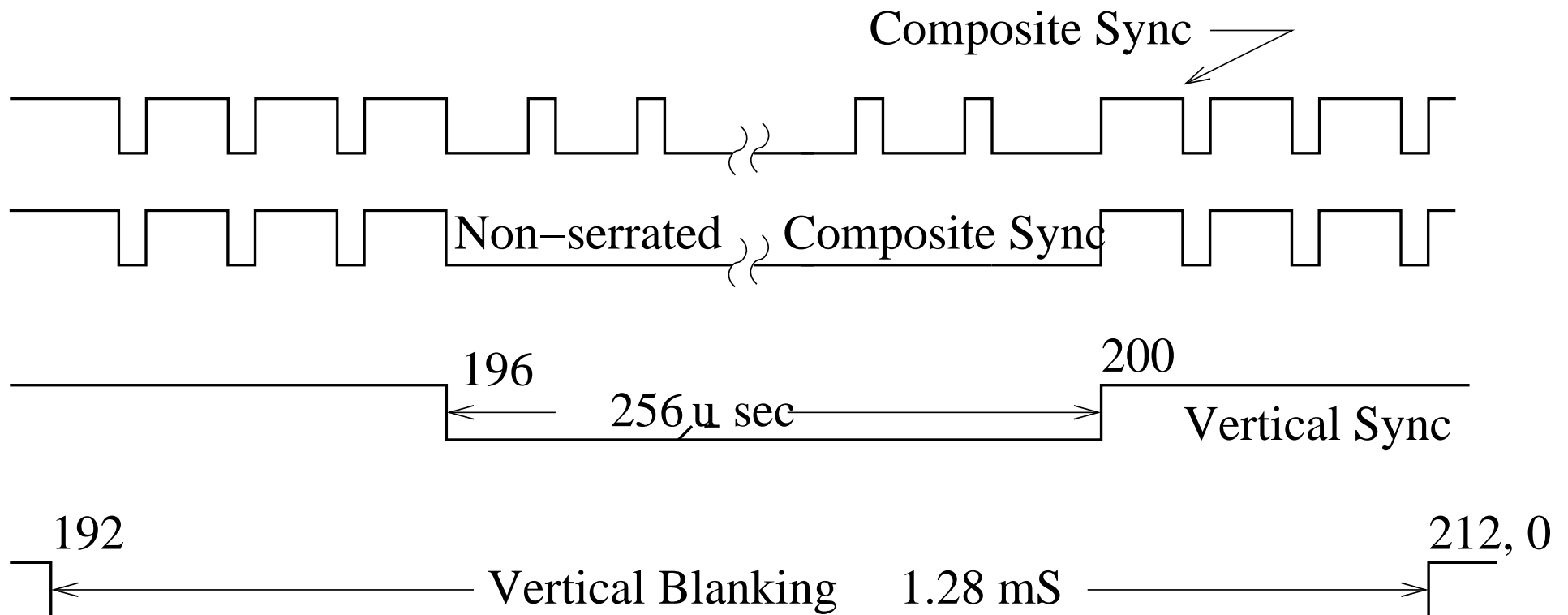 - ☐ **256 X 192 = 49,152 = 48K pixels = 6 K bytes**
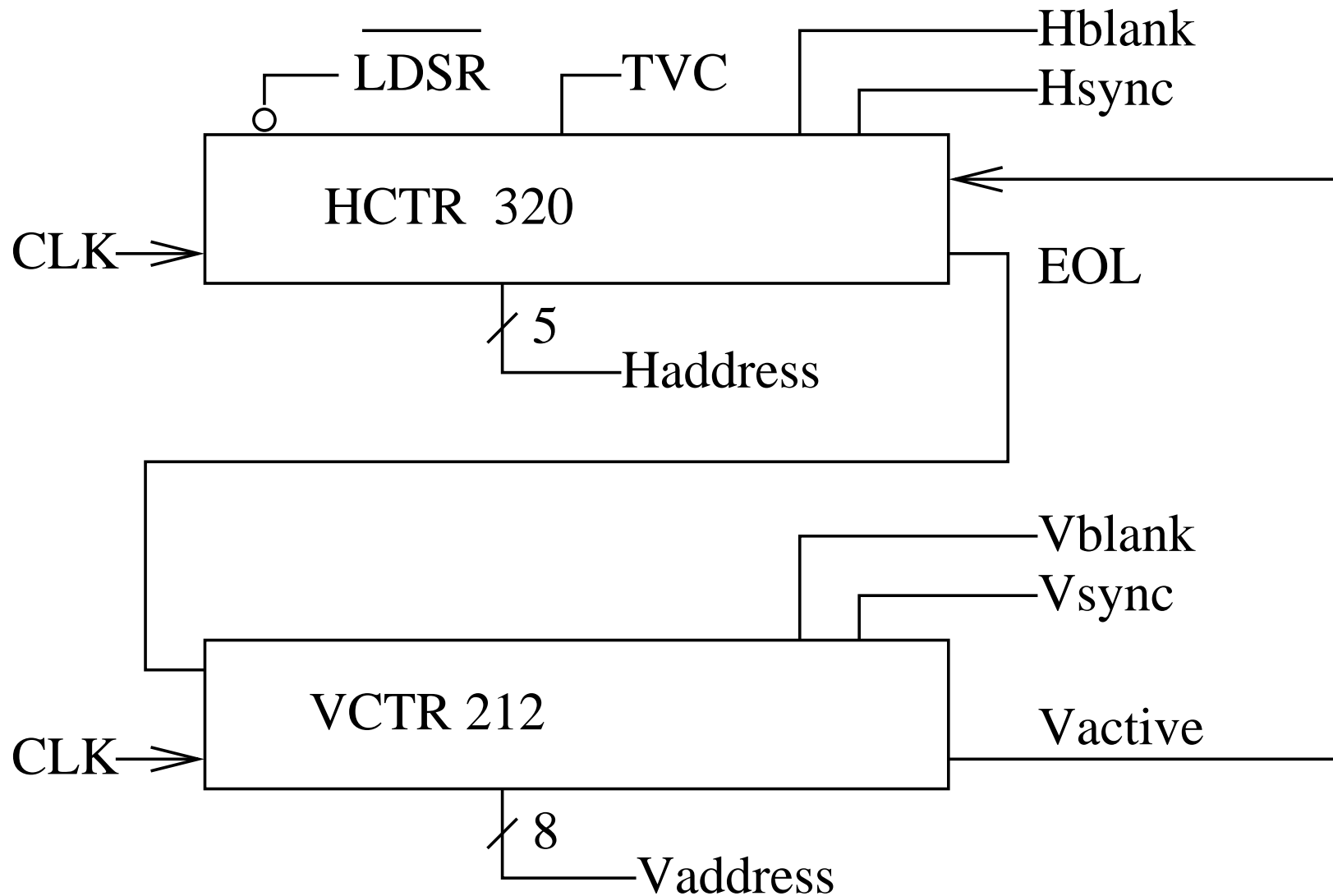
Vertical Sync Timing

- **Our display format.**
  - **256 pixels X 192 rows**
  - **10 MHz clock => 200 nanoseconds per pixel**
  - **256 X 192 = 49,152 = 48K pixels = 6 K bytes**

Composite Sync

Non−serrated Composite Sync

196   200

256 μ sec

Vertical Sync

192   212, 0

Vertical Blanking   1.28 mS

- **What signals need to be glitch free?**

hctr.v

```
/*********************************
* Filename:   hctr.v           *
* Description: Horizontal counter   *
* Author:     Don Troxel        *
* Date:       3/13/2004         *
* Course:     6.111            *
*********************************/

module hctr (clk, vactive, reset,
          hcnt, n_srld, tvc, hblank, hsync, eol);

   input clk, vactive, reset;
   output n_srld, tvc, hblank, hsync, eol;
   output [8:0] hcnt;

   wire n_srld, tvc, eol, hactive;
   reg hblank, hsync;
   reg [8:0] hcnt;


//   parameter start = 9'd224;
   parameter start = 9'd000;

   assign n_srld = !(hcnt[0] & hcnt[1] & tvc);
   assign tvc = hcnt[2] & hactive & vactive;
   assign eol = (hcnt == 9'b100111111) ? 1'b1 : 1'b0;
   assign hactive = (hcnt < 9'b100000000) ? 1'b1 : 1'b0;
```
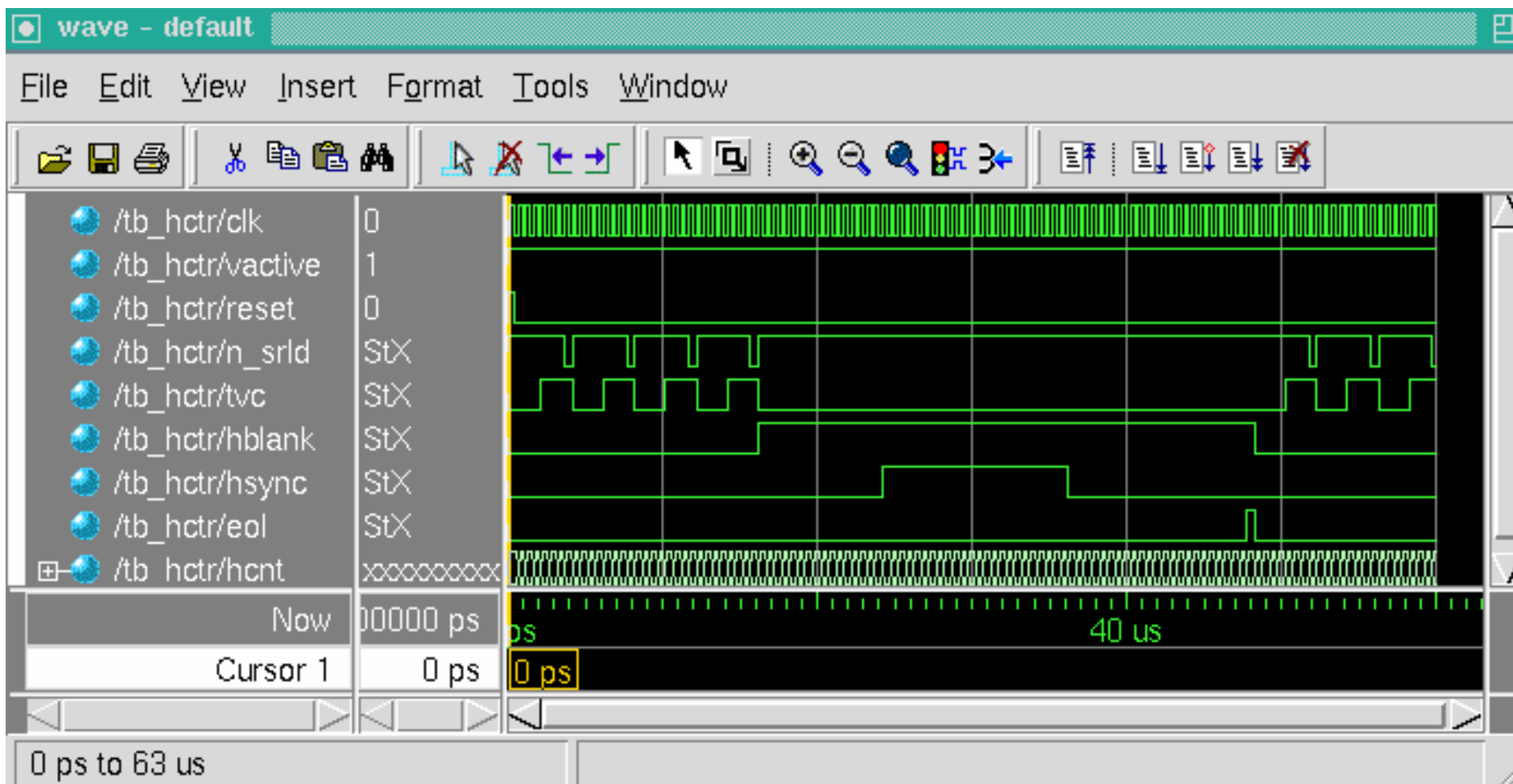
```
always @(posedge clk, posedge reset)
  begin
   if(reset == 1)
     begin
       hcnt <= start;
       hblank <= 1'b0;
       hsync <= 1'b0;
     end
   else if (hcnt == 9'd319)  // reset to 0
     begin
       hcnt <= start;
       hblank <= 1'b0;
     end
   else
     hcnt <= hcnt + 1;

   if (hcnt == 9'd255)
     hblank <= 1'b1;
   else if (hcnt == 9'd271)
     hsync <= 1'b1;
   else if (hcnt == 9'd295)
     hsync <= 1'b0;
  end

endmodule
```
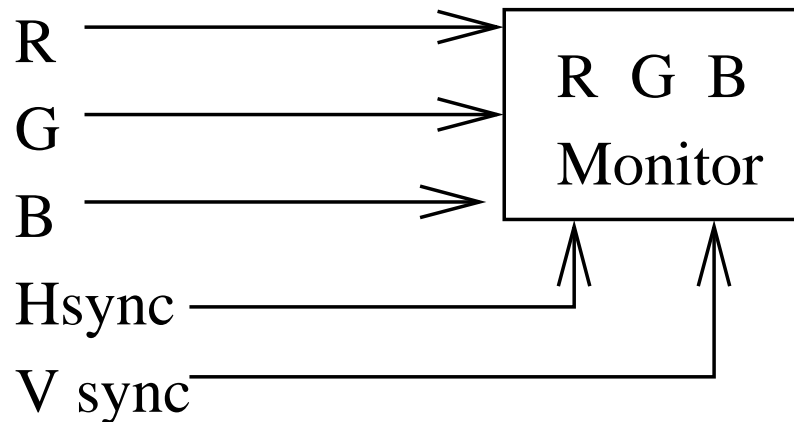
Simulation of hctr.v

- **Color displays are similar to three monochrome displays operated together, i.e., the colors add.**

- **Three binary signals yield an eight-color display.**
  - □ **Well, one of the colors is black!**
  - □ **Some monitors have an analog video input for each color.**

- **Sync is sometimes on a separate wire.**
  - □ **Sometimes it is superimposed on the green signal.**

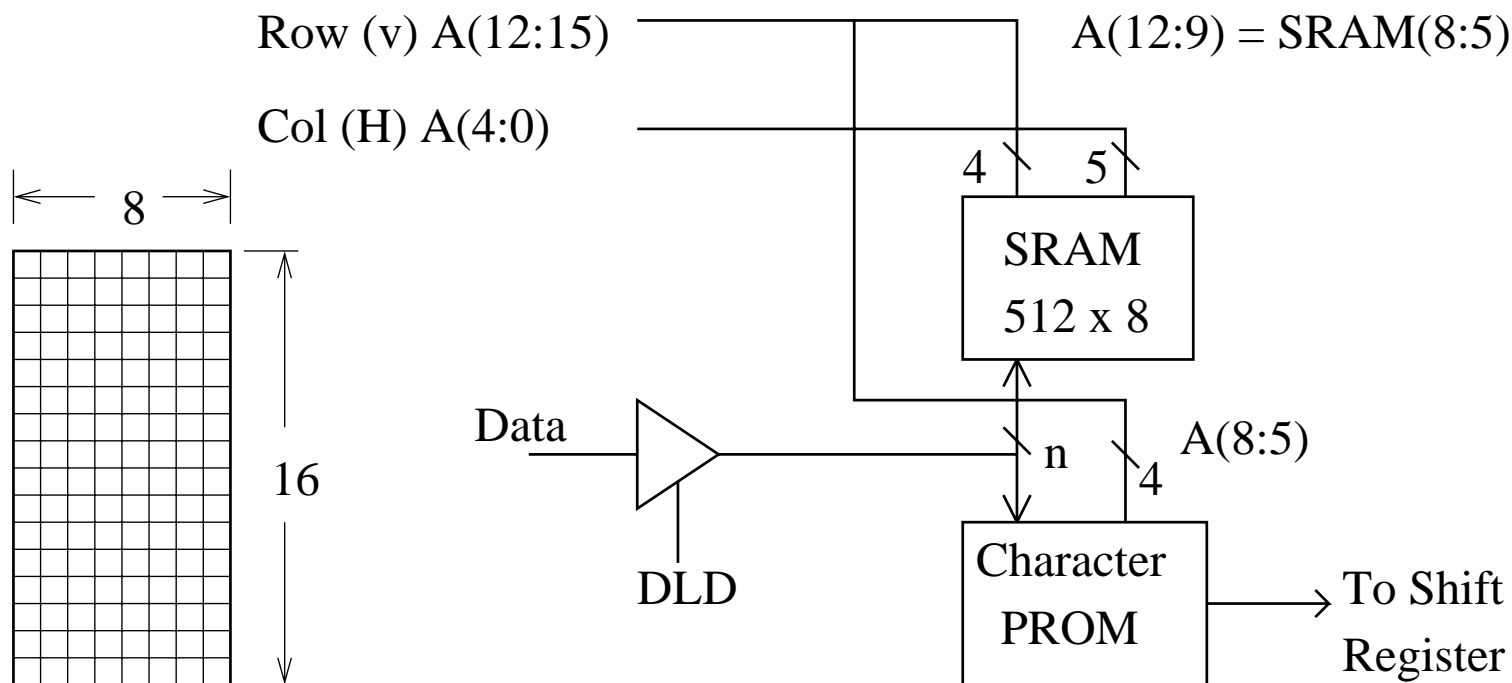|	R	G	B
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Purple	1	0	1
Yellow	1	1	0
White	1	1	1

R
G
B
Hsync
V sync

R G B
Monitor
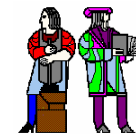
- **Characters are fixed bit patterns.**
  - □ **They always have the same shape but can appear at different places on the screen.**
  - □ **Use of characters can save video memory and make the manipulation of video memory contents simpler.**

For a screen 256 x 192 one gets 384 characters. The screen address is used to specify the position and part of the address of the character ROM

Row (v) A(12:15)

Col (H) A(4:0)

A(12:9) = SRAM(8:5)

8

16

4   5

SRAM
512 x 8

Data

DLD

n   4   A(8:5)

Character
PROM

To Shift
Register

- **Row formatting is not as simple as before.**
  - □ **But remapping is easily done in an HDL.**

For a screen 256 x 192 one gets 512 characters. The screen address modified by combinational logic is used to specify the position and part of the address of the character ROM

Col (H)

Row (V)

Combinational Logic in HDL

H

L

A(4:0)

4

5

SRAM 512 x 8

Data

DLD

4

n

Character PROM

8

12
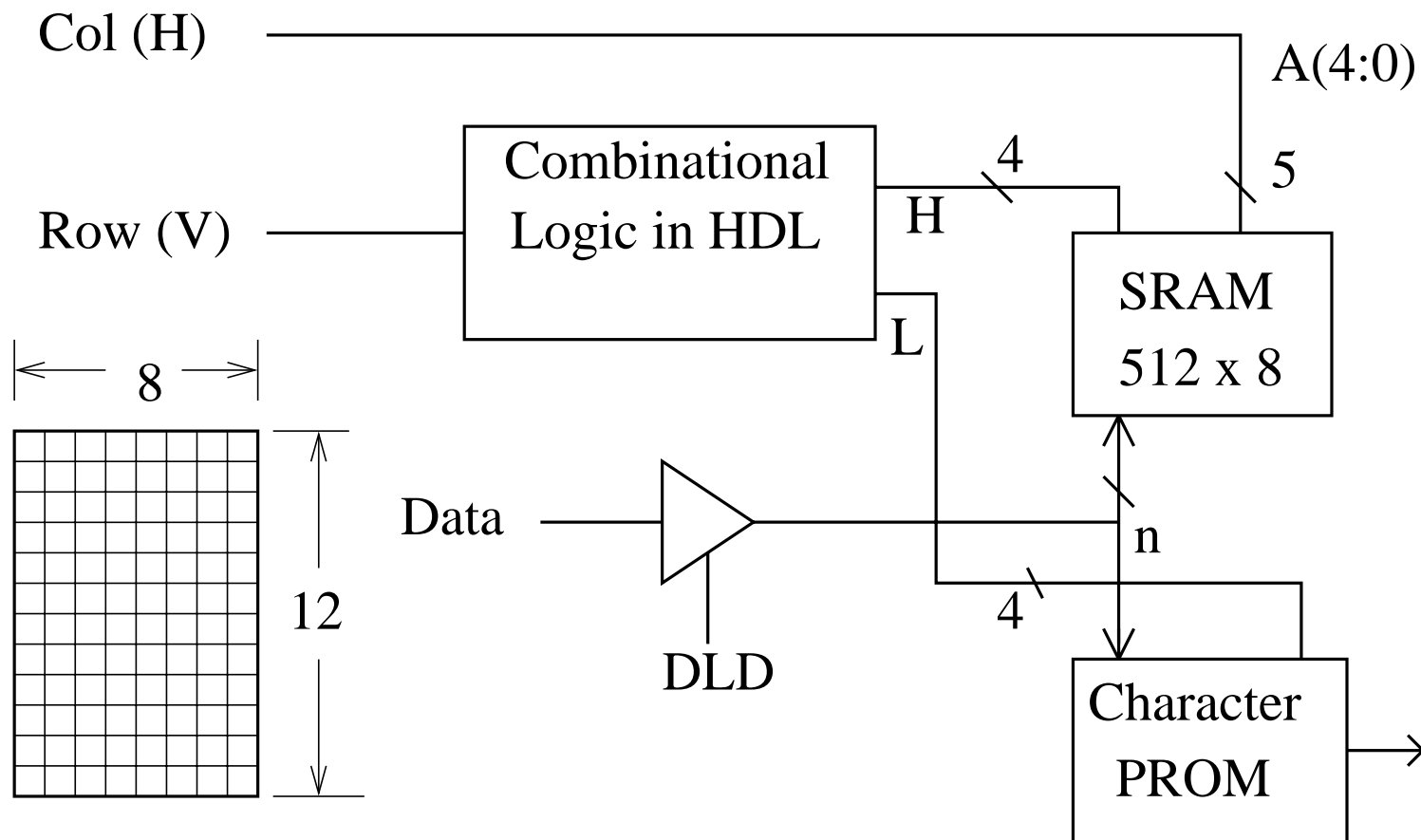
- **Sometimes, pairs of characters can create the same motion effect as bit-mapped graphics.**
  - **The speed of the motion depends on the update rate.**

- **These 24 characters (12 x 2) can display an arrow at any vertical position.**