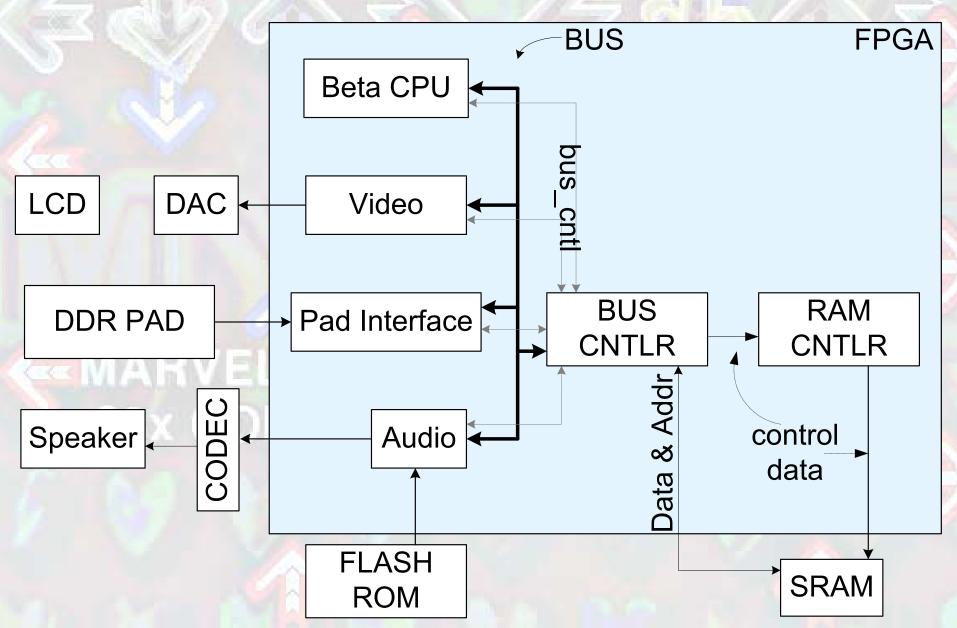
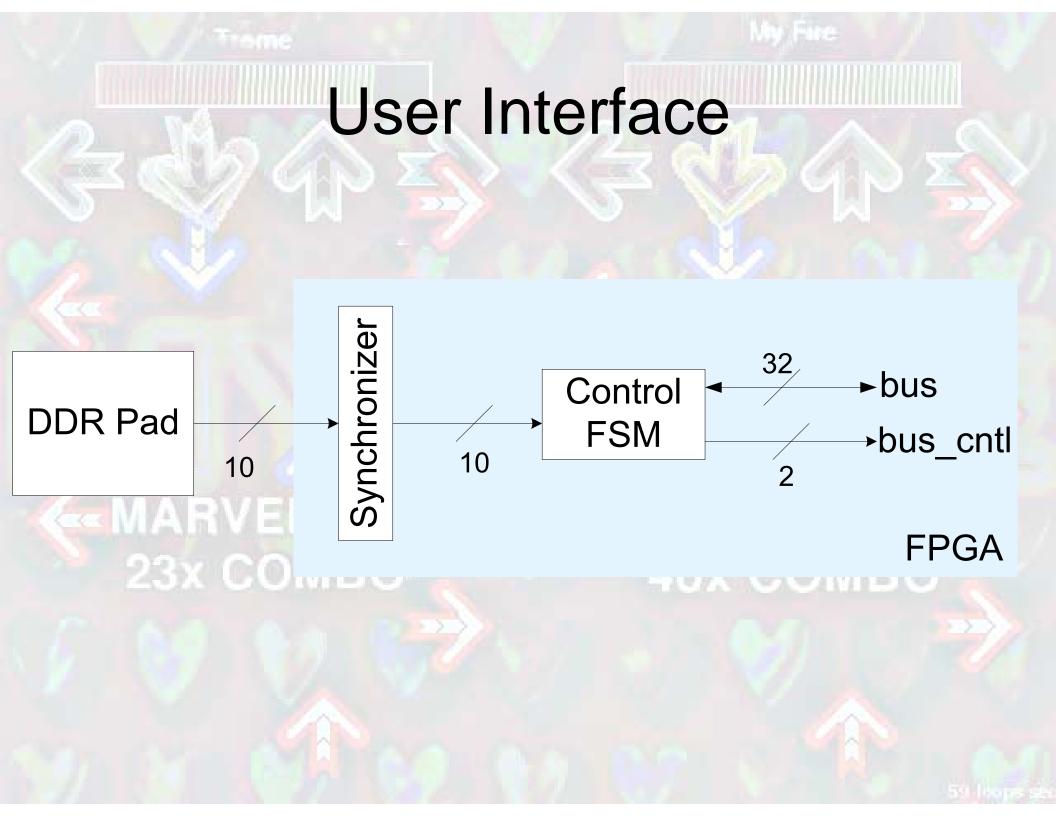


Design Overview User Interface Beta CPU Software Audio Video / EL ous PERFECT 23x COMBO 46x COMBO

Overall Block Diagram



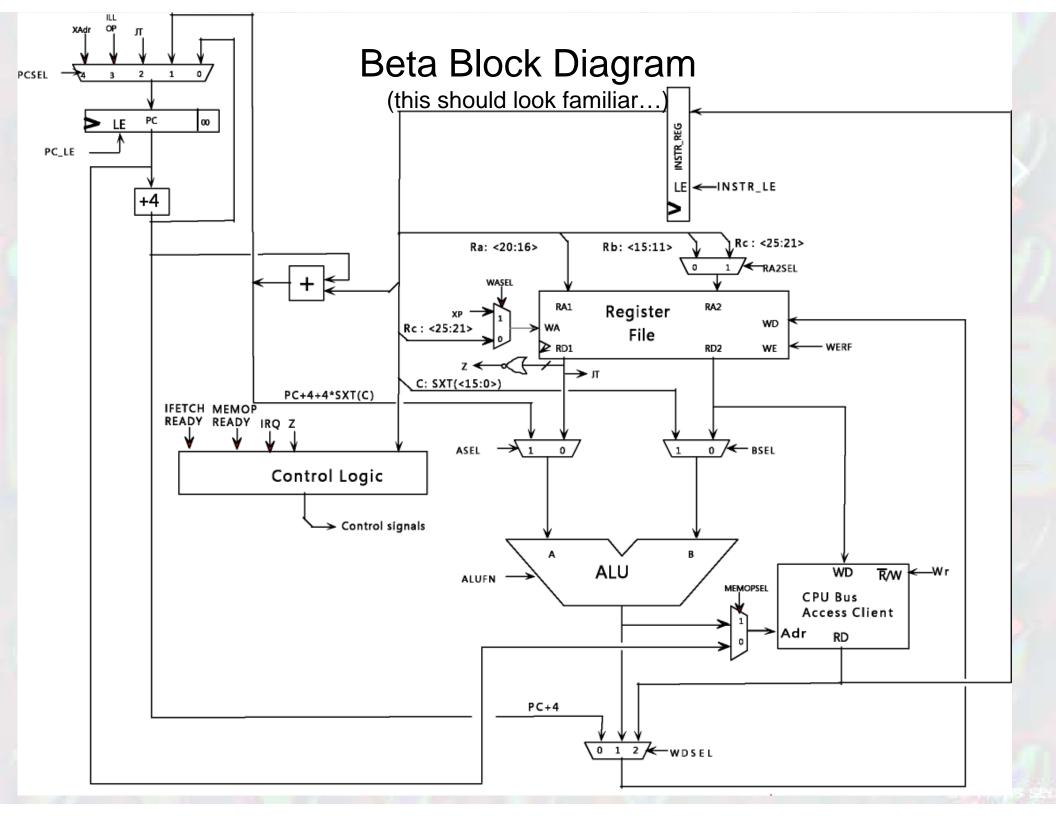


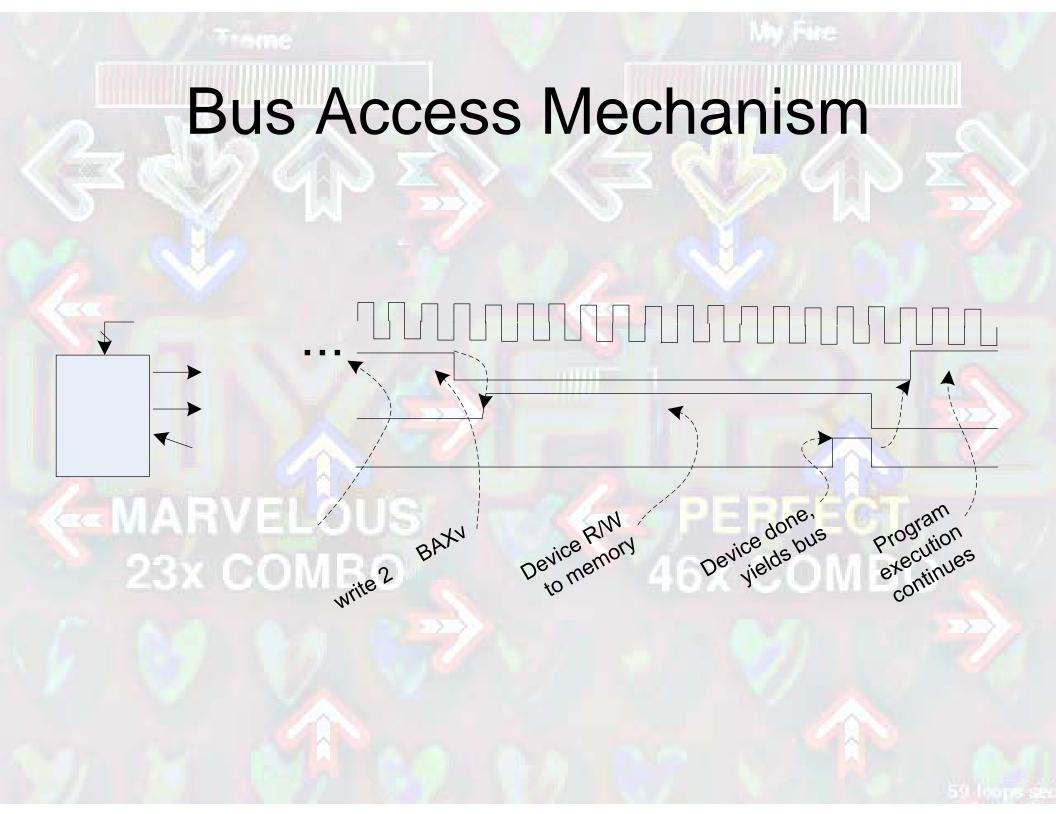
Beta CPU

- Non-pipelined, 4.5 MIPS @ 27 MHz i386 (1993): 5 MIPS @ 16 MHz
- Full support for beta ISA
 - RISC "Load-Store" Architecture

MARVELOUS

- Shared memory bus
 - Bus controller arbitrates access to main memory between up to 8 devices.





DDR Software

- Determine current time.
- Look at list of "correct" steps.
 - Any past by > ¾ sec? No points! Advance ptr.
 - Any recently (<¾ sec) past? If matches user input, award points = f(user_time-correct_time). Dequeue input & advance correct step ptr.
- Any more user input?
 - Steps are early! If < ¾ sec early, award points on same function as before. Dequeue input & advace correct step ptr.
- Rebuild display with upcoming steps & score
 - Gradient background + bilblt'd gliphs (text, arrows, etc.)

Audio

