Massachusetts Institute of Technology

High Speed Digital Design Overview

- Overview of Printed Circuit Board Technology
- Issues in Signal Integrity

Lecture material courtesy of Keith Kowal

Introduction

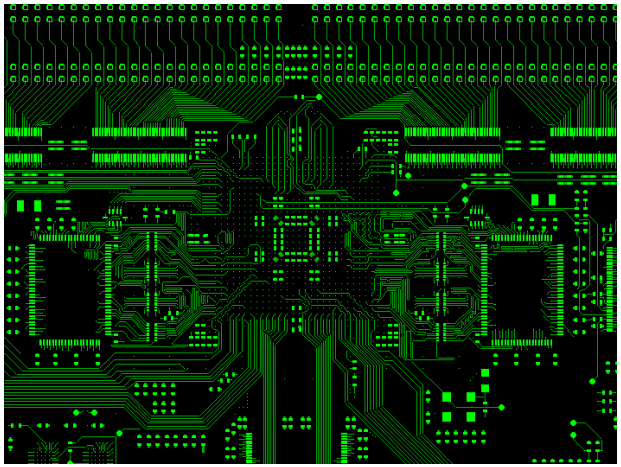
- My Motivation
- PCB Overview
  - Terminology
  - PC Board construction
  - Components
  - Assembly
- Signal Integrity Introduction
  - Decoupling
  - Components
  - Transmission lines
  - EMC/EMI

PCB History

- The inventor of the printed circuit was probably the Austrian engineer Paul Eisler (1907 - 1995) who, while working in England, made one in about 1936 as part of a radio set. In about 1943 the USA began to use the technology on a large scale to make rugged radios for use in World War II. After the war, in 1948, the USA released the invention for commercial use. Printed circuits did not become commonplace in consumer electronics until the mid-1950s.
- Before printed circuits, point-to-point construction was used. For prototypes, or small production runs, wire wrap can be more efficient.
- Originally, every electronic component had wire leads, and the PCB had holes drilled for each wire of each component. The components were then soldered into the PCB. This method is called *through-hole* construction. This could be done automatically by passing the board over a ripple, or wave, of molten solder in a wave-soldering machine. Through-hole mounting is still useful in attaching physically-large and heavy components to the board.

From wikipedia

PCB Example – 1 layer



Product Development

- Hardware Design
  - System – Documentation, interfaces, software, power, etc.
  - Board hardware - Schematics,FPGAs, parts availability
  - PCB Design – Simulation of PCB for Signal Integrity
  - PCB Assembly – reflow, IR : wave soldering
  - PCB Test – Netlist, General Radio. Flying probe, System test
- Qualification – reliability [temperature, vibration, esd …]
- Compliance – FCC, Safety [UL] – domestic and foreign

Printed Circuit board Basics

- Material used for dielectric
  - Fiberglass - FR4, prepreg, epoxy/glass
- Copper Layer construction
  - Signal, Power, Ground
- Multilayer interconnect
  - Vias, through hole connectors
- Process
  - Through hole & SMT
  - Techniques – multilayer, ***Flex***

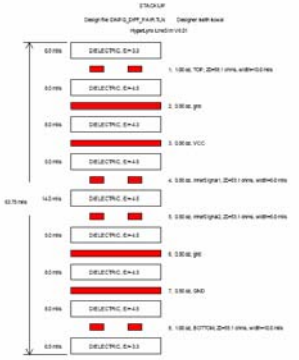
PCB Design Components

- Planes
  - Solid, split (hatched, rarely used)
- Dielectric Layers – Prepreg, epoxy glass, other
- Silkscreen
- Soldermask
- Surface finish – bare copper, tin plate, gold
- TEST points! (used for bed of nails or flying probe testing)
- Signal Layers
  Trace impedance (technology @ 4mil – 0.004", good manuf. yield)
  Board layer impedance – per layer / stackup
- Multilayer Interconnect - Stackup / design rules
  - Through / Blind / Buried / manufacturing cost
- Components – thru hole / SMT / components on both sides
  - PCB Fine pitch components, BGAs, passives – caps / ferrites / resistors

Layers

- Multilayer PCB construction (stackup)

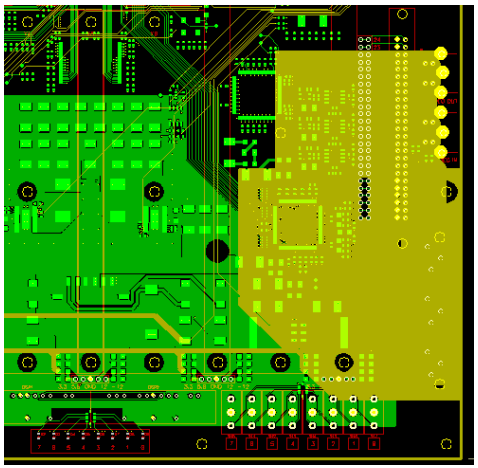
S= signal
G = ground plane (solid)
V = Voltage plane (solid/split)



Planes

- Solid – Copper
  - (1 oz Copper = thickness 0.0014)
  - (1/2 oz Copper = 0.0007)
  - Ref. 1oz copper = 1 ft^2
- Solid – filled / voltage and ground
- Split – voltage plane
  - Ground plane (generally is not split except for High voltage isolation - e.g. Ethernet connectors

SPLIT Planes



Dielectric Materials

Glass/epoxy
- *Thickness 0.001 through 0.007 / Er = 4.7*

Solder mask
- Liquid photo imageable (5-20uM)

Prepreg
- thickness 0.0016 through 0.0066
- Er = between 4.3 and 5.0

Polyimide Er = 4.0 to 4.5 (at 1.0mhz) (specific Er is dependent on glass-to-resin , Er is virtually constant from 1.0mhz to 3.0ghz).

Rogers corporation
- ULTRALAM Â® 2000PTFE/ woven glass
- RT/duroid® Â® 5870 PTFE/ random microfiber glass
- RT/duroid® Â® 5880 PTFE/ random microfiber glass
- RT/duroid® Â® 6002 PTFE/ ceramic
- RT/duroid® Â® 6006 PTFE/ ceramic
- RT/duroid® Â® 6010LM PTFE/ ceramic

What is Relative Dielectric Constant, e_r ?

- Relative dielectric constant, e_r, is a measure of the affect an insulator has on the capacitance of a pair of conductors as compared to the same conductor pair in a vacuum.
- The dielectric constant of a vacuum is 1. All materials have e_r greater then 1.
- The higher the e_r the lower the impedance.

e_r

- An equation to calculate e_r using velocity
- All dielectrics slow electromagnetic waves down according to the equation below.
  - Sqrt [e_r] = C / V

    where: C = speed of light, 0.0118 INCH/pSec

    V = measured Propagation Velocity

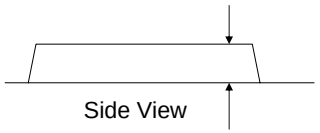
Material	e_r	Velocity (in/nSEC)	Velocity (pSEC/in)
Air	1.0	11.76	89.4
Rogers RO	2.9	6.94	143.1
FR-4/Glass	4.3	5.82	172.0
Water	73.0	0.4	2200.0

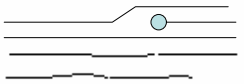
ETCH

- Copper

  (H=1/2 oz Copper = thickness 0.007 in.)
  - Trapezoidal - typical
  - Over etching – higher Zo
  - Under etching – lower Zo
  - Shapes (small inductors)
  - Delay – about 1.6ns/ft

    is slower at higher temperatures
  - General Design rules
    - F(layer) = 4mil etch 6 mil spacing





Plan view

Surface Finish

Surface Finish

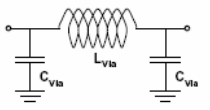
Classification	Electroless Tin Plating	Electroless Gold Plating	Solder Leveling	Organic Coating
Standard Space	10mil	10mil	10mil	10mil
Minimum Space	4mil	4mil	4mil	4mil
Solder Mask Thickness	.0001 to .0010	3 to 10m inch	.003 to .0015	
Tayo	Yes	Yes	Yes	Yes
PROBIMER 52	Yes	Yes	Yes	Yes
Dry Film	Yes	Yes	Yes	Yes

Vias

- Vias Connect layers
- Anti-Via – term for area around via
- Barrel – finished diameter
- Tented – solder mask

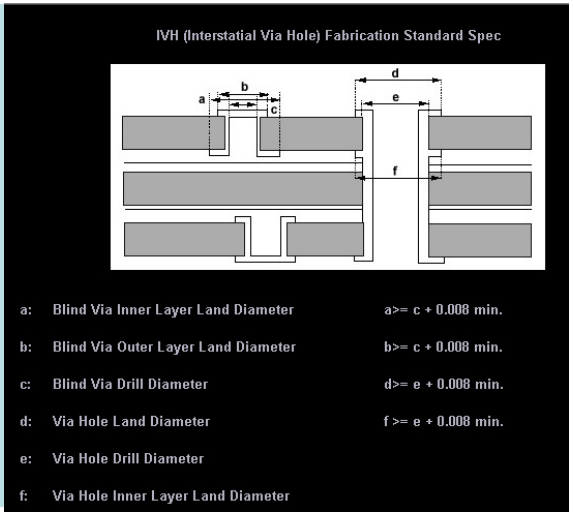
Stitching technique – lower inductance

Through hole - Thermal relief (power plane)



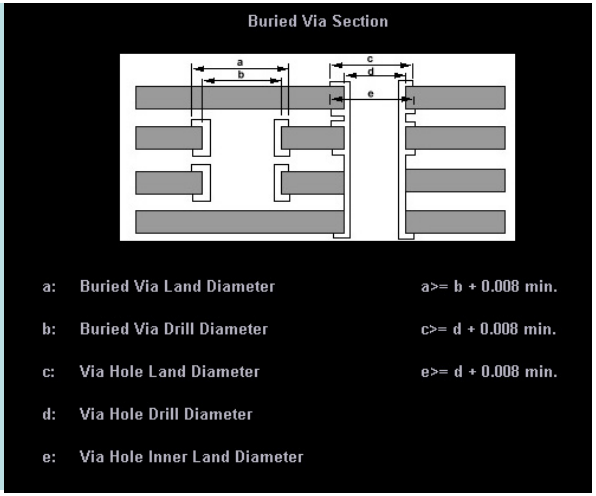
Blind Via

- The blind via hole connects the surface layer to one or more layers of a multilayer board. This via is plated and does not go though the entire board.



Buried Via

- The buried via is shown as a plated through hole connecting two or more layers which is buried within the board structure.

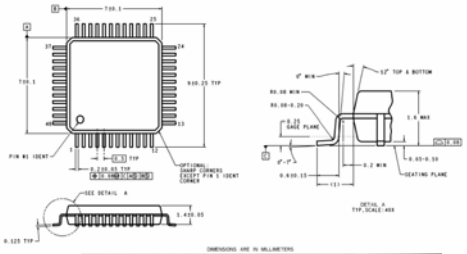


Pads

Pads for SMT components

*Through hole

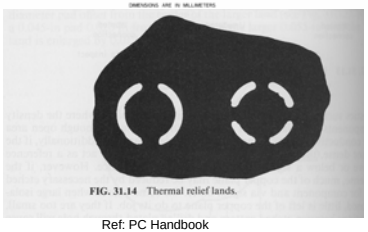
* SMT



Inner layer - Thermal Pads

* Used for through hole connectors and power components

* used for reliability and repair in de-soldering



Ref: PC Handbook

PCB Design

- Software tools – import schematic based netlist and component information
  - Make up library components that match physical characteristics of actual device and design pads to match component footprint and manufacturing constraints.
- Process technology – Gerber Files, aperture file, drill file, Fabrication Drawing

PCB Fabrication

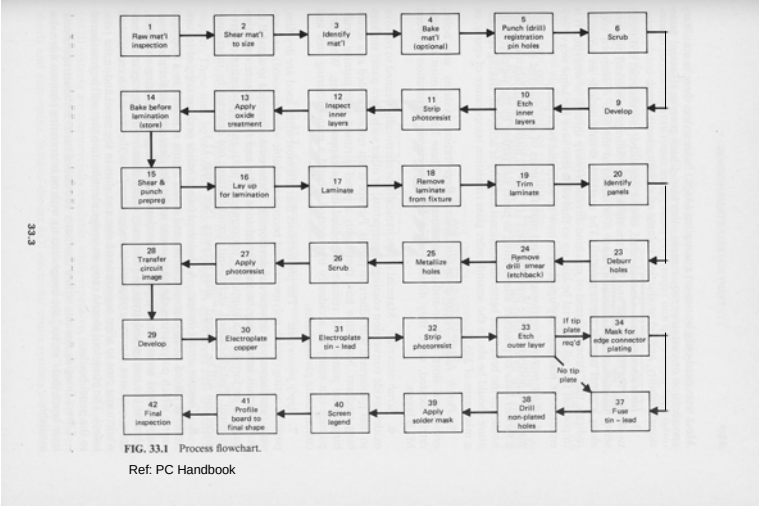


FIG. 33.1 Process flowchart.

Ref: PC Handbook

Board Assembly

- Solder Paste application - stencil
- Pick-n-Place
- Reflow - IR / vapor phase
- Wave Solder
- Visual Inspection - defects
- Testing / repair

REFLOW

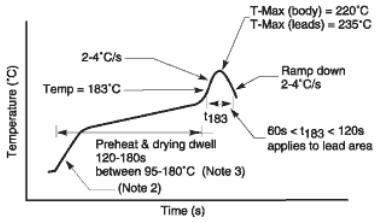


Figure 5-3: **Typical Conditions for IR Reflow Soldering of Sn/Pb Solder**

Notes:

1. Max temperature range = 220°C (body). Minimum temperature range before 205°C (leads/balls).
2. Preheat drying transition rate 2-4°C/s
3. Preheat dwell 95-180°C for 120-180 seconds
4. IR reflow shall be performed on dry packages

Courtesy of Xilinx

BGA components

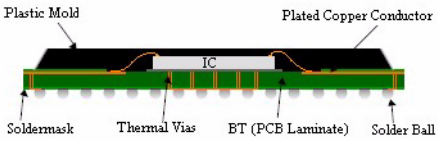


Figure 1-1: **'Cavity-Up' Ball Grid Array Package**

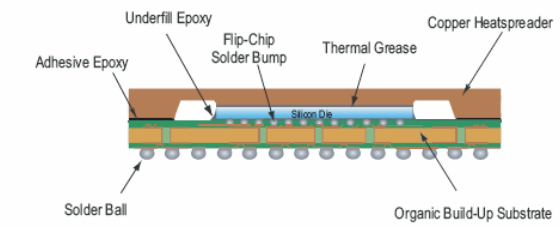


Figure 1-4: **Flip-Chip Package**

Pictures Courtesy of Xilinx

PCB specifications

- Instant Online Quote Capabilities for our Standard Full Service Product
  2 to 8 Layers
- Quantity: 1 to 10 pieces
- FR4 material (dielectric)
- 2 Layers: **Same day turn** to 3 days turn time
  4 Layers: 1 day to 3 days turn time. (3 days price has no premium over a 4 or 5 day price!)
  6 Layers: 1 day to 4 days turn time. (4 days price has no premium over 5 day price!)
  8 Layers: 1 day to 5 days turn time.
- .031 to .125 inch thick boards
  10 square inches to 155 square inches boards
  8/8 mil trace and space to 5/5 mil trace and space
  All types of Gold finish
  ¼ to 2 ounce Copper Weight
  8 mil to 12.5 mil holes
  Gold Fingers
  Scoring, Tab Routing or Route and Retain
  Standard Product Boards are **Design Rule Checked** and **100% Netlist Tested**
  No multiple parts or part numbers **(please give us a single image of a single PCB)**
  For more details see our Frequently Asked Questions page.
  and see our Product Comparison
  Courtesy of sierra proto express

for technology minimums and maximums refer to the web page below - typical

- https://www.2justforyou.com/NASApp/sierraproject/jsp/destination3_new_products_.jsp?sourcex=np121202#ourproducts

Some PCB Issues for Hdw Designers

- BGA breakout vs number of layer needed
- What is the best way to decouple a BGA
- Split planes – return path concerns
- Routing clocks to minimize skew
- High Speed / High Gain op Amp layout
- DC-DC power chip layout – to Reduce EMI
- Jitter Concerns (e.g.data,clk) and Differential Pair routing
- Crosstalk / digital lines effecting Analog signal
- Things that could go wrong

http://www.electronics.ca/cbt/album/ph_smd.html

Signal Integrity Introduction

- WHY
  - Technology gets faster or changes
  - As a Hardware designer early 80's we mostly cared about signal propagation delay on and off chips.
  - FCC RF emission limits for consumer products – commercial product limits are different.
  - Complexity of digital designs has increased
  - **Today**, speeds top 2.5gb/sec

Signal Integrity

- In Hardware Design
  - Frequencies > DC and frequencies < 1 GHz (FCC)
  - Applies to board design as well as chip design
  - Transmission of signals - delay / quality / error rate / reliability
  - Clocking [oscillators] and clock skew and clock distribution
    single-ended vs. differential pair [LVDS,PECL…technology]
  - -- Emissions -> lower (e.g. radiated harmonics)
  - Crosstalk -> lower (e.g. aggressor vs. victim scenario)
  - cables / flexible PCBs / Hot swap boards
  - Power Supplies / power sources / Decoupling capacitors
- What it is NOT SI major focus

Power concerns for trace widths ? – heat dissipation ? / these are reliability
High-voltage isolation – ESD
mechanical enclosure design – but is part of FCC compliance

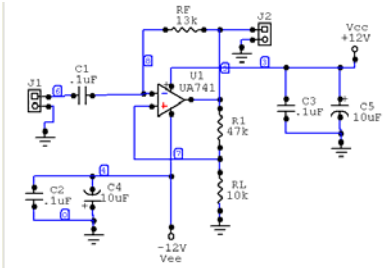
SI describes the environment in which the signal must exist. It covers the various techniques and design issues that ensure signal are undistorted and do not cause problems to themselves, to other components in the system, or to other systems in proximity / (xilinx)

Picture - Courtesy of Mentor Graphics

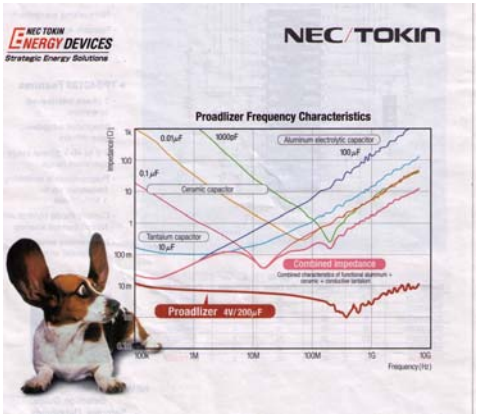
Decoupling Capacitors

- Each IC should have at least 1 decoupling capacitor – local filtering per pin (if possible or needed)
- Use low ESR capacitors / check tolerance
  - ESR = equivalent series resistance
- Check temperature characteristics on ceramic caps
  - Capacitors of equal value are not all created equal
  - Technology
    Electrolytic - varies widely with temperature, beware of tolerance
    Z5U dielectric - below 10 degrees C is not recommended
    X7R dielectric – better temperature and aging characteristics
- Local bypass caps provide low impedance at higher frequencies
- $F_{bypass} = X_{max} / (2 \pi L_{C2})$: $X_{max} = 0.1$ ohm $L_{c2} = 5$ nH
  - L_{C2} = lead inductance causes the impedance to go up, at very high frequencies. $F_{bypass} = 3.18$ MHz.
  - C =Tradeoff operational frequency of IC and max current needed
- The best way to provide a low inductance path is to parallel a lot of small capacitors

Decoupling



Example shown above



Ref: EDN April 2005

Transmission of signals

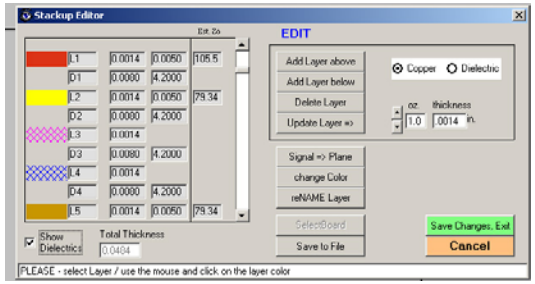
- **SI Goals Defined**:
  Quality
  - Timing between ICs and system components + margin
  - Susceptibility - Surrounding signals may interfere
  - Conducted emissions (FCC, international requirements)
  - Radiated emissions (FCC, international requirements)

- **Design Goals Defined**:
  System Reliability
  - Bit Error Rate
  - System clock margining (v, f , t)
  - Component selection
  - ESD
  - other – earthquake / Belcore / MIL / altitude

Board Impedance Calculation

- Zo is dependent on where the trace is located for any given stack up
- Controlled Impedance vs. controlled construction - Cost $
- Transmission line
  - Zo =sqrt (L / C) : characteristic Impedance
  - Minimize Reflections

Zo Calculator



Zo calculators:

http://www.icd.com.au/
http://www.emclab.umr.edu/pcbtlc/microstrip.html
http://www.sunmantechnology.com/resources/cal_cat00.shtml
http://www.rogers-corp.com/mwu/mwi_java/mwij_vp.html
http://www.csgnetwork.com/boardrunimpcalc.html

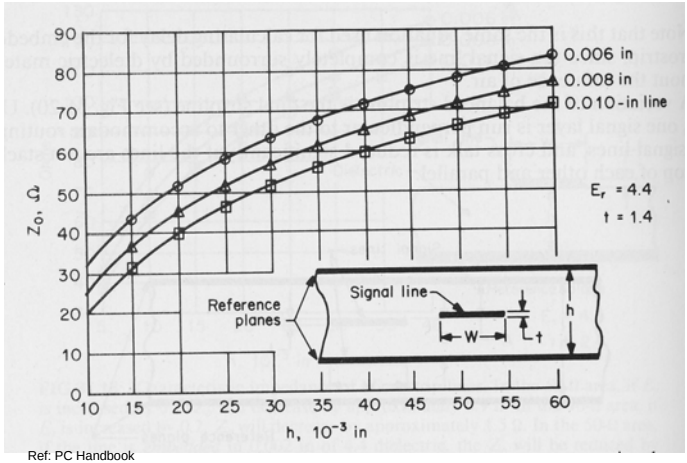
Zo Calculations

- Traces usually involve vias which effect Zo calculations
- Calculations usually ignore adjacent signals
- Manufacturing Process variation
- Solder mask effects Zo (outer layers)
- The Classic mistake – when changing layer, many designers do not keep the same impedance on the routed signal.

Zo Microstrip - equations

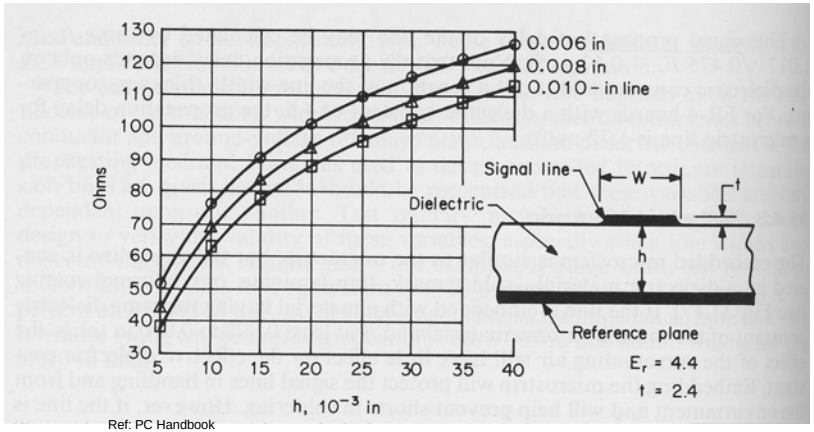
```
tmp1 = (w / b)    : w=width (inches) , b=height above plane (inches)
If tmp1 < 0.35 Then
        tmp2 = (w / 2)
        tmp3 = ((t / (PI * w)))
        tmp4 = (4 * PI * w) / t
        tmp5 = 0.255 * (t / w) ^ 2
        ZSTR_K1 = tmp2 * (1 + (tmp3 * (1 + Log(tmp4)) + tmp5))
        ZSTRIP = (60 / Sqr(er)) * Log((4 * b) / (PI * ZSTR_K1))     ' skinny
Else
        tmp2 = 1 - (t / b)
        tmp3 = 1 / tmp2
        tmp4 = tmp2 ^ 2
        ZSTR_K2 = (2 * tmp3 * Log(tmp3 + 1)) - ((tmp3 - 1) * Log((1 / tmp4) - 1))
        tmp3 = 1 / Sqr(er)
        tmp4 = w / b
        tmp5 = ZSTR_K2 / PI
        ZSTRIP = (94.15 / ((tmp4 / tmp2) + tmp5)) * tmp3   ' wide
End If
```


Microstrip Zo Plot



Ref: PC Handbook

Stripline



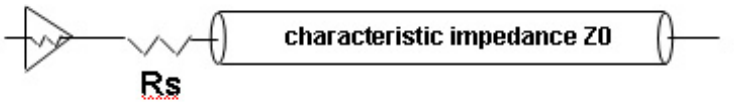
Ref: PC Handbook

Technology

- TTL
- ECL (emitter coupled logic)
- BTL (backplane transceiver logic)
- HC/ABT, etc.
- LVDS – single ended, differential
- PECL – single ended, differential

- Analog – audio, raw video
  - Susceptibility to digital signal interference (e.g. Telco)

Series Resistor Termination



driver impedance + Rs = Z0

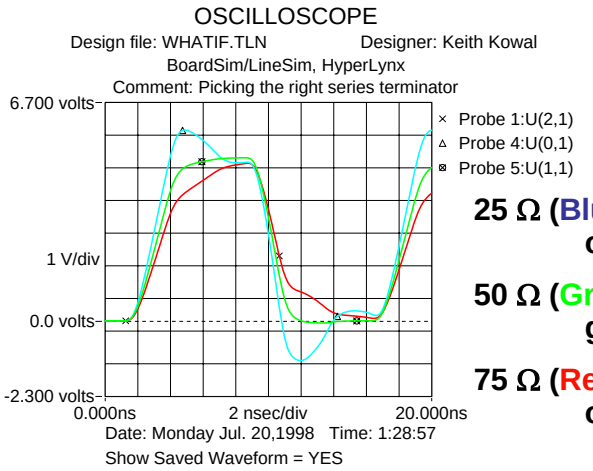
Half step into line; doubles to full step at end; reflection from end dies at driver

Proper Termination

- Overshoot
- Undershoot
- Termination resistor/component placement

Demo – transmission line animation

Proper Termination (con't)



25 Ω (Blue; too low, overshoot)

50 Ω (Green; good match)

75 Ω (Red; too high, over-damped)

Transmission of signals - Methods

- Prerequisites
  - Decoupling
    - Bulk – large value / Tantalum, electrolytic
    - IC – 1 per pin , generally High Frequency 0.1uf
    - Using Ferrites and Voltage plane islands
    - Types of caps – Electrolytic, SMT - Ta, Ceramic
    - Calculation

      Power supply rejection

      Lower EMI
- NET topology, number of loads, technologies used

Termination (SI)

- **Series -** Single component - Low power - Damps entire circuit – single receiver
- **Pull Up/Down -** Single component -Value choice easy - OK for multiple receivers

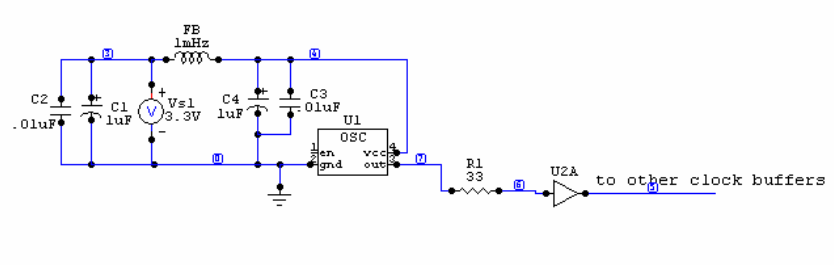
  - e.g. noisy microprocessor bus with many peripheral chips

Termination (EMC)

- **Type Summary - Series -** Best Reduced driver currents give good performance. Works best when resistor is very close to driver
- **DC Pull Up/Down -** Good Less ringing generally reduces EMC. At certain frequencies this may increase
- There are many more types of termination schemes

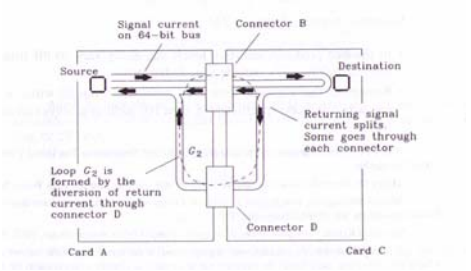
Ferrites

- Used for EMC
- Oscillators



Connectors

- Proper Ground pin distribution
- Proper terminations



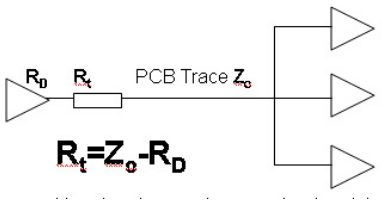
Oscillators

- Frequency – the higher tolerance > $
- Stability – temperature
- Aging - time
- Voltage sensitivity – power supply noise rejection
- Other - jitter, shock, vibration, humidity

- Proper decoupling and PCB layout

Clock distribution & clock skew

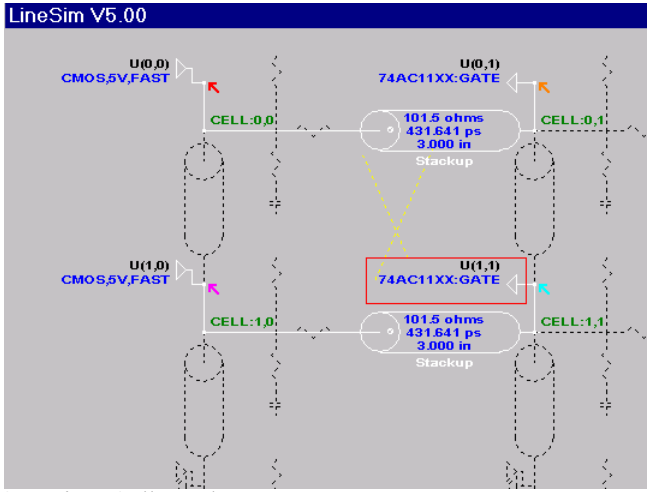
- Fan-out
- Delay lines



Crosstalk

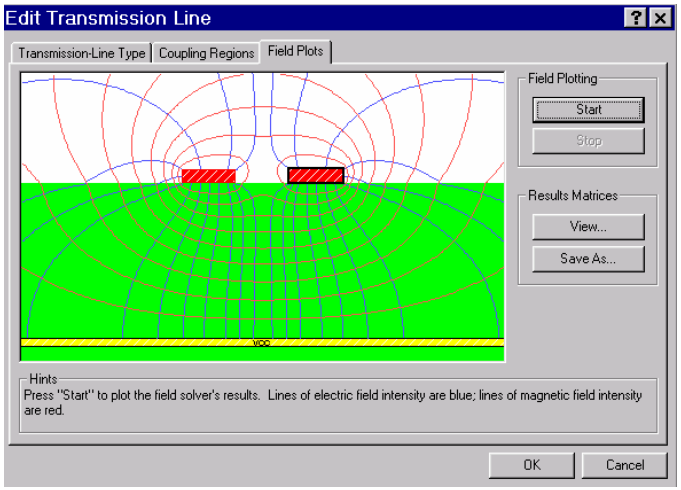
- Victim & Aggressor scenario
- Guard traces – not generally a good practice
- Adjacent pins – on ICs or Connectors
- Co-planner Traces
- Adjacent parallel traces
- Mutual capacitive/inductive
- Differential signaling
- Sips – single inline package
- Reduction
- Simulation

Crosstalk Simulation - prelayout



Courtesy of Mentor Graphics - Hyperlynx

E/M fields



Courtesy of Mentor Graphics - Hyperlynx

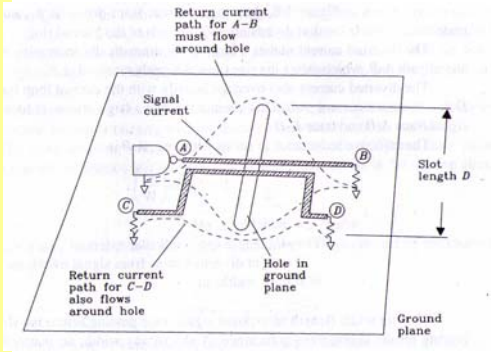
GND ?

- Analog vs. Digital Ground
  - used for isolation purposes, keeping digital induced noise away from sensitive circuitry inside an IC

Chassis Ground – reduction of FCC emissions

Planes

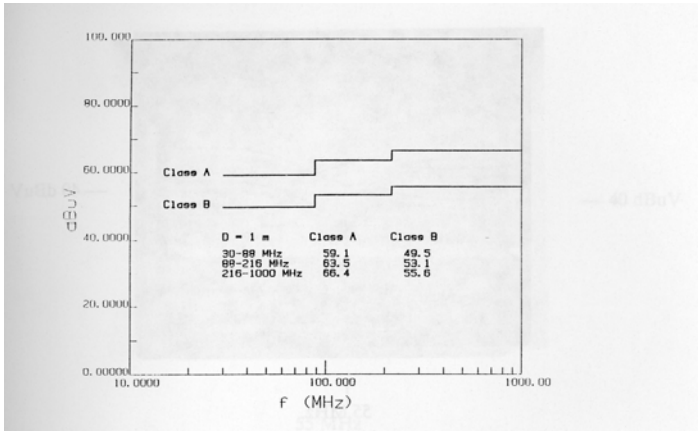
- Isolated planes – its common to reduce noise by making an island under a BGA for power – not Ground!
- Split planes – when signals cross split or isolated planes watch out for the return path



FCC Product requirements

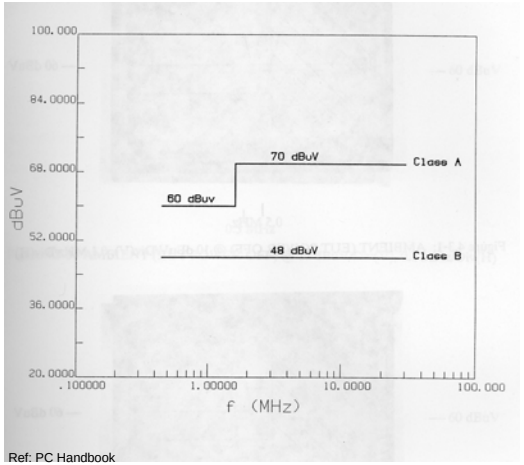
- Limitations FCC [class A, class B]
- Conducted
- Part 68 - Telco

FCC radiated limits



Ref: PC Handbook

FCC Conducted Limits



Ref: PC Handbook

Reduction of Emissions

- Proper termination of clocks / signals
- Keep trace runs short , but that doesn't mean that you have solved the problem
  - For FPGAs,Control slew rate of output buffers
- Keep slower signals on outer layers
- Good decoupling practice, including Ferrites for ICs and oscillators
- Build in emission compliance by simulation

SI Software

Time Domain – generally used for signals below 1gHz

HyperLynx – LineSim, BoardSim, Multiboard (which I wrote)

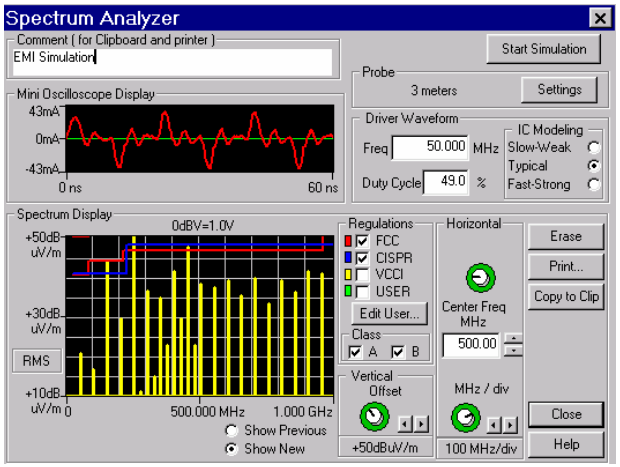
SpectraQuest – similar to spice

Frequency Domain

Ansoft – HFSS, many more

3-d structures modeling

EMI Simulation



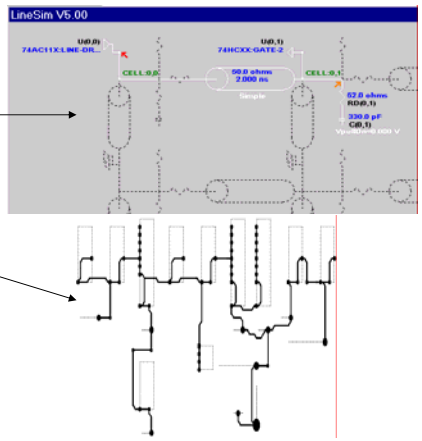
Courtesy of Mentor Graphics - Hyperlynx

PCB Signal Integrity design Tools

- Pros/cons
  - Wave form analysis
    - * batch mode
    - – PreLayout (lump model) – spice
    - - Post layout
- EMC analysis
  - * Batch mode

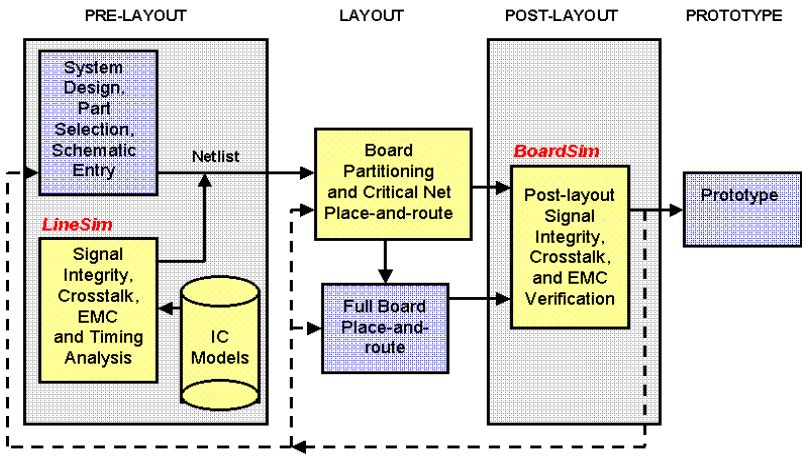
IBIS modeling

Courtesy of Mentor Graphics - Hyperlynx



Many trace segments, vias, branches and stubs make manual calculation of impedance very difficult.

Signal Integrity Design Flow



References

- High-Speed Digital Design, Howard Johnson, Martin Graham, Prentice Hall, 1993.
- Printed Circuits Handbook, Clyde F. Coombs, Jr., McGraw-Hill, 1988.
- Printed Circuits and Design Magazine, Designing High-Speed PCBs for First-Time Success, Keith Kowal, March 98.
- Several pictures provided by Mentor Graphics, and Xilinx.