Recognition of Hand-Drawn Circuits

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Project Goals

• Input a hand-drawn circuit
• Recognize components and values
• Understand connectivity
• Generate primitive SPICE netlist

• Output to LCD monitor
Layout

• Draw components on 8x8 grid
• Each grid block 64x64 pixels
  – Component area
  – Text area

• Monochromatic image (binary)
Drawing Rules

- Entire component must fit in one grid block
- Appropriate borders must be crossed
- Component must avoid designated text area
- Drawings must be "reasonably" accurate
- Limited number of components

- Text must follow separate text grid
Recognition

- Memory Handling
- Component Recognition
- Text Recognition
- Store Information

Minor FSMs to recognize different components
Component Recognition

- Decision tree method
- Identify important characteristics
  - Number of terminals
  - Continuous?
  - Important “Gaps”
Decision Tree

Original Image

Edge Check

Vertical 2-Terminal Components
Horizontal 2-Terminal Components
1-Terminal Components (Top Edge)
3-Terminal Components

Recognized Component Uniquely Defined by Edge Combination

Recognized Component

Test for Discontinuities, Gaps, Thickness
Text Recognition

• Recognize text in 8x6 blocks
• Use pads to recognize 10 numbers and 7 letters
• Currently, users need to use straight lines
• More pads will be added to allow the user greater freedom in writing
Video Block Diagram
Raw Circuit Display
Ideal Circuit State Transition Diagram and Example Output
Spice Display Block Diagram

Global Inputs
- CLK
- RESET

Character ROM
- 8x288

DFS Stack (RAM)
- 6x64

Stack Manager
- stack_addr
- stack_data
- stack_ctl

Major FSM

Ideal Circuit Data RAM
- 20x64

Spice Display

Sync Generator
- active
- node_addr
- node_data

Video RAM
- 8x60000

Swaps
- vram_addr
- vram_data

HSYNC
- VSYNC
- BLANK
Spice Display State Transition Diagram and Example Output

V0 0 1   DC 5
R0 1 2   100k
Q0 2 3 3 NPN
Analysis Flowchart

- Depth-First Search with Enqueued List
- Enqueued List is 64-bit register
- Stack module abstraction
- Node RAM holds values for all possible nodes
Timeline

- Current Status: Partial component recognition, raw circuit display
- April 22: Component recognition, ideal ckt display without nodes
- April 26: Basic serial communication, ideal ckt display with nodes
- May 2: Load circuit bitmaps over serial line, Spice Display
- May 9: Save spice files over serial line