

Massachusetts Institute of Technology  
Department of Electrical Engineering and Computer Science

## 6.111 – Introductory Digital Systems Laboratory

### General Information

#### In-charge and Lecturer

Prof. Anantha Chandrakasan, Room 38-107, 258-7619, [anantha@mtl.mit.edu](mailto:anantha@mtl.mit.edu)

#### Secretary

Margaret Flaherty, Room 38-107, x3-0016, [meg@mtl.mit.edu](mailto:meg@mtl.mit.edu)

#### TAs

Kyeong-Jae Lee ([kjaelee@mit.edu](mailto:kjaelee@mit.edu), x3-7350, Rm 38-600)

Theodoros Konstantakopoulos ([tkonsta@MIT.EDU](mailto:tkonsta@MIT.EDU), x3-7350, office hours in 38-600)

Javier Castro ([javy@mit.edu](mailto:javy@mit.edu), x 3-7350, office hours in 38-600)

#### LAs

Christopher Falling ([c.l.falling@verizon.net](mailto:c.l.falling@verizon.net)), Amir Hirsch ([amirh@mit.edu](mailto:amirh@mit.edu)), James J. Wnorowski ([jamwno@mit.edu](mailto:jamwno@mit.edu)), Yun Wu ([yunw@mit.edu](mailto:yunw@mit.edu))

#### Technical Instructor

Gim P. Hom ([gim@mit.edu](mailto:gim@mit.edu), Room 38-644, x4-3373)

#### Recommended Reading (Purchase is NOT required).

Logic Design: Randy Katz, Gaetano Borriello, Contemporary Logic Design, Pearson Education, 2005.

Verilog: Samir Palnitkar, Verilog HDL, Pearson Education (2nd edition).

*(Quantum Books, located at 4 Cambridge Center, Kendall Square, Phone: (617) 494-5042, [www.quantumbooks.com](http://www.quantumbooks.com)).*

**6.111 Homepage** <http://web.mit.edu/6.111/www/s2006/>

#### Component Pinouts/Data

Pinouts for most components easily available through the web (e.g., do a google search to locate the appropriate data sheet). We will post most of the relevant sheets needed for the labs on the course web site.

#### Conduct of the Subject (minor changes may be made):

#### Classes

In the first couple of weeks of the term, there will be lectures on Friday (to quickly ramp up on material needed for lab 1). Then, Fridays will be used for recitations (three parallel recitation sections from 1-2pm). Lectures and recitations are discontinued at the end of the term so you can focus on the final project (see course schedule for details). We will meet in the lecture hall (34-101) for project group presentations after the block diagram conferences. Notification of particulars of the project presentations will be sent by email to [6.111students@mit.edu](mailto:6.111students@mit.edu).

### **6.111 Lab (Room 38-600)**

The laboratory facilities are located on the sixth floor of Building 38. Each student will be issued his/her own Laboratory Kit which includes a proto-board, discrete components, a USB flash drive, oscilloscope probes, logic analyzer pods, wire stripper, chip extraction tool, etc. **The FPGA kits are shared and located on the lab benches.** Please turn-off the power to the kits when you are done using them. In the Digital Systems Laboratory (Room 38-600) you will find logic analyzers and oscilloscopes needed for the lab exercises. Please check the lab hours posted on the website for the hours. The lab will not be staffed by Teaching Assistants (TAs) or Lab Aides (LAs) all of the open hours. The schedule of TAs and LAs will be available on the course web page.

### **NO FOOD or DRINKS in the lab (38-600)**

There are lockers for the safe storage of your kits along the 5th and 6th floor corridors of building 34. Apply at the 6th-floor instrument room desk for one. You should also remember to periodically back up all of your important files (both on Athena and the USB flash drive). When the sixth floor entrance is locked, the alarm system for the lab is usually activated. You are to enter and exit via the 5th floor. If you get stuck in the Lab after closing, you MUST have a TA let you out.

### **Laboratory Assignments**

All laboratory exercises must be completed; these are intended to prepare you for the term project. In doing these exercises, each student works individually. We strongly recommend that you use a computer-based drawing package to draw block diagrams and schematics for the lab reports and final project.

### **Problem Sets**

Three problem sets will be issued. The problem sets will emphasize the material covered in lectures and recitations and the primary goal is to help you prepare for the labs.

### **Quiz**

There will be one quiz during the term before Drop Date.

### **Term Project**

The most important assignment is the Term Project, about which you will receive more detailed instruction later. In doing this assignment, you will work with one or, at most, two partners. You should begin finding your partner(s) early in the term.

### **Grading Policy**

Late work will be penalized. Lateness of the lab assignments will result in a 20% per day penalty for work completed 1-5 working days after the due date. No point credit will be given for unexcused lateness exceeding 5 days.

The Lab 1 Checkoff sheet is to be initialed by a TA or LA and included with your report. Note that the checkoff sheet is NOT the report. Lab 1 report template is posted on the web site.

Lab 2 report will be used for part of the CIM requirement. More details will be provided in lecture.

Lab 3 will only include the checkoff. There is no need to write a detailed lab report for lab3. The lab will have instruction on what is to be turned.

Lab 4 has an intermediate checkoff (not graded) and the final checkoff. There is virtually no modification required to a report depending on the working of your lab implementation. However, reports with no lab effort will receive a zero.

The term project requirements *must* be completed in accordance with the schedule given in the instructions. You must make a presentation of your part of your project to the rest of the class after the logic diagram conference. You must demonstrate (i.e., present) your term project even if it does not fully function, and you must submit the written report in order to receive a passing grade.

The following approximate weights will be used to determine your course grade:

Quiz	10%
Problem Sets (3)	3%
4 Lab Exercises	
Lab 1 (check-off, report)	9%
Lab 2 (check-off, report)	10%
Lab 3 (check-off, no report)	7%
Lab 4 (check-off, report)	11%
Writing (Lab 2 revised report - part of CIM requirement)	10%
Class participation (lectures, recitations, project presentations)	3%
Final Project	37%

We construct a histogram of these summary numbers and proceed to discuss individual performances of all students. Some of the factors considered are:

1. Completion of labs. Past history has been that it is rare for a student to receive an A without completing the labs.
2. Project performance.
  - a) Any student who does not turn in a final project report will receive an F.
  - b) Students who do not construct a project will receive an F.
  - c) Project complexity is an important factor in discriminating between an A and a B. An A is rarely given if the final project is not as complicated as lab 4.
  - d) **It is extremely difficult for a student to receive an A without completing the final project.** Of course, it is possible to get a grade lower than an A even if the final project is completed.

Although 6.111 has a significant classroom component, it is *primarily* a lab subject. Accomplishments in the lab tend to be weighted more heavily than other components. The classroom component is viewed as supportive of the lab components. Some material covered in lectures will be related to advanced topics (power dissipation, mapping to ASICs, testing, etc.). Some the concepts might not be applicable to your final project but are important emerging digital system issues in industry today.

Traditionally, both average grade levels and average performance have been quite high in 6.111. A large number of students do “A” level work and are, indeed, rewarded with a grade of A. The corollary to this is that, since average performance levels are so high, punting any part of the subject, can lead to a disappointing grade. It is important that you keep up with the work.

Finally, and unfortunately, it is important for us to outline our expectations for academic honesty in 6.111. We do this not because we expect any of you to be dishonest, nor to insult your intelligence or character, but to avoid any misunderstandings.

First, the quiz is to be an individual effort. The problem sets and lab exercises are also to be individual efforts; however, it is okay to ask questions, get help from us, fellow students, or anyone else. But then, do them by yourself. Indications of collaboration such as incidents of identical code or copied figures (without attribution) are unacceptable and are liable to be dealt with in a seemingly harsh fashion. The TA's will be asking you about your solutions to make sure you really do understand what you have done. The Final Project is a different story. We do expect you to collaborate, with the course staff and with your fellow students, especially with your lab partner.

### **Schedule**

The schedule of the lectures and assignments is in this packet. The schedule of the lectures and assignments is posted (and will be updated regularly) on the course website. Staying on schedule is very important in this subject, in order to be prepared to do the term project, which is the single most important assignment in 6.111. It will be an enjoyable experience if you are properly prepared.