

Wireless Headphones

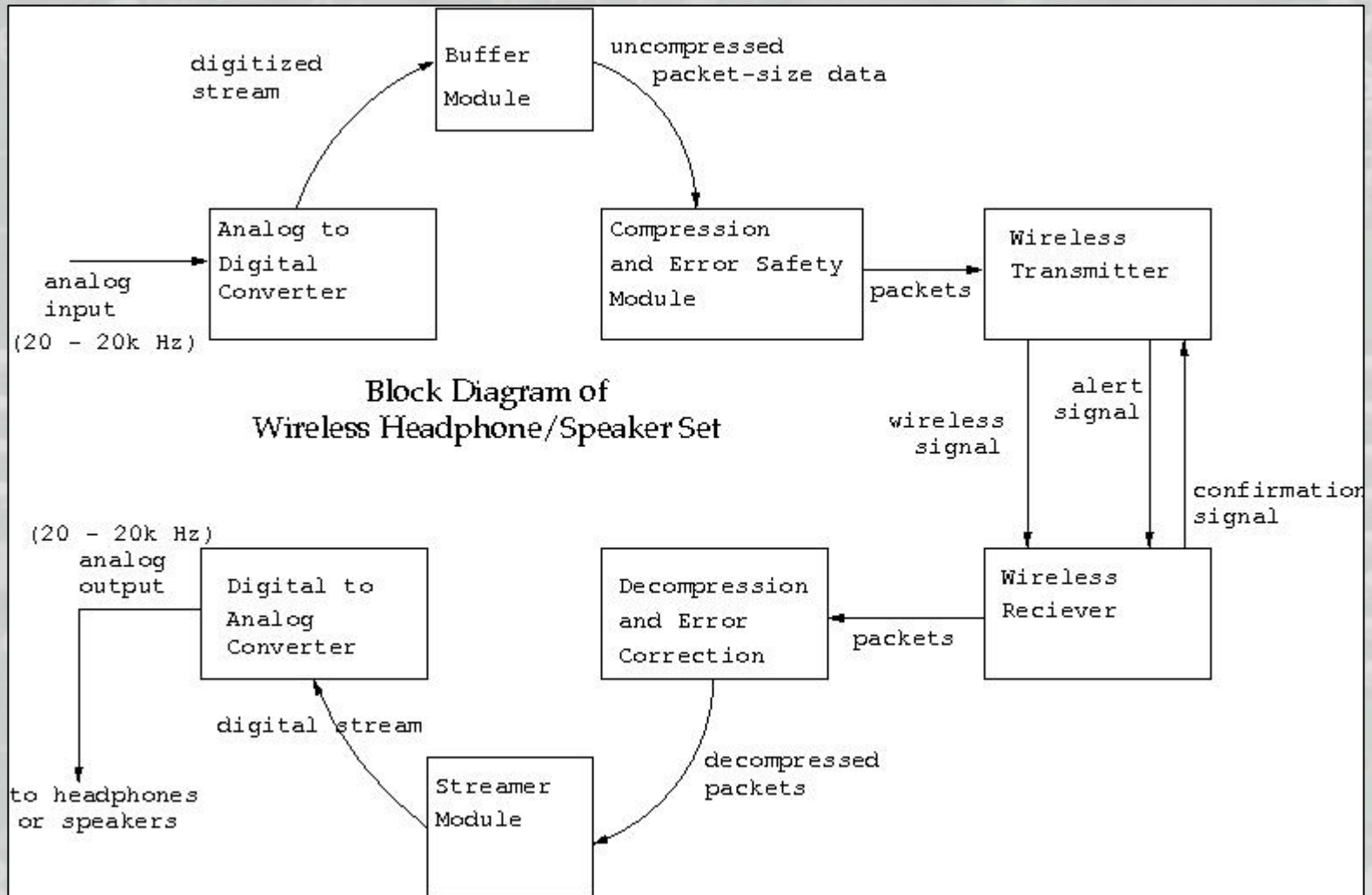
6.111 Final Project

Nivedita Chandrasekaran

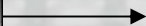
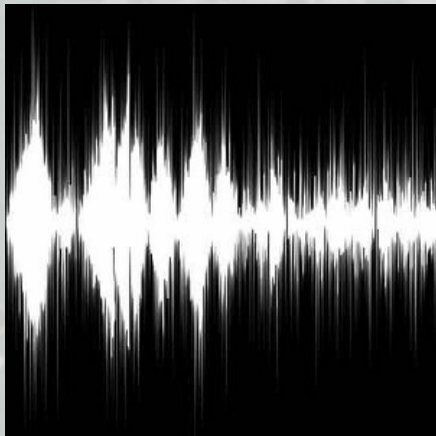
Jessica Nesvold

Aditi Shrikumar

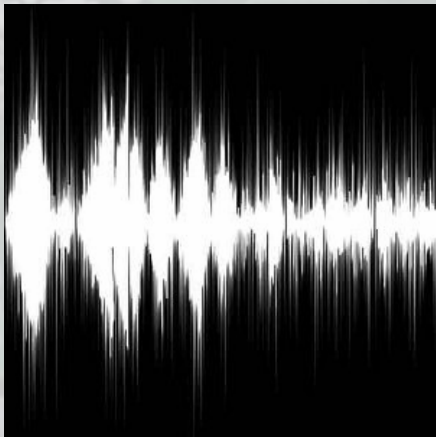
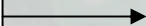
Overview



Analog to Digital...



```
010101011101000101  
01010101010111010101  
0100 Aditi S. 0101  
101010101010101001  
111110101010101010
```



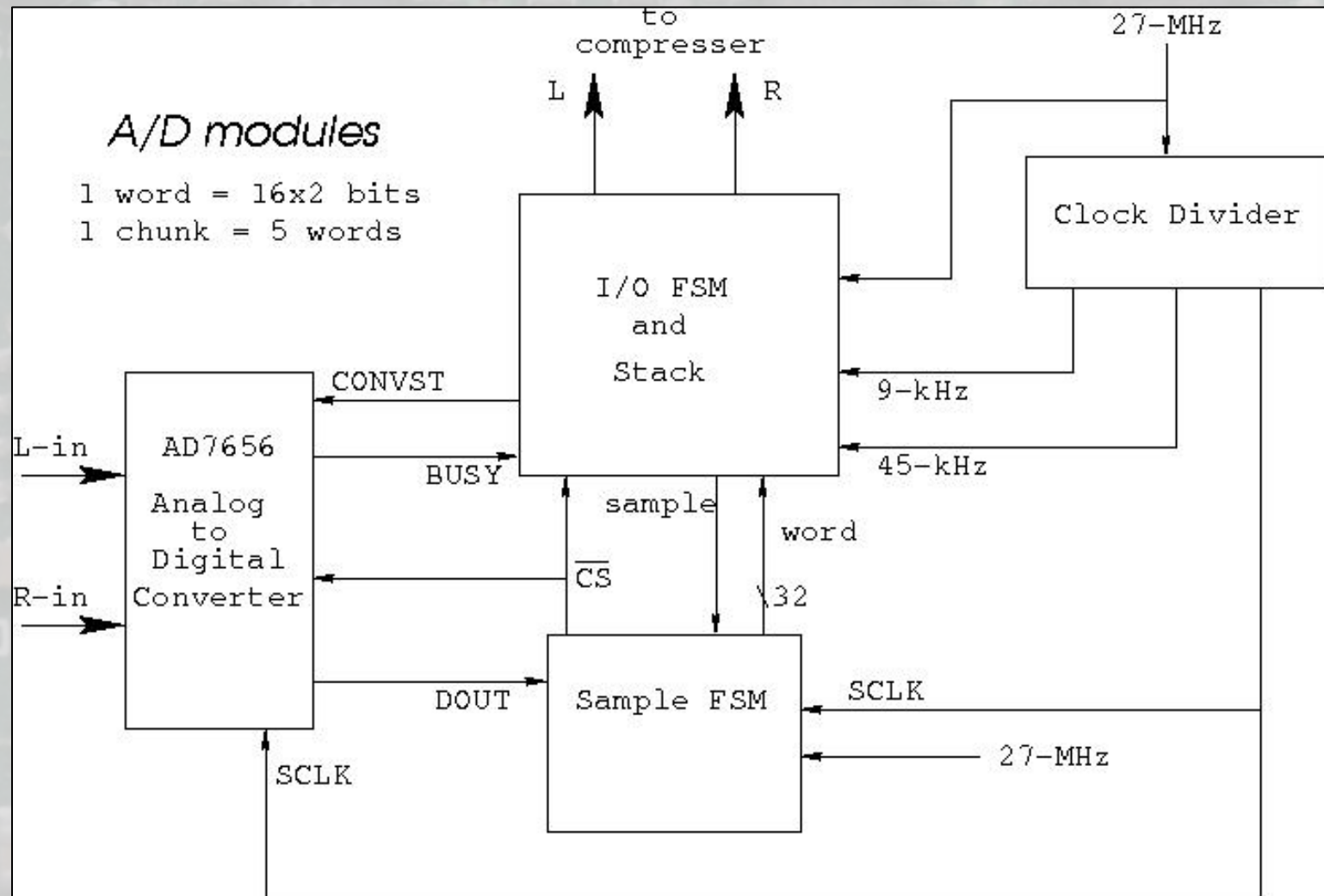
...Digital to Analog

Specifications and Requirements

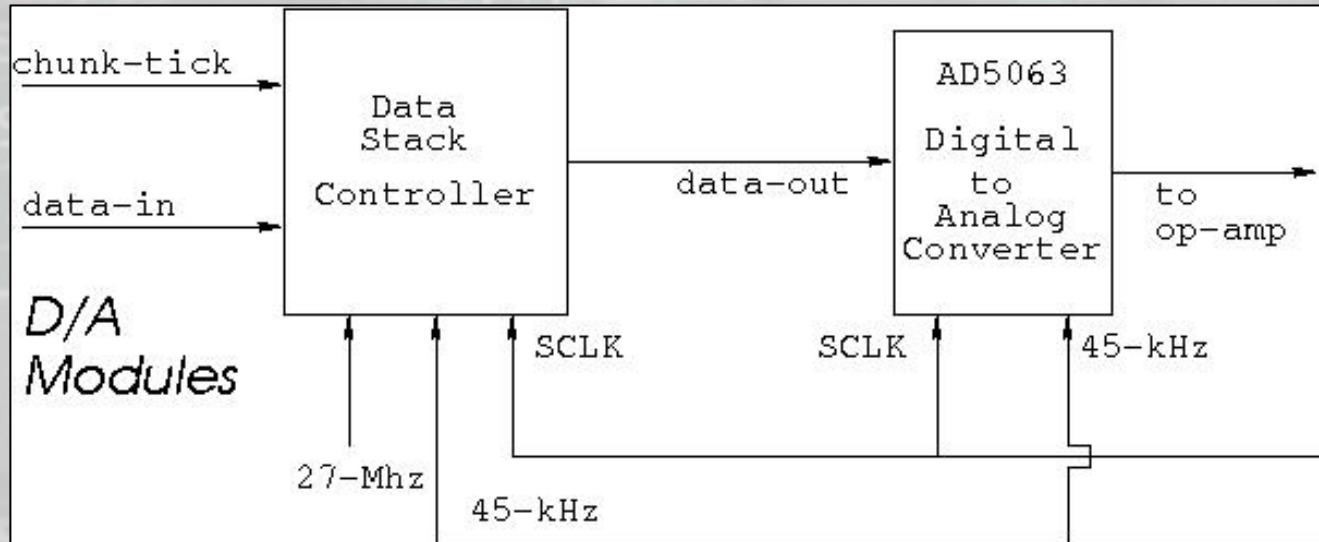


- No aliasing: at least 44-kHz sampling rate
- High resolution: at least 8 bit bits per sample
- Stereo: two samples per sampling period
- Wireless transmission rates: not too many bits per sample

Analog to Digital Conversion



Digital to Analog Conversion





COMPRESSION

DECOMPRESSION

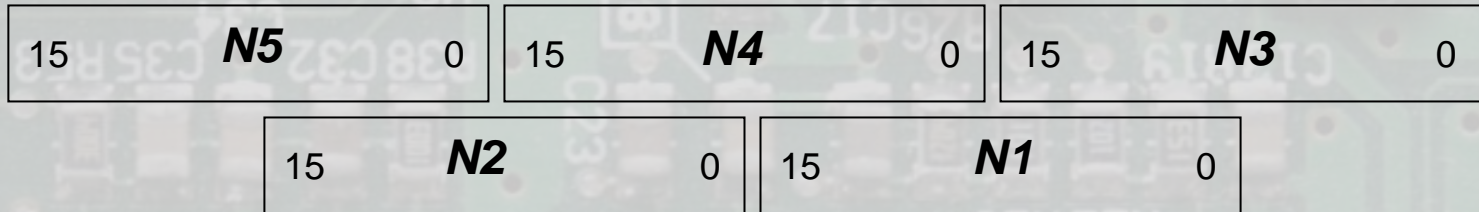


Jessica N.



Codec – Big Picture

80 bits

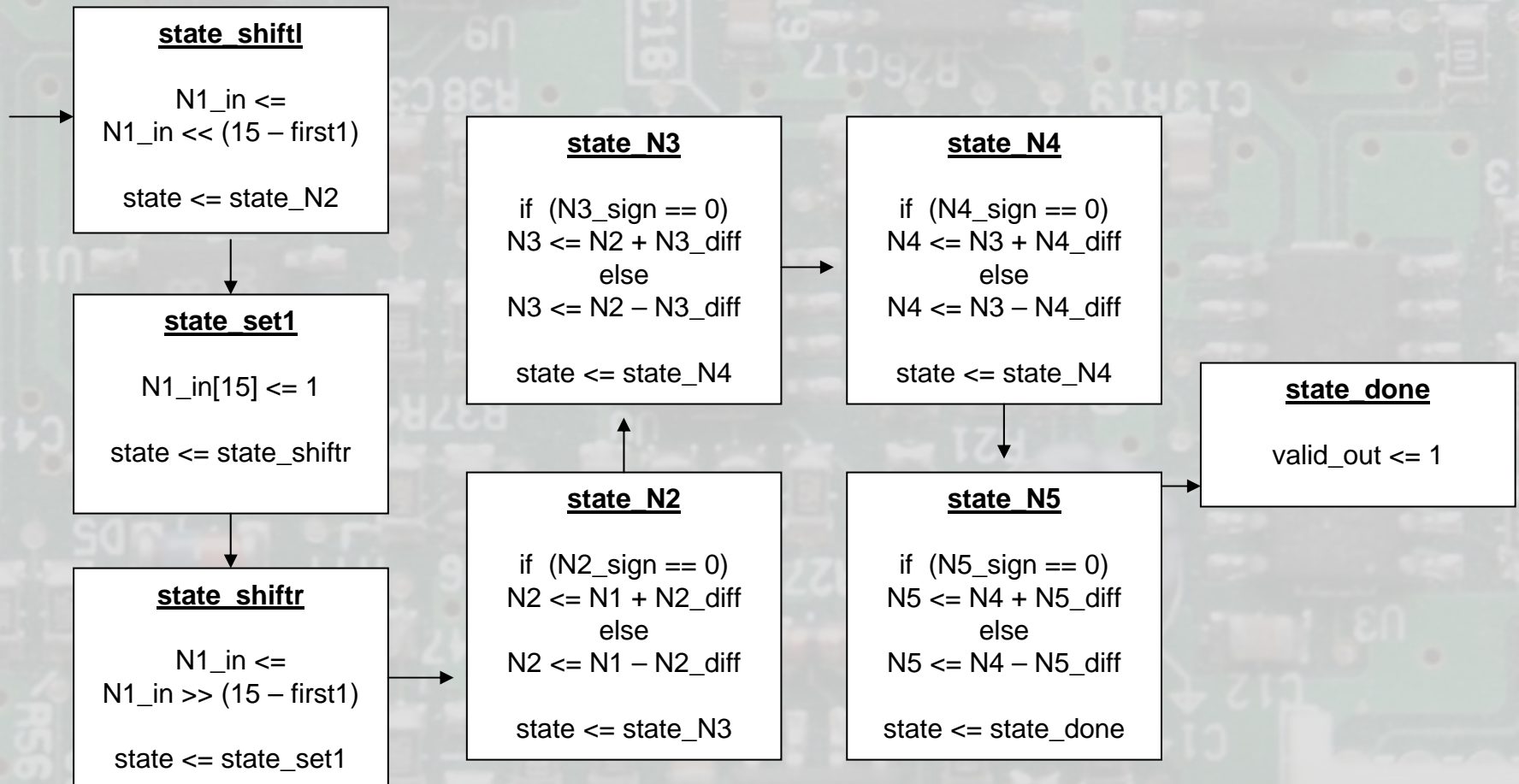


40 bits



COMPRESSION

Decompression



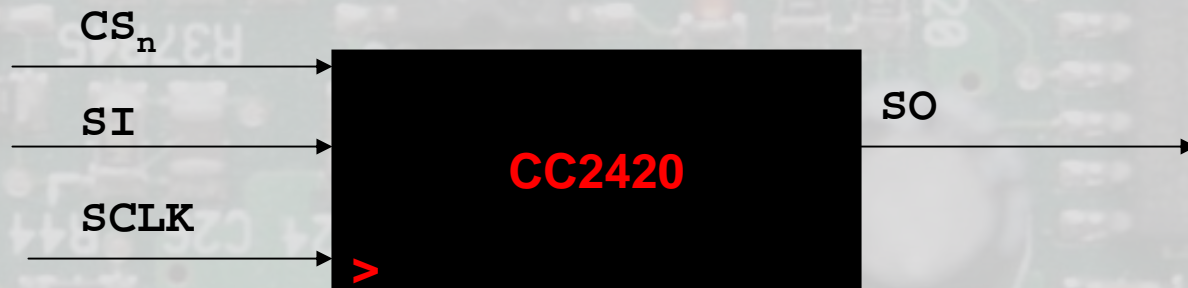
Wireless

Nivedita C.



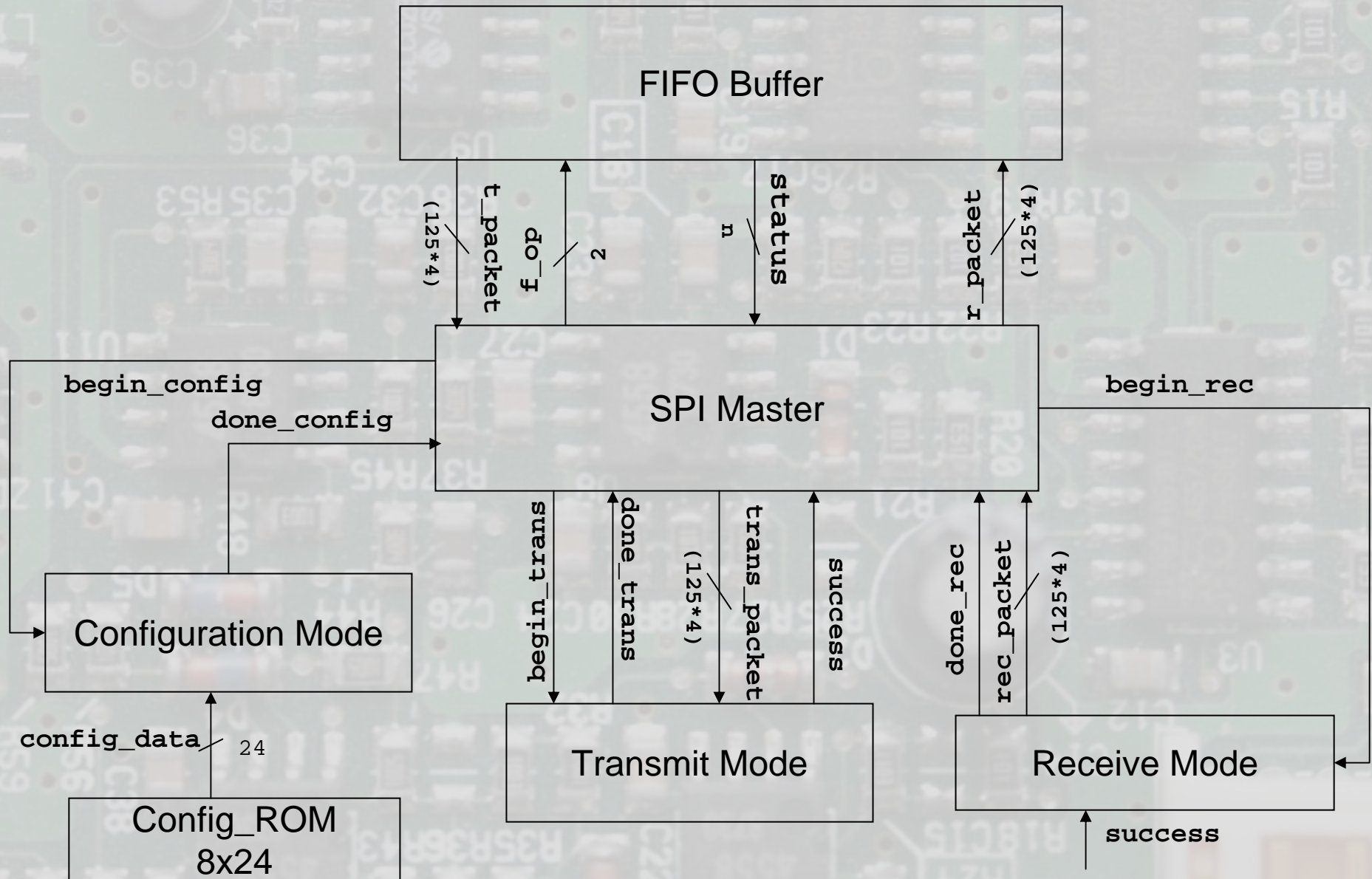
Wireless – Operation, Specifications and Requirements

- Hardware: Two CC2420 transceivers mounted on two evaluation boards
- All communication with chips implemented in Verilog
- Talk to chips via a Serial Peripheral (SPI) interface clocked at 10MHz



- All operations performed by writing or reading from 33 16-bit configuration registers and 15 8-bit command strobe registers

General Transceiver Block Diagram



Implementation Issues

- Data Throughput
 - Chipcon specs: max data rate ~250 kbps
 - Overhead: includes frame check sequences, may have to introduce error correction sequences
 - Assumes uninterrupted transmission
- Memory buffer sizes
 - The lower the data rate, the greater the required size of the buffers
- Dealing with two labkit clocks
 - Need to time interaction of two halves of the system properly
 - Solution: Handshake/acknowledgement protocol between transmitter and receiver

