

Student Name:
TA:
Date Submitted:

Lab 1: Checkoff Sheet

Be prepared to show relevant diagrams as requested in each problem. You may get checked off per problem, rather than the whole lab at once. Collect initials for each problem on this sheet and turn it in with your report.

1. _____

2. _____

3. _____

4. _____

5. _____

6. _____

7. _____

8. _____

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Lab 1: Report Template

This report template is useful to prepare for each exercise's checkoff. Fill in answers for the questions requested by exercise; you may use a different sheet of paper if more convenient, but be sure to follow the template. Be sure to prepare relevant diagrams as requested by each problem. Turn in this report after completing the lab 1 checkoff.

Exercise 1: TTL/CMOS Static Electrical Characteristics

Low Voltage Measurement (In = 1) for 74LS00:

High Voltage Measurement (In = 0) for 74LS00:

Low Voltage Measurement (In = 1) for 74HC00:

High Voltage Measurement (In = 0) for 74HC00:

For each of these measurements, does the output satisfy the ranges specified in the appropriate datasheets? Explain.

What problems could arise from using the LS series with the HC series (at +5V supply)?

Exercise 2: Build your own ring oscillator

Please draw out the waveform showing the output for the 5-inverter oscillator ring. Be sure to label the maximum and minimum voltages, and label the appropriate time intervals.

What is the average TTL inverter propagation delay? Show calculations and briefly explain.

Estimate the period of oscillation for a 3 inverter ring, rather than 5? Explain. What was your measured result?

What happens if you add a long piece of wire to the 3 inverter ring? Explain what causes this to happen.

What is the voltage measurement when you connect the output to the input of a single inverter? What is the significance of this voltage?

Exercise 3: Glitches

What is the width of the glitch measured using the scope and the logic analyzer?

Why does this glitch occur, and what is the lesson learned from this exercise?

Under what conditions is it a bad idea to use a glitchy signal as an input?

Exercise 4: Asynchronous Counters

Please draw a diagram showing the flip-flop arrangement of a typical asynchronous counter, emphasizing the source of each clk input for each flip-flop.

What is your measurement for the clk to MSB delay? From this measurement, show calculations for the clk-to-q delay for a typical flip-flop in the LS393, and explain the derivation.

Exercise 5: Synchronous Counter

Draw a diagram showing the flip-flop arrangement of a typical synchronous counter, emphasizing the source of each clk input for each flip-flop.

How long does it take, after the rising edge of the clock, for one of the flip-flops to change state? Does it matter which output bit you choose? Explain

Show the logic analyzer output to a TA. Can you observe any glitches on RCO? Explain under what circumstance you might expect RCO glitches to occur.

Explain why the RCO and ENT are connected between the two counters, and explain how they work.

What is the difference between the ENT and ENP inputs on a 74LS163?

Explain some differences between the 74LS163 and the 74LS393 in terms of design and performance. How many flip-flops and how much logic is required to implement the counter?

Exercise 6: Set-Reset Latch Construction

Draw your circuit diagram for the SR Latch.

Draw the truth table for the SR Latch.

Explain the functionality of the SR Latch and give an example on how it may be used.

Exercise 7: Setup Time Measurement of a *D Edge-triggered Register*

Explain your solution using relevant diagrams and explanations.

Explain the main sources of error in the measurement technique and potential differences with datasheets.

Exercise 8: Writing Combinational Verilog code

Print out your code for the combinational Verilog code, and be sure to have it ready for checkoff. Draw out the 7 Karnaugh maps corresponding to the different outputs, and generate the minimized equation, that is, either MPS or MSP as appropriate. Write down the equations below each Karnaugh map.

a

	00	01	11	10
00				
01				
11				
10				

b

	00	01	11	10
00				
01				
11				
10				

c

	00	01	11	10
00				
01				
11				
10				

d

	00	01	11	10
00				
01				
11				
10				

e

	00	01	11	10
00				
01				
11				
10				

f

	00	01	11	10
00				
01				
11				
10				

g

	00	01	11	10
00				
01				
11				
10				