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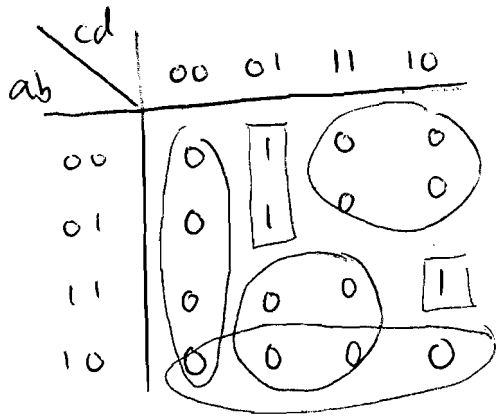
PROBLEM 1

(#1)

a	b	c	d	f
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0



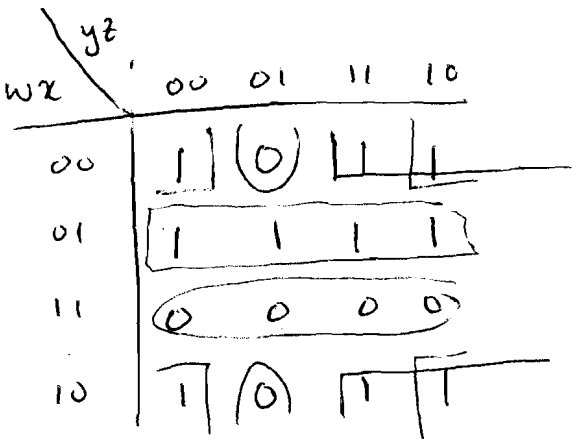
$$SOP = \bar{a} \cdot \bar{c} \cdot d + a \cdot b \cdot c \cdot \bar{d}$$

$$POS = (\bar{a} + \bar{d})(c + d)(\bar{a} + b)(a + \bar{c})$$

#2 $f = \overline{(w+\bar{x})(z\bar{y}+x)} = \overline{(w+\bar{x})} + \overline{(z\bar{y}+x)}$

$= (\bar{w}\cdot x) + ((\bar{z}+y)\cdot\bar{x}) = \bar{w}x + \bar{x}\bar{z} + \bar{x}y$

w	x	y	z	f
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

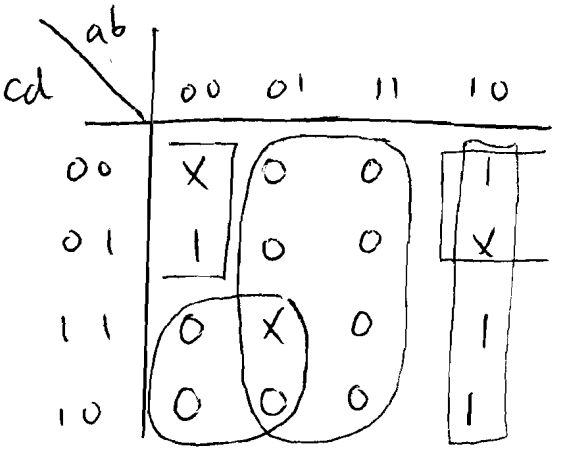


SOP = $\bar{w}x + \bar{x}\bar{z} + \bar{x}y$

POS = $(\bar{w}+\bar{x})(x+y+\bar{z})$

PROBLEM 2

#1



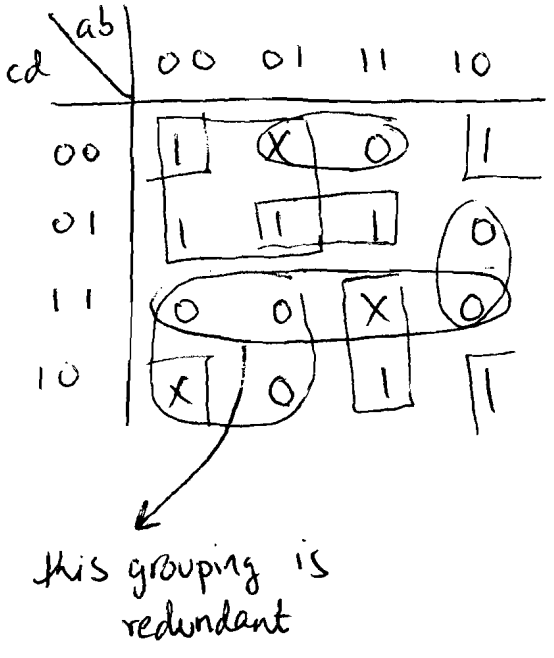
i) min SOP = $a\bar{b} + \bar{c}\bar{b}$

ii) min POS = $\bar{b} \cdot (a + \bar{c})$

iii) Yes

iv) Yes

#2



i) min SOP = $abc + \bar{b}\bar{d} + \bar{a}\bar{c} + b\bar{c}\bar{d}$

ii) min POS = $(c + d + \bar{b})(a + \bar{c})(\bar{a} + b + \bar{d})$

iii) POS is unique, but SOP is not
e.g. $\bar{a}\bar{c} + b\bar{c}d + acd + \bar{b}\bar{d}$

iv) NO

PROBLEM 3

#1 $\overline{\overline{(a+d)}\ \overline{(\bar{b}+c)}} = (a+d) + (\bar{b}+c)$

#2 $\overline{\overline{(a \cdot b \cdot \bar{c})} + \overline{(\bar{c} \cdot d)}} = (a \cdot b \cdot \bar{c}) \cdot (\bar{c} \cdot d)$

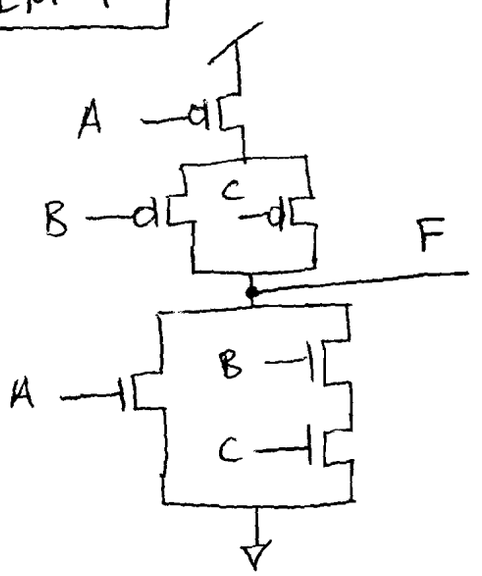
$= a \cdot b \cdot \bar{c} \cdot d$

#3 $\overline{\bar{a}+d} \cdot \overline{b+\bar{c}} \cdot \overline{\bar{c}+d} = (a \cdot \bar{d}) \cdot (\bar{b} \cdot c) \cdot (c \cdot \bar{d})$

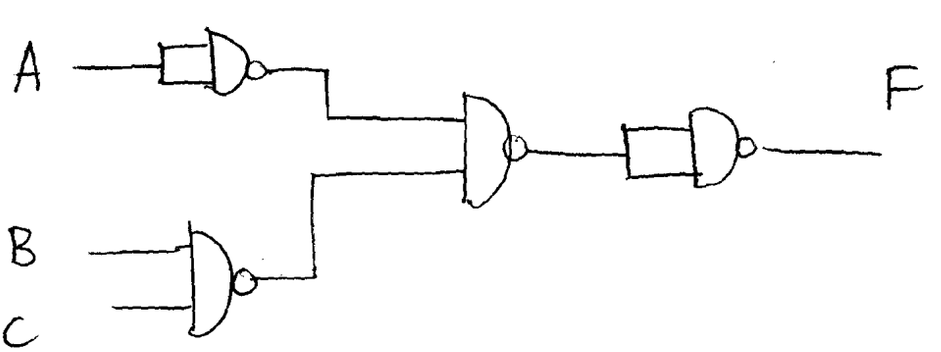
$= a \cdot \bar{b} \cdot c \cdot \bar{d}$

PROBLEM 4

#1



#2



PROBLEM 5

5/5

#1 $t_{setup} = 0$

$t_{hold} = 2\,t_{inv}$ (to ensure stability, we want the signal to propagate through I_1 & I_2 before $\overline{G}$ is asserted).

#2 Master-Slave positive-edge triggered register (or flip flop)

#3 $t_{setup} = 2\,t_{inv}$ (before rising edge of the clk, the data must propagate through both inverters).

$t_{hold} = 0$ (@ rising edge, the inverter feedback loop is stable so no need to hold data)

$t_{c \to q} = 2\,t_{inv}$ (looking @ the second D-flip flop)

Note: since we have a positive-edge triggered register, the timing parameters are calculated with respect to the rising (i.e. low-to-high transition) of the clock.