Lecture 1 - February 4, 2009

Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.111 -- Introductory Digital Systems Laboratory

HANDOUTS are distributed at the lectures. If you don't get them at lecture, you can print them from the course web page, **http://web.mit.edu/6.111/www/s2009.** Extra handouts will be stored for some time in 38-600.

CONTENTS of this first day of class packet:

1. General Information

2. Syllabus

3. Problem Set 1

4. Lab 1 and Lab1 Report Template

5. Safety Memo:
   Read this, sign it and return form as indicated before coming to get your kit.

6. Kit Sign-out Form:
   Read the back and sign it before coming to get your kit. Kits will be available starting at 1:30 PM Thursday (February 5, 2009) from 38-600.

7. 6.111 Information Sheet and Permission Form
   Fill this out NOW and turn it in at the end of this class. You may change your election at a later time this term. We need this form to create computer accounts for the lab.

In addition, Lecture 1 will be provided as a separate handout.

Email questions or problems to 6.111-st09-staff@mit.edu.

Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.111 – Introductory Digital Systems Laboratory (Spring 2009)

General Information

Lecturer
Prof. Akintunde Ibitayo (Tayo) Akinwande, Room 39-553, x8-7974, akinwand@mtl.mit.edu

Course Assistant
Carolyn Collins, Room 39-553, x3-0016, collins@mtl.mit.edu

TAs
Adam Lerer (alerer@MIT.EDU), x3-7350, Rm 38-600)
Chris Celio (celio@MIT.EDU), x3-7350, Rm 38-600)

LAs
Lance Collins (ljcol25@mit.edu), Sam Gross (sgross@mit.edu)

Technical Instructor
Gim P. Hom (gim@mit.edu, Room 38-644, x4-3373)

Recommended Reading (Purchase is NOT required).
Logic Design: Randy Katz, Gaetano Borriello, Contemporary Logic Design, Pearson Education, 2005.
Verilog: Samir Palnitkar, Verilog HDL, Pearson Education (2nd edition).
(Quantum Books, located at 4 Cambridge Center, Kendall Square, Phone: (617) 494-5042, www.quantumbooks.com).

6.111 Homepage http://web.mit.edu/6.111/www/s2009/

Component Pinouts/Data
Pinouts for most components easily available through the web (e.g., do a google search to locate the appropriate data sheet). We will post most of the relevant sheets needed for the labs on the course web site.

Conduct of the Subject (minor changes may be made):

Classes
In the first couple of weeks of the term, there will be lectures on Friday (to quickly ramp up on material needed for lab 1). Then, Fridays will be used for recitations (two parallel recitation sections from 1-2pm). Lectures and recitations are discontinued at the end of the term so you can focus on the final project (see course schedule for details). We will meet in the lecture hall (32-144) for project group presentations after the block diagram conferences. Notification of particulars of the project presentations will be sent by email to 6.111students@mit.edu.

6.111 Lab (Room 38-600)

The laboratory facilities are located on the sixth floor of Building 38. Each student will be issued his/her own Laboratory Kit which includes a proto-board, discrete components, a USB flash drive, oscilloscope probes, logic analyzer pods, wire stripper, chip extraction tool, etc. **The FPGA kits are shared and located on the lab benches**. Please turn-off the power to the kits when you are done using them. In the Digital Systems Laboratory (Room 38-600) you will find logic analyzers and oscilloscopes needed for the lab exercises. Please check the lab hours posted on the website for the hours. The lab will not be staffed by Teaching Assistants (TAs) or Lab Aides (LAs) all of the open hours. The schedule of TAs and LAs will be available on the course web page.

NO FOOD or DRINKS in the lab (38-600)

There are lockers for the safe storage of your kits along the 5th and 6th floor corridors of building 34. Apply at the 6th-floor instrument room desk for one. You should also remember to periodically back up all of your important files (both on Athena and the USB flash drive). When the sixth floor entrance is locked, the alarm system for the lab is usually activated. You are to enter and exit via the 5th floor. If you get stuck in the Lab after closing, you MUST have a TA let you out.

Laboratory Assignments
All laboratory exercises must be completed in order to pass this course and these are intended to prepare you for the term project. In doing these exercises, each student works individually. We strongly recommend that you use a computer-based drawing package to draw block diagrams and schematics for the lab reports and final project.

Problem Sets
Three problem sets will be issued. The problem sets will emphasize the material covered in lectures and recitations and the primary goal is to help you prepare for the labs.

Quiz
There will be one quiz during the term before Drop Date.

Term Project
The most important assignment is the Term Project, about which you will receive more detailed instruction later. In doing this assignment, you will work with one or, at most, two partners. You should begin finding your partner(s) early in the term.

Grading Policy
Late work will be penalized. Lateness of the lab assignments will result in a 20% per day penalty for work completed 1-5 working days after the due date. No point credit will be given for unexcused lateness exceeding 5 days.

The Lab 1 Checkoff sheet is to be initialed by a TA or LA and included with your report. Note that the checkoff sheet is NOT the report. Lab 1 report template is posted on the web site.

Lab 2 report will be used for part of the CIM requirement. More details will be provided in lecture.

Lab 3 will only include the checkoff (which will include some detailed questions related to memory). There is no need to write a detailed lab report for lab3. The lab will have instruction on what is to be turned.

Lab 4 has an intermediate checkoff (not graded) and the final checkoff. There is virtually no modification required to a report depending on the working of your lab implementation. However, reports with no lab effort will receive a zero.

The term project requirements *must* be completed in accordance with the schedule given in the instructions. You must make a presentation of your part of your project to the rest of the class after the logic diagram conference. You must demonstrate (i.e., present) your term project even if it does not fully function, and you must submit the written report in order to receive a passing grade.

The following approximate weights will be used to determine your course grade:

Quiz	10%
Problem Sets (3)	3%
4 Lab Exercises	
Lab 1 (check-off, report)	9%
Lab 2 (check-off, report)	10%
Lab 3 (check-off, no report)	8%
Lab 4 (check-off, report)	11%
Writing (Lab 2 revised report - part of CIM requirement)	10%
Class participation (lectures, recitations, project presentations)	3%
Final Project	36%

We construct a histogram of these summary numbers and proceed to discuss individual performances of all students. Some of the factors considered are:

1. Completion of labs. Past history has been that it is rare for a student to receive an A without completing the labs. All labs must be completed in order to pass the course even when no credit is awarded due to lateness.

2. Project performance.

    a) Any student who does not turn in a final project report will receive an F.
    b) Students who do not construct a project will receive an F.
    c) Project complexity is an important factor in discriminating between an A and a B. An A is rarely given if the final project is not as complicated as lab 4.
    d) **It is extremely difficult for a student to receive an A without completing the final project.** Of course, it is possible to get a grade lower than an A even if the final project is completed.

Although 6.111 has a significant classroom component, it is *primarily* a lab subject. Accomplishments in the lab tend to be weighted more heavily than other components. The classroom component is viewed as supportive of the lab components. Some material covered in lectures will be related to advanced topics (power dissipation, mapping to ASICs, testing, etc.). Some the concepts might not be applicable to your final project but are important emerging digital system issues in industry today.

Traditionally, both average grade levels and average performance have been quite high in 6.111. A large number of students do “A” level work and are, indeed, rewarded with a grade of A. The corollary to this is that, since average performance levels are so high, punting any part of the subject, can lead to a disappointing grade. It is important that you keep up with the work.

Finally, and unfortunately, it is important for us to outline our expectations for academic honesty in 6.111. We do this not because we expect any of you to be dishonest, nor to insult your intelligence or character, but to avoid any misunderstandings.

First, the quiz is to be an individual effort. The problem sets and lab exercises are also to be individual efforts; however, it is okay to ask questions, get help from us, fellow students, or anyone else. But then, do them by yourself. Indications of collaboration such as incidents of identical code or copied figures (without attribution) are unacceptable and are liable to be dealt with in a seemingly harsh fashion. The TA's will be asking you about your solutions to make sure you really do understand what you have done. The Final Project is a different story. We do expect you to collaborate, with the course staff and with your fellow students, especially with your lab partner.

Schedule

The schedule of the lectures and assignments is in this packet. The schedule of the lectures and assignments is posted (and will be updated regularly) on the course website. Staying on schedule is very important in this subject, in order to be prepared to do the term project, which is the single most important assignment in 6.111. It will be an enjoyable experience if you are properly prepared.

Preliminary Course Schedule (updated 1/26/09) - see website for updates

Monday	Wednesday	Friday
February 2 ***Registration Day***	**February 4** **L1: Introduction** (PDF) Course objectives, digital logic, hardware description languages, Process Technology **Lab 1 handed out** **Problem Set 1 handed out**	**February 6** **L2: Combinational Logic (PDF)** Logic gates, Boolean algebra, visualizations of Boolean algebra, hazards **Hands-on Logic Analyzer Tutorial by TAs and Gim Hom (in the 6.111 lab) , February 5-8**
February 9 **L3: Introduction to Verilog- Combinational Logic (PDF)** Logic synthesis, the Verilog hardware description language, combinational logic in Verilog, testbenches	**February 11** **L4: Sequential Building Blocks** (PDF) Preserving state with feedback, latches and flip-flops, clocks and timing constraints, clock skew	**February 13** **L5: Simple Sequential Circuits and Verilog** (PDF) Simple counters, Verilog implementation of Sequential Circuit. **Hands-on Tutorial by TAs and Gim Hom (in the 6.111 Lab): ModelSim, Labkit, February 12-15**
February 16 - No Class **February 17 - Monday Schedule of Classes Held on 2/17 (Tuesday)** **L6: Finite-State Machines and Synchronization** (PDF) Metastability and synchronization, Mealy and Moore formalisms, Verilog implementations, FSM examples **Problem Set 1 Due** **Problem Set 2 handed out**	**February 18** **L7: Memory Basics and Timing** (PDF) Technologies, types of RAM and ROM, memory controller circuits, specialty memories, high-performance interfaces **Lab 1 Checkoff and Report due by 1PM (turn in report at lecture, 32-144)** **Lab 2 (Auto Alarm FSM) handed out**	**February 20** **Recitation (36-112, 36-144, 36-155)** ***FSM Examples, Verilog Lab 2 Discussion***
February 23 **Finish Memory** **L8: Arithmetic Structures** (PDF)	**February 25** **L9: Arithmetic Structures** (cont.) Binary addition and subtraction,	**February 27** **Recitation (36-112, 36-144, 36-155)** ***More FSM, Memory, Arithmetic*** **Problem Set 2 Due**

Binary addition and subtraction, implementation and performance of the full adder, high-speed addition, signed arithmetic	implementation and performance of the full adder, high-speed addition, signed arithmetic CI-M requirements (Lab2 report guidelines)	**Problem Set 3 handed out**
March 2 **L10: Analog Building Blocks** (PDF) Analog inputs, useful op-amp circuits, A/D and D/A conversion, useful A/D and D/A circuits --- **Lab 2 Checkoff**	**March 4** **Finish Analog Building Blocks** **L11: System Integration Issues and Major/Minor FSM** (PDF) Hierarchy and modularity, data and control paths, major and minor FSMs --- **Lab 2 Report Due in Lecture (32-144)** **Lab 3 (Memory Tester) handed out**	**March 6** **Recitation (36-112, 36-144, 36-155)** ***VGA Timing Generation*** **(PDF),** ***Block RAM/ROM*** (PDF) ***Lab 3 Discussion***
March 9 **L12: Reconfigurable Logic Architecture** (PDF) Overview of commercial devices, programmable logic (PAL), FPGA Architectures, and software tools	**March 11** **L13: Video** (PDF) **Problem Set 3 Due** **Lab 3 (Memory Tester) checkoff (Thursday March 12) - No detailed report due (see lab for details)**	**March 13** **Quiz Review by TAs (32-144)** **Lab 4 (Pong Game) handed out**
March 16 No Class on March 17 **6.111 Quiz on March 17th (Tuesday)** **Location: 32-155** **From 7:30PM-9:30PM**	**March 18** **L14: Project Kickoff** (PDF) Video of past 6.111 projects, project ideas, deadlines and goals, project guidelines, grading, asynchronous interfaces --- **Formation of Project Teams**	**March 20** **No Recitation** --- **Lab 4 Intermediate Checkoff (not graded)**
March 23-27 ***Spring Break***		

March 30 **L15: LSI Integration and Performance Transformations** (PDF) Moore's Law, VLSI integration, layout and fabrication, application-specific circuits, microprocessors. Behavioral and algorithmic transformations, retiming, parallelism and pipelining	**April 1** **L16: Power Dissipation in Digital Systems (PDF)** Heat and battery life issues, sources of power dissipation, circuit and algorithm optimizations for power, voltage scaling **Lab 4 Check Off (Thursday April 2)**	**April 3** **No More Lectures or Recitation**
April 6 *No Lecture* **Project Abstracts Due** **Lab 4 Report Due** **(both by 1PM in 39-553)**	**April 8** *No Lecture* **Proposal Conference with TAs (April 8-10). Bring Project Proposals for the Proposal Conference**	**April 10** *No Lecture* **Lab 2 revised report due (part of CIM)** **Proposal Conference with TAs (April 8-10). Bring Project Proposals for the Proposal Conference**
April 13 **Block Diagram Conference With TAs** *No Lecture*	**April 15** **Block Diagram Conference With TAs** *No Lecture*	**April 17** **Block Diagram Conference With TAs** *No Lecture*
April 20 **Patriots Day (Holiday)**	**April 22** **Project Design Presentation in 32-144**	**April 24** **Project Design Presentation in 32-144**
April 27 **Project Design Presentation in 32-144** **Customized Project Checklist Due** **(groups + staff)**	**April 29** **Implement/Debug - Milestone 1** *No Lecture*	**May 1** **Implement/Debug - Milestone 1** *No Lecture*
May 4 **Implement/Debug - Milestone 2** *No Lecture*	**May 6** **Implement/Debug - Milestone 2** *No Lecture*	**May 8** **Implement/Debug - Milestone 2** *No Lecture*
May 11 **Implement/Debug** *No Lecture*	**May 12/13/14 (Tu/W/Th)** **May 12: Final Project Check-off with TA** **May 13: Demo and Video Taping** **May 15: Final Project Report Due by 5PM (electronic to the**	**May 15**

	TA)	

Massachusetts Institute of Technology

Department of Electrical Engineering and Computer Science
6.111 - Introductory Digital Systems Laboratory

Problem Set 1

Issued: February 4, 2009 **Due**: February 17, 2009

Boolean Algebra Practice Problems (do not turn in):

Simplify each expression by algebraic manipulation. Try to recognize when it is appropriate to transform to the dual, simplify, and re-transform (e.g. no. 6). Try doing the problems before looking at the solutions which are at the end of this problem set.

1) $a + 0 =$ _____

2) $\bar{a} \cdot 0 =$ _____

3) $a + \bar{a} =$ _____

4) $a + a =$ _____

5) $a + ab =$ _____

6) $a + \bar{a}b =$ _____

7) $a(\bar{a} + b) =$ _____

8) $ab + \bar{a}b =$ _____

9) $(\bar{a} + \bar{b})(\bar{a} + b) =$ _____

10) $a(a + b + c + ...) =$ _____

For (11),(12), (13), $f(a,b,c) = a + b + c$

11) $f(a,b,ab) =$ _____

12) $f(a,b,\bar{a} \cdot \bar{b}) =$ _____

13) $f[a,b,\overline{(ab)}] =$ _____

14) $y + y\bar{y} =$ _____

15) $xy + x\bar{y} =$ _____

16) $\bar{x} + y\bar{x} =$ _____

17) $(w + \bar{x} + y + \bar{z})y =$ _____

18) $(x + \bar{y})(x + y) =$ _____

19) $w + [w + (wx)] =$ _____

20) $x[x + (xy)] =$ _____

21) $\overline{(\bar{x} + \bar{x})} =$ _____

22) $\overline{(x + \bar{x})} =$ _____

23) $w + (w\bar{x}yz) =$ _____

24) $\bar{w} \cdot \overline{(wxyz)} =$ _____

25) $xz + \bar{x}y + zy =$ _____

26) $(x + z)(\bar{x} + y)(z + y) =$ _____

27) $\bar{x} + \bar{y} + xy\bar{z} =$ _____

Problem 1: Karnaugh Maps and Minimal Expressions

For each of the following Boolean expressions, give:

i) The truth table,
ii) The Karnaugh map,
iii) The minimal sum of products expression. (Show groupings)
iv) The minimal product of sums expression. (Show groupings)

1) $(\bar{a} + b \cdot \bar{d}) \cdot (c \cdot b \cdot a + \bar{c} \cdot d)$

2) $\overline{(w + \bar{x})(z\bar{y} + x)}$

Problem 2: Karnaugh Maps with "Don't Cares"

Karnaugh Maps are useful for finding minimal implementations of Boolean expressions with only a few variables. However, they can be a little tricky when "don't cares" (X) are involved. Using the following K-Maps:

cd \ ab	00	01	11	10
00	X	0	0	1
01	1	0	0	X
11	0	X	0	1
10	0	0	0	1

(1)

cd \ ab	00	01	11	10
00	1	X	0	1
01	1	1	1	0
11	0	0	X	0
10	X	0	1	1

(2)

i) Find the minimal sum of products expression. Show your groupings.
ii) Find the minimal product of sums expression. Show your groupings.
iii) Are your solutions unique? If not, list and show the other minimal expressions.
iv) Does the MPS = MSP?

Problem 3: DeMorgan's Theorem

Use DeMorgan's Theorems to simplify the following expressions:

1) $\overline{\overline{(a+d)} \cdot \overline{(\overline{b}+c)}}$

2) $\overline{\overline{(a \cdot b \cdot \overline{c})} + \overline{(\overline{c} \cdot d)}}$

3) $\overline{\overline{a}+d} \cdot \overline{b+\overline{c}} \cdot \overline{\overline{c}+d}$

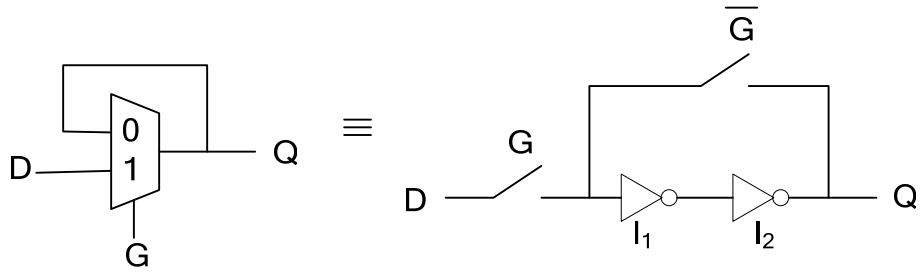
Problem 4: Transistor/Gate Level Synthesis

1) Construct a transistor level circuit with inputs *A*, *B*, and *C*, and output *F* of the following function using NMOS and PMOS devices: $F = \overline{A + B \cdot C}$

2) Construct a gate level circuit of the same function with inputs *A*, *B*, and *C*, and output *F* only using NAND gates.

Problem 5: Setup and Hold Times for D Flip-Flop *(Flip-flops will be covered in lecture 4)*

1) Let a D latch be implemented using a mux and realized as follows:

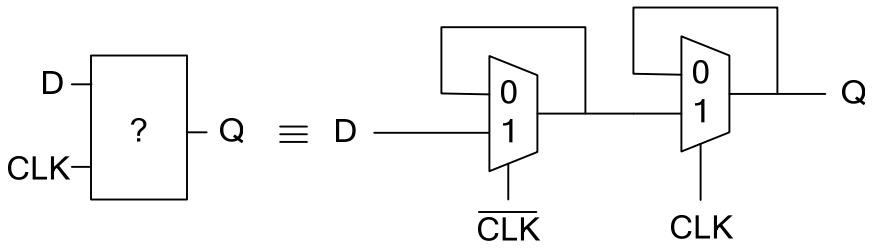


You may assume the following:

a) G and $\overline{G}$ are complements and have zero skew, i.e. when G is 1, $\overline{G}$ is exactly 0, and vice versa.
b) Assume the switches are ideal, with no delay. E.g. when G is 0, the switch is open.
c) The propagation delay of the inverters is t_{inv} (assume that the contamination delay or minimum delay is equal to the propagation delay).

What is the setup and hold time of this latch?

2) What memory element is created when two muxes are cascaded as in the figure below? Assume that CLK and $\overline{CLK}$ are complements with zero skew.



3) What is the setup time, hold time, and clock to Q delay of the above memory element?

Solutions to the Boolean Algebra Practice Problems

1) $a + 0 = a$
2) $\bar{a} \cdot 0 = 0$
3) $a + \bar{a} = 1$
4) $a + a = a$
5) $a + ab = a(1 + b) = a$
6) $a + \bar{a}b = (a + \bar{a})(a + b) = a + b$
7) $a(\bar{a} + b) = a\bar{a} + ab = ab$
8) $ab + \bar{a}b = b(a + \bar{a}) = b$
9) $(\bar{a} + \bar{b})(\bar{a} + b) = \bar{a}\bar{a} + \bar{a}b + \bar{b}\bar{a} + \bar{b}b = \bar{a} + \bar{a}b + \bar{a}\bar{b} = \bar{a}(1 + b + \bar{b}) = \bar{a}$
10) $a(a + b + c + ...) = aa + ab + ac + ... = a + ab + ac + ... = a$
11) $f(a, b, ab) = a + b + ab = a + b$
12) $f(a, b, \bar{a} \cdot \bar{b}) = a + b + \bar{a}\bar{b} = a + b + \bar{a} = 1$
13) $f[a, b, \overline{(ab)}] = a + b + \overline{(ab)} = a + b + \bar{a} + \bar{b} = 1$
14) $y + y\bar{y} = y$
15) $xy + x\bar{y} = x(y + \bar{y}) = x$
16) $\bar{x} + y\bar{x} = \bar{x}(1 + y) = \bar{x}$
17) $(w + \bar{x} + y + \bar{z})y = y$
18) $(x + \bar{y})(x + y) = x$
19) $w + [w + (wx)] = w$
20) $x[x + (xy)] = x$
21) $\overline{(\bar{x} + \bar{x})} = x$
22) $\overline{(x + \bar{x})} = 0$
23) $w + (w\bar{x}yz) = w(1 + \bar{x}yz) = w$
24) $\bar{w} \cdot \overline{(wxyz)} = \bar{w}(\bar{w} + \bar{x} + \bar{y} + \bar{z}) = \bar{w}$
25) $xz + \bar{x}y + zy = xz + \bar{x}y$
26) $(x + z)(\bar{x} + y)(z + y) = (x + z)(\bar{x} + y) = xy + \bar{x}z$
27) $\bar{x} + \bar{y} + xy\bar{z} = \bar{x} + \bar{y} + \bar{z}$

Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science
6.111 - Introductory Digital Systems Laboratory (Spring 2009)

Laboratory 1 - Introduction to Digital Electronics and Lab Equipment (Logic Analyzers, Digital Oscilloscope, and FPGA-based Labkit)

Issued: February 4, 2009
Checkoff and Report Due in Class (1PM) on: February 18, 2009

Introduction

This lab assignment introduces you to important tools and devices that we will be using throughout the term. You will be introduced to the following:

- Logic analyzer and digital scope.
- 74LS TTL series chips, including the ‘00, ‘04, ‘163, ‘393, ‘74
- 74HC00, a CMOS NAND gate
- 1.8432 MHz Crystal Oscillator
- TTL and CMOS voltage levels
- Karnaugh Maps and Boolean Algebra
- Latches and Flip-flops, Simple Sequential and Asynchronous circuits
- Simple Verilog
- ModelSim (Verilog simulator), Xilinx FPGA labkit, Xilinx programming software

The following are relevant handouts that you should be using in conjunction with this lab:

- Lectures 1-5
- Safety Memo

Procedure

This lab is divided into several exercises to guide you through the design, construction, and debugging process. You will be asked to wire circuits for many of the exercises. Save all of these circuits until you have completed the lab as many of these circuits might be reused in subsequent parts of this lab.

1. Read and understand the whole assignment.
2. Design, build, test, debug, and fix each exercise in turn. Be sure to answer all the questions in the report template before you get checked off. You do NOT have to get checked-off on a exercise before proceeding to the next one. For each exercise, be sure to have the appropriate figures ready. Turn in the completed report template after your checkoff.
3. **Do not use the power supply from the labkit to power the external proto board. Use the bench power supply. Problems 1-7 should not use the FPGA labkit and should be done on the external breadboard.**

Exercise 1: TTL/CMOS Static DC Characteristics

The logic values of 1 and 0 are represented by voltage levels in the hardware implementation. The voltage levels and other electrical characteristics are not standardized from one logic family to another. 6.111 will use both TTL (Transistor-Transistor Logic) and CMOS (Complementary Metal-Oxide Semiconductor) logic. The voltage ranges for the two logic families are different.

In this exercise, you will first measure the electrical characteristics of a TTL and CMOS gate using the circuit in Figure 1. Wire up this circuit using a 74LS00 part. Do not forget to wire power and ground! These connections are usually omitted from logic diagrams, as the power and ground of the 74LS series are generally the top-right and bottom-left pin, respectively. Typically, the top of the chip has a small semi-circular cutout, or a white dot next to pin 1.

Ground the input of the inverter (the first NAND) and measure the output voltage using the oscilloscope. Be sure to be using the voltage markers on the oscilloscope. Connect the input to a logic '1' and repeat the measurement.

Figure 1: (a) Logic Level Measurement (Measure voltage at *OUT* node).
(b) Power Supply Wiring.

Next, use a 74HC00 and wire up the same circuit and hook V_{CC} to a +5V supply. Perform the same measurements and record your results.

Look up the valid input and output voltage ranges using the datasheet for a 74LS00 and a 74HC00. For each experiment, do your output values satisfy the range specified in the datasheets?

Consider interfacing a TTL inverter to a CMOS inverter and vice versa. Look at the datasheet titled "HCMOS Family Characteristics". Based on the +5V supply you used, find out the recommended input voltage for HCMOS inputs. Discuss potential issues when interfacing TTL and CMOS components? Run the two experiments (interface TTL to CMOS and vice versa) and make voltage measurements.

Exercise 2: Build Your Own Ring Oscillator

Important timing parameters associated with the speed of digital logic gates are the propagation delay time t_{PD}, and the output signal rise and fall times, t_r and t_f. Propagation delay is a measure of how much time is required for a signal to change state. It is measured as the time from the 50% point of the input to the 50% point of the output (Figure 2). It is often cited as the average of the high-to-low and low-to-high delays (corresponding to the two transitions). The rise and fall times represent the amount of time for a signal to change state. To measure rise and fall times, you should be using the 10% to the 90% point, or vice versa.

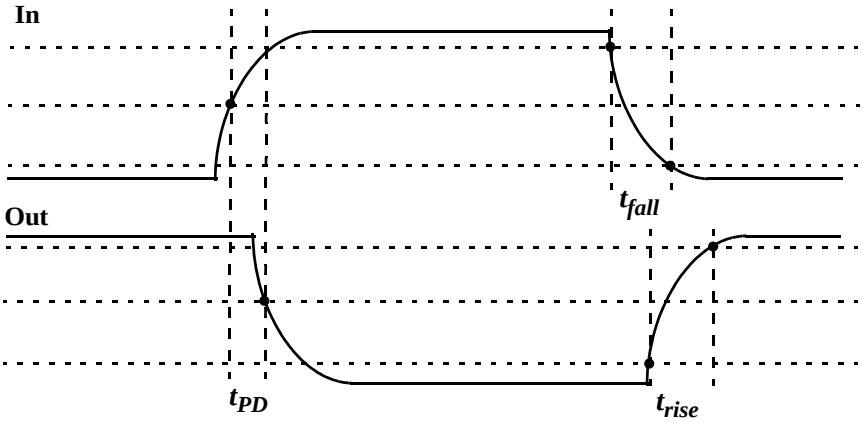


Figure 2: Timing Characteristics (10%, 50%, 90% marked).

Construct the ring oscillator shown in Figure 3 using a 74LS04 with as little wire as possible. From this circuit, determine the average propagation delay of a TTL inverter by measuring the period of oscillation by using the time markers on the oscilloscope. You can determine this by determining the number of gates a signal must travel through to complete a full period of oscillation.

What should the period of oscillation be with 3 inverters in the ring? Rewire the circuit and measure the period. Comment on the new result.

Insert a long piece of wire (about 3 feet) into the ring of 3 inverters. Observe how this extra length of circuit affects the signal. Can you explain the change?

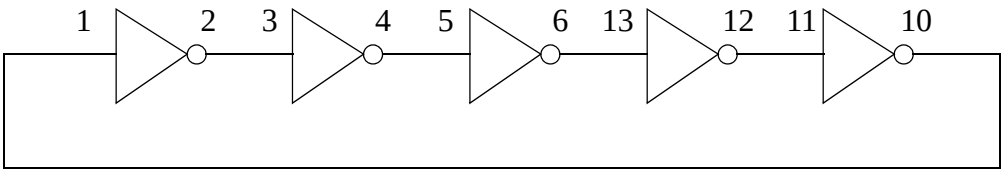


Figure 3: Ring Oscillator (using a 74LS04).

Finally, take a single inverter, and wire the output to the input. The voltage should be stable. If it isn't, connect a capacitor (0.01 μF) between this single node and ground to stabilize the voltage. Measure the voltage, and explain the significance of this voltage.

Exercise 3: Glitches

Wire up the circuit in Figure 4 using a 1.8432 MHz crystal oscillator and a 74LS00. Be sure to wire the crystal oscillator right side up. Pin 1 should be marked with a dot. The output *GLITCH* is a purposely glitchy output caused by the circuit. Using the oscilloscope, measure the width of the glitch.

Next, add *CLK* and *GLITCH* as signals to the logic analyzer and measure the width of the glitch (please refer to http://web.mit.edu/6.111/www/s2008/handouts/quick_la.html for a quick introduction to the logic analyzer). Is there a significant difference between your two different types of measurements? Why does this glitch occur, and what is the lesson learned from this exercise? Under what conditions is it a bad idea to use a glitchy signal as an input?

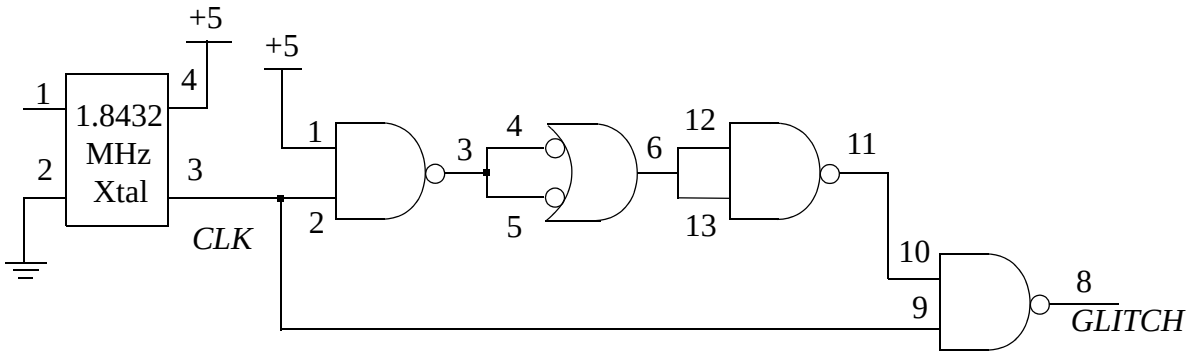


Figure 4: Glitch Measurement Circuit (74LS00).

Exercise 4: Asynchronous Counters

Wire up the 1.8432 MHz clock from the previous exercise to an 8-bit ripple counter as shown in Figure 5. You do not need to disconnect the previous circuit. In this exercise, we are concerned with how each output bit changes with respect to other bits. Since this counter increments its count every falling edge of the clock, each output bit must have a period twice that of the next significant bit. Because of this characteristic, counters make good clock dividers; if you want a slower frequency clock, it may be helpful to use a counter or a series of counters. Verify the counter's operation using the oscilloscope.

Trigger on either a rising or falling edge of the MSB, and measure the time between the falling-edge of *CLK* to edge of the MSB. Estimate the clk-to-q delay for each flip-flop in this chip.

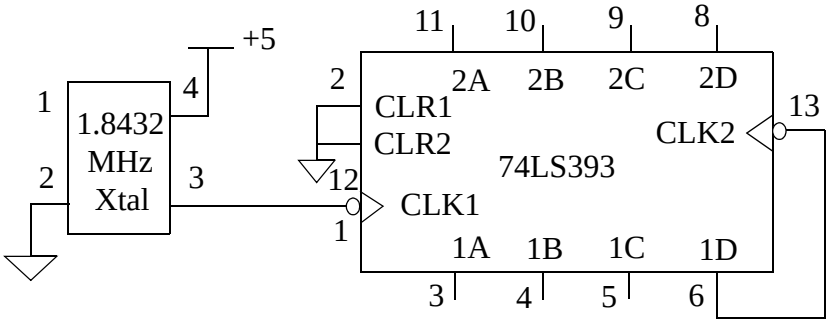


Figure 5: Clock and Ripple Counter.

Exercise 5: Synchronous Counter

One of the most useful of the 74LS series is the 74LS163. This is a 4-bit loadable synchronous counter with a synchronous reset. Wire two 74LS163s so that they count continuously as shown in Figure 6. Trigger your scope on the most significant bit (MSB) and verify its operation.

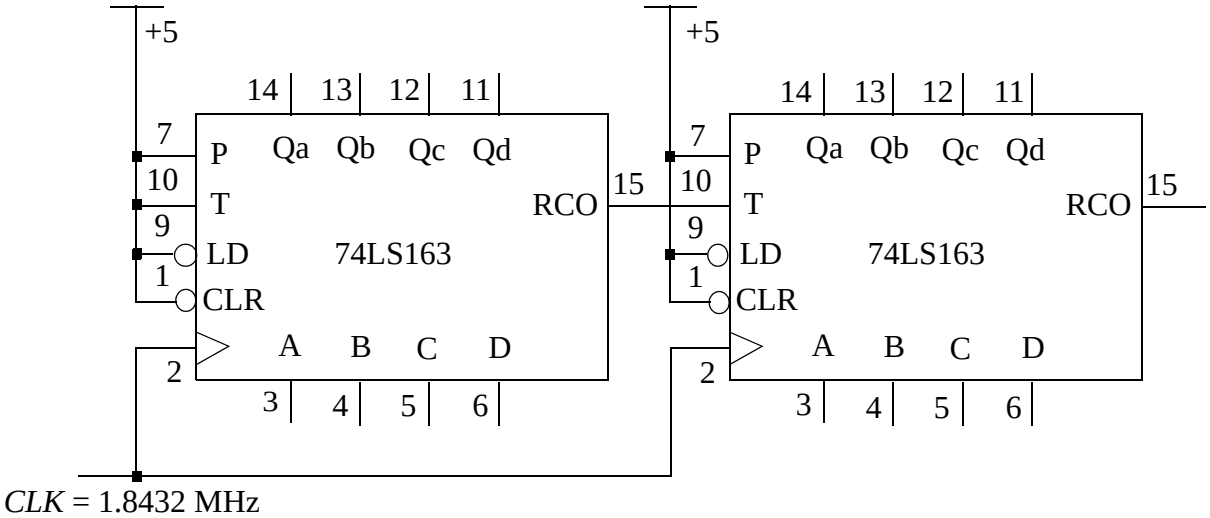
Explain why the *RCO* and *ENT* are connected between the two counters, and explain how they work. What is the difference between the *ENT* and *ENP* inputs on a 74LS163?

How long does it take, after the rising edge of the clock, for one of the flip-flops to change state? You should be triggering the oscilloscope on an appropriate output bit. Does it matter which output bit you choose?

Use the logic analyzer to capture the Q_A, Q_B, Q_C, Q_D and *RCO* outputs of the *low-order* counter. Display the values of *A*, *B*, *C* and *D* as a 4-bit hex number. For a quick introduction to the logic analyzer, please refer to http://web.mit.edu/6.111/www/s2008/handouts/quick_la.html.

Look at the *RCO* output of the *low-order* counter. Use the "Glitch Trigger" feature of the logic analyzer to see if you can locate any *RCO* glitches. Do you observe any glitches on the carry output? Glitches like these are hard to see as they are very short. The carry output does not always have glitches, just sometimes for particular chips. Try using the oscilloscope as well to look for glitches.

Be prepared to comment on the difference between the 74LS163 and the 74LS393 in terms of design and performance; in particular, the speed and area of the device. By area, we are asking you to consider how complicated it is to implement the counter. How many flip-flops and how much logic is required to implement each counter?



CLK = 1.8432 MHz

Figure 6: Synchronous Counter Wiring (RCO of the first chip is only connected to *T*, not +5).

Exercise 6: Construct a Set-Reset Latch with NAND gates

Build a clocked positive SR latch using NAND gates (use the setup shown in Figure 7). On a "set", the output Q should be high, and $\overline{Q}$ should be low. On a "reset", the output $\overline{Q}$ should be high, and Q should be low. However, since this is a clocked latch, the output can only change during the clk high phase; it is held at all other times. Explain how the SR latch works and demonstrate the functionality of the built circuit. Be prepared to explain what happens during the case when both *S* and *R* are high.

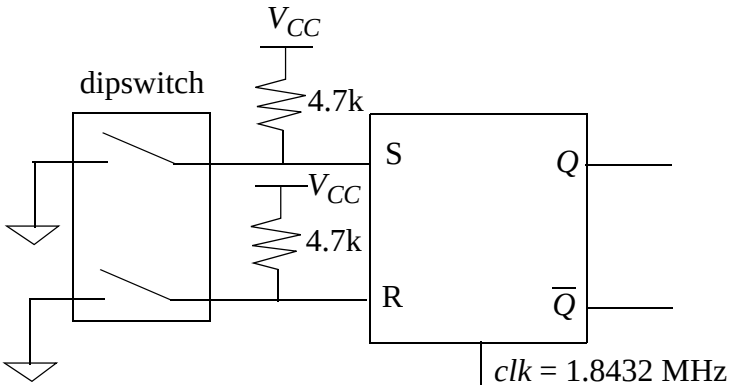


Figure 7: Setup for SR Latch.

Exercise 7: Setup Time Measurement of a *D Edge-triggered Register*

This is an open-ended problem. If you find a solution, be descriptive in your measurement methodology. If you can't find a solution, explain the different methods you did try and other possibilities that you thought may work.

Setup and hold times are important constraints to follow when implementing a digital system. With respect to a *D edge-triggered register*, explain what each of these constraints are, and explain types of failures that may occur if one of these constraints is violated. Using a 74LS74 part and any additional components necessary, develop a system that can measure the setup time of a *D register.* Remember that you need to test both when a *D register* should capture a 0 and when it should capture a 1. Be sure that the system only tests the setup time and does not change any other parameters, such as the rise and fall times of the inputs. You may use any method possible, but be sure to justify the method.

Find the published setup time on the datasheet for a 74LS74 (this number will vary from manufacturer to manufacturer and across chips) and compare to your measured time. Provide possible reasons why they might not match. Be prepared to demonstrate how you measured the setup time using a circuit diagram and an oscilloscope.

Exercise 8: Writing Combinational Verilog code (introduction to ModelSim, Xilinx Software and the Labkit)

In this exercise, you will design and implement a Verilog module that takes as input a 4-input binary coded decimal and outputs 7 bits that will properly illuminate a 7-segment display. Figure 8a (left) shows the 10 possible digits and Figure 8b shows the output mapping to segments.

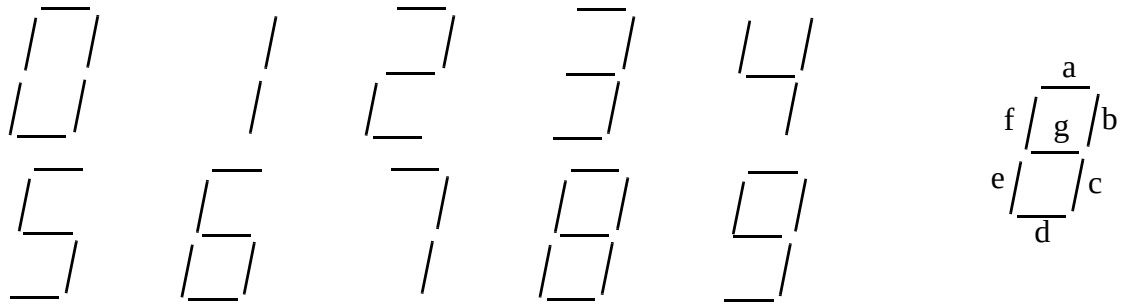


Figure 8: (a) The ten segmented digits. (b) shows the mapping of outputs a-g to segments.

Using Karnaugh Maps, design the combinational logic that encodes the 4-bit input to the 7-segment display. Fill out each Karnaugh Map, and make circles for either Minimal Sum-of-Products, or Minimal Product-of-Sums so that you minimize the required logic. Some segments will use MSP, and others will use MPS.

In Verilog, program the combinational logic. You do not have to use the minimized equations for programming the logic. Synthesis tools are powerful and will automatically optimize your logic equations. Download three source files from the course website: http://web.mit.edu/6.111/www/s2008/LABS/LAB1/{lab1_labkit.v, labkit.ucf, and seven_segment.v}. lab1_labkit.v instantiates the seven_segment conversion module as well as other circuitry to drive the dot-matrix display on the labkit (appropriate wrapper logic is included to make the dot-matrix display on the labkit look like a 7-segment display. **Please do not use the discrete 7-segment display chip given with the kit**). For this exercise, you should only modify the seven_segment.v source code and assign the correct logic function to the outputs.

Go to the labkit documentation on the course website, and follow through the 'Getting Started with ISE' and 'Programming the Labkit' tutorial. You can simulate your 7-segment decoder using ModelSim. Please read 'Simulating with ModelSim', which describes running ModelSim directly from Xilinx ISE. These tutorial sites can be found at: http://www-mtl.mit.edu/Courses/6.111/labkit/{ise.shtml, configuration.shtml, simulation.shtml}.

You should now be able to create a new Xilinx project that includes lab1_labkit.v, labkit.ucf, and seven_segment.v. Find where your 'segment_decoder' module is instantiated under lab1_labkit.v. Create a simple test bench called tb_7segment.v to verify that your 7-segment decoder works correctly (call the top level module tb_7segment). Simulate your 7-segment decoder using ModelSim. Observe the outputs of your test vectors on the Wave window. After you have verified that the logic is correct, you will compile and program the FPGA to display the ten digits. After you

load your project on the FPGA, use the low four switches as the input. Verify that the correct digit appears on the LED display.

You may also run ModelSim in stand alone mode for simulation (in general, we recommend you run ModelSim directly from the Xilinx ISE environment). Details of this can be found on the course website (http://web.mit.edu/6.111/www/s2009/handouts/ModelSim_tutorial.pdf).

Student Name:
TA:
Date Submitted:

Lab 1: Checkoff Sheet

Be prepared to show relevant diagrams as requested in each problem. You may get checked off per problem, rather than the whole lab at once. Collect initials for each problem on this sheet and turn it in with your report.

1. _____

2. _____

3. _____

4. _____

5. _____

6. _____

7. _____

8. _____

Student Name:
TA:
Date Submitted:

Lab 1: Report Template

This report template is useful to prepare for each exercise's checkoff. Fill in answers for the questions requested by exercise; you may use a different sheet of paper if more convenient, but be sure to follow the template. Be sure to prepare relevant diagrams as requested by each problem. Turn in this report after completing the lab 1 checkoff.

Exercise 1: TTL/CMOS Static Electrical Characteristics

Low Voltage Measurement (In = 1) for 74LS00:

High Voltage Measurement (In = 0) for 74LS00:

Low Voltage Measurement (In = 1) for 74HC00:

High Voltage Measurement (In = 0) for 74HC00:

For each of these measurements, does the output satisfy the ranges specified in the appropriate datasheets? Explain.

What problems could arise from using the LS series with the HC series (at +5V supply)?

Exercise 2: Build your own ring oscillator

Please draw out the waveform showing the output for the 5-inverter oscillator ring. Be sure to label the maximum and minimum voltages, and label the appropriate time intervals.

What is the average TTL inverter propagation delay? Show calculations and briefly explain.

Estimate the period of oscillation for a 3 inverter ring, rather than 5? Explain. What was your measured result?

What happens if you add a long piece of wire to the 3 inverter ring? Explain what causes this to happen.

What is the voltage measurement when you connect the output to the input of a single inverter? What is the significance of this voltage?

Exercise 3: Glitches

What is the width of the glitch measured using the scope and the logic analyzer?

Why does this glitch occur, and what is the lesson learned from this exercise?

Under what conditions is it a bad idea to use a glitchy signal as an input?

Exercise 4: Asynchronous Counters

Please draw a diagram showing the flip-flop arrangement of a typical asynchronous counter, emphasizing the source of each clk input for each flip-flop.

What is your measurement for the clk to MSB delay? From this measurement, show calculations for the clk-to-q delay for a typical flip-flop in the LS393, and explain the derivation.

Exercise 5: Synchronous Counter

Draw a diagram showing the flip-flop arrangement of a typical synchronous counter, emphasizing the source of each clk input for each flip-flop.

How long does it take, after the rising edge of the clock, for one of the flip-flops to change state? Does it matter which output bit you choose? Explain

Show the logic analyzer output to a TA. Can you observe any glitches on RCO? Explain under what circumstance you might expect RCO glitches to occur.

Explain why the RCO and ENT are connected between the two counters, and explain how they work.

What is the difference between the ENT and ENP inputs on a 74LS163?

Explain some differences between the 74LS163 and the 74LS393 in terms of design and performance. How many flip-flops and how much logic is required to implement the counter?

Exercise 6: Set-Reset Latch Construction

Draw your circuit diagram for the SR Latch.

Draw the truth table for the SR Latch.

Explain the functionality of the SR Latch and give an example on how it may be used.

Exercise 7: Setup Time Measurement of a *D Edge-triggered Register*

Explain your solution using relevant diagrams and explanations.

Explain the main sources of error in the measurement technique and potential differences with datasheets.

Exercise 8: Writing Combinational Verilog code

Print out your code for the combinational Verilog code, and be sure to have it ready for checkoff. Draw out the 7 Karnaugh maps corresponding to the different outputs, and generate the minimized equation, that is, either MPS or MSP as appropriate. Write down the equations below each Karnaugh map.

a

	00	01	11	10
00				
01				
11				
10				

b

	00	01	11	10
00				
01				
11				
10				

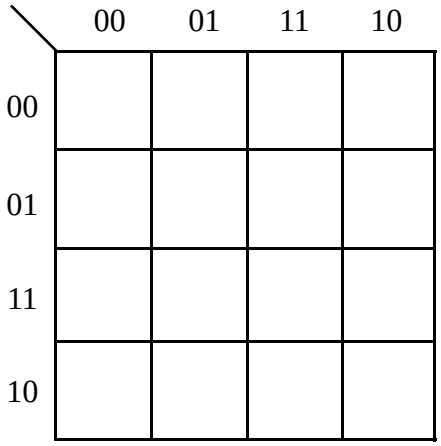
c

	00	01	11	10
00				
01				
11				
10				

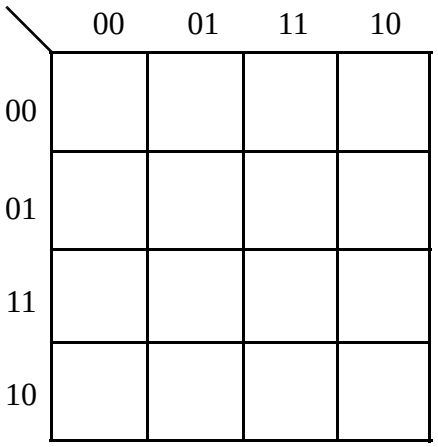
d

	00	01	11	10
00				
01				
11				
10				

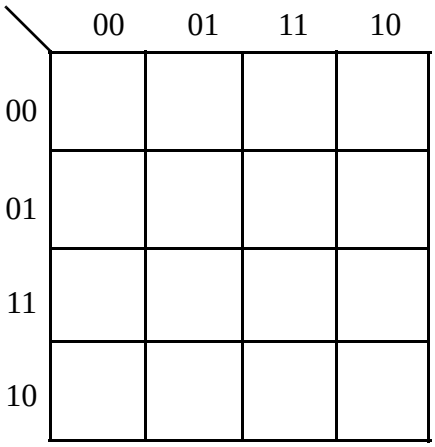
e



f



g



Department of Electrical Engineering & Computer Science

ELECTRICAL SAFETY

for Staff and Students in EECS Instructional Laboratories

NEVER WORK ALONE

If you will be working with energized circuits or equipment **over 50 volts peak or 50 volts DC**, make sure that at least one other person can see you and hear you. In case of emergency **DIAL 100** from any institute phone [**617-253-1212** from cell phones]; and notify the stock clerk or lab instructor on duty.

VOLTAGE RULES

All EECS Instructional Laboratories lab kit voltages are **below 50 volts peak or 50 volts DC**. (OSHA permits "unqualified persons" to work on such circuits with "awareness-type" training, which is what this document is.)

If you intend to work on a project using power sources **over 50 volts peak or 50 volts DC**, you must first **secure permission** from your Instructor or TA; and take an ***Electrical Safety Training class*** from either Ron Roscoe [38-641, 253-4635] or Gim Hom [38-644, 324-3373] **before** any work on the project begins.

PREVENT ACCIDENTS: FOLLOW THIS ADVICE

- Never hurry. Work deliberately and carefully.
- Connect to the power source **LAST.**
- If you are working with a lab kit that has internal power supplies, **turn the main power switch OFF** before you begin work on the circuits. Wait a few seconds for power supply capacitors to discharge. These steps will also help prevent damage to circuits.
- If you are working with a circuit that will be connected to an external power supply, **turn the power switch of the external supply OFF** before you begin work on the circuit.
- Check circuit power supply voltages for proper value and for type (DC, AC, frequency) before energizing the circuit.
- Do not run wires over moving or rotating equipment, or on the floor, or string them across walkways from bench-to-bench.
- Remove conductive watchbands or chains, finger rings, wristwatches, etc., and do not use metallic pencils, metal or metal edge rulers, etc. when working with exposed circuits.
- When breaking any high-voltage or high current inductive circuit open the switch with your left hand and turn your face away to avoid danger from any arc which may occur across the switch terminals.
- When using large electrolytic capacitors be sure to wait long enough (approximately five time constants) for the capacitors to discharge before working on the circuit.
- All conducting surfaces intended to be at ground potential should be connected together.

ADDITIONAL CAUTIONS

- The EECS Instructional Laboratories (38-500, 38-600, 38-601) are equipped with Ground Fault Current Interrupt (GFCI) circuit breakers. Check for leakage paths to ground when breakers trip repeatedly and the problem is not due to an overload.

- Any equipment used in the laboratories must be equipped with a standard three-prong AC plug or a two-pronged polarized plug.

- All exposed non-current-carrying metal parts of fixed and portable equipment that may accidentally become energized should be grounded.

- All electrical equipment or apparatus that may require frequent maintenance must be capable of being completely disconnected from the power source.

- Do not bring into the lab or use in the lab equipment that does not conform to these rules without specific permission from your instructor, TA, or Ron Roscoe or Gim Hom.

LASER LABORATORY SAFETY

- Students who intend to use laser systems **must** read the Radiation Protection Office (RPO) Laser Safety Program Handbook **before** working with lasers. Copies of this handbook are available from the 38-501 Stockroom.

- Students must attend the RPO Safety Training Seminar if they will be using Class III or IV lasers.

RIGHT-TO-KNOW LAW (OSHA HAZARD COMMUNICATION STANDARD)

- OSHA requires MIT to inform employees (and MIT requires students be informed the same as employees) about potential exposure to hazardous chemicals and about the Institute's Hazard Communication Program and the requirements of the Federal Right-to-Know Law. Your supervisor/instructor and department are responsible for providing you with safety information and/or training on: • MIT Policies and Procedures on Environmental Health & Safety • Material Safety Data Sheets • Labeling requirements for all hazardous materials • The location of the hazardous material inventory of your work area • Any operations in your work area that involve hazardous chemicals and the associated health and safety hazards • Safety precautions and procedures • Emergency procedures • The hazards of tasks done infrequently

- The OSHA Hazard Communication Standard and MIT's written Hazard Communication Program are on file in the MIT Safety Office and will be made available to any member of the MIT Community, upon request.

QUESTIONS ABOUT WORK/SCHOOL SAFETY

- Any questions about work or school safety should be brought to the attention of your immediate supervisor or instructor. If problems arise that cannot be solved at this level, you should contact the EECS Safety Officer:

Ron Roscoe	Rm. 38-641	253-4635	rroscoe @ MIT.EDU

BASIC ELECTRICAL SAFETY PRACTICES

The Institute requires everyone who uses electrical equipment to understand these safety precautions to comply with the OSHA Electrical Safety-Related Work Practices standard and MIT's electrical safety policies. The following safe work practices can prevent electrical shock. Contact your supervisor for additional safety training if your job involves repairing, installing or working on energized parts.

A. Safe Work Practices

1. Turn off and unplug equipment (instead of relying on interlocks that can fail) before removing the protective cover to clear a jam, replace a part, adjust or troubleshoot. Ask a qualified person to do the work if it involves opening equipment and creating an exposure to energized parts operating at **50 volts peak or 50 volts DC** or more.
2. Don't use an electrical outlet or switch if the protective cover is ajar, cracked or missing. Call FIXIT (x3-4948) and report this.
3. Only use DRY hands and tools and stand on a DRY surface when using electrical equipment, plugging in an electric cord, etc.
4. Never put conductive metal objects into energized equipment.
5. Always pick up and carry portable equipment by the handle and/or base. Carrying equipment by the cord damages the cord's insulation.
6. Unplug cords from electrical outlets by pulling on the plug instead of pulling on the cord.
7. Use extension cords temporarily. The cord should be appropriately rated for the job.
8. Use extension cords with 3-prong plugs to ensure that equipment is grounded.
9. Never remove the grounding post from a 3-prong plug so you can plug it into a 2-prong wall outlet or extension cord.
10. Re-route electrical cords or extension cords so they aren't run across the floor, under rugs or through doorways, etc. Stepping on, pinching or rolling over a cord will break down the insulation and will create shock and fire hazards.
11. Don't overload extension cords, multi-outlet strips and wall outlets.
12. Heed the warning signs, barricades and/or guards that are posted when equipment or wiring is being repaired or installed or if electrical components are exposed.

B. *Check for Unsafe Conditions* (either before or while you're using equipment:)

1. Is the cord's insulation frayed, cracked or damaged, exposing the internal wiring?
2. Are the plug's prongs bent, broken or missing, especially the third prong?
3. Is the plug or outlet blackened by arcing?
4. Was liquid spilled on or around the equipment?
5. Are any protective parts (or covers) broken, cracked or missing?
6. Do you feel a slight shock when you use the equipment?
7. Does the equipment or the cord overheat when it is running?
8. Does the equipment spark when it is plugged in or when switches or controls are used?

C. **If you observe any of these unsafe conditions:**

1. Don't use (or stop using) the equipment.
2. Tag/label the equipment UNSAFE--DO NOT USE and describe the problem.
3. Notify your supervisor, FIXIT or the service company, as appropriate.

Electrical safety is for everyone because even contact with the standard 117 volt electrical circuits, which we constantly use, can be lethal under certain conditions.

I CERTIFY THAT I HAVE READ AND UNDERSTOOD *"ELECTRICAL SAFETY FOR STAFF AND STUDENTS IN EECS INSTRUCTIONAL LABORATORIES"* AND *"BASIC ELECTRICAL SAFETY PRACTICES"* AND I AGREE TO ABIDE BY THOSE RULES AT ALL TIMES WHILE I AM ENROLLED IN ANY EECS LABORATORY COURSE, OR WHILE TEACHING OR ASSISTING IN A LABORATORY COURSE.

TA's & LA'S ASSIGNED TO ANY ONE OF THE LISTED SUBJECTS MUST, AS A CONDITION OF EMPLOYMENT, ATTEND ONE OF THE ELECTRICAL SAFETY TRAINING LECTURES HELD DURING THE FIRST WEEKS OF THE SEMESTER. EXACT TIMES AND PLACE WILL BE POSTED. **ALL OTHER STUDENTS: FILL OUT, SIGN, AND RETURN THIS PAGE ONLY TO ONE OF THE EECS STOCKROOM WINDOWS at 38-501 or 38-601, IN ORDER TO RECEIVE YOUR LAB KIT.**

[No laboratory kits or supplies or equipment will be issued to students until this form is filled out and signed and on file at one of the EECS stockroom windows at 38-501 or 38-601.]

SIGNED:_____

PRINT NAME:_____

MIT ID NUMBER:_____

DATE:_____

EVERYONE PLEASE CHECK SUBJECT NUMBER:

6.002_____**6.003**_____**6.099**_____**6.101**_____

6.102_____**6.111**_____**6.115**_____**6.121J**_____

6.131_____**6.152J**_____**6.161**_____**6.301**_____

6.302_____**6.331**_____**6.691**_____**6.776**_____

Other_____**(specify)**

M A S S A C H U S E T T S I N S T I T U T E O F T E C H N O L O G Y
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

6.111 Lab Kit Signout – Spring 2009

The components, tools, breadboard and test equipment probes/pods you'll need to complete the labs are available in a lab kit which you can check out of the Instrument Room, 38-601. This kit must be returned to the Instrument Room by 5:00pm, Thursday May 14, 2009. **You are responsible for returning all the items in the kit in working condition** and will be charged a replacement fee for missing or broken items (in particular, please take good care of the probes and pods as they are expensive!). There is a $40 late fee if we have already charged your bursar's account when the kit is finally returned. Note that the Bursar's office charges an additional $5 fee for charges of $10 or less. All additional components signed out at project time must be returned at the same time as the lab kits.

Contents of the Lab Kit (replacement costs shown in italics):

(2) 74LS00	(1) 1.8432 MHz oscillator	(1) wire stripper *($11)*
(1) 74HC00	(1) 7-segment LED display	(1) IC extraction tool *($6)*
(1) 74LS04	(1) dip switch	(1) long nose pliers *($16)*
(1) 74LS74	(1) 10-pin header strip	(2) scope probes *($80 each)*
(2) 74LS163	(1) 6264 SRAM Memory	(2) 8-pin analyzer pods *($250 each)*
(1) 74LS393	(1) USB Flash Drive (*$20*)	(1) protoboard *($25)*

To check out a lab kit please complete the information below and bring this form to the Instrument Room, 38-601, during normal business hours.

NAME:_____ MIT ID #: _____

TERM ADDRESS: _____

PHONE: _____ EMAIL: _____

I certify that I have read and understood the *Electrical Safety Instructions for Staff and Students in EECS Instructional Laboratories* and *Basic Electrical Safety Practices*, and I agree to abide those rules at all times while I am enrolled in 6.111.

SIGNATURE: _____ DATE: _____

Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science
6.111 – Introductory Digital Systems Laboratory

Information Sheet and Permission Form (Spring 2009)

Generation Information:

Name:_____ **MIT ID:**_____
(last) (first)

Course: _____ **Year:**_____

Term Address:_____ **Phone:**_____

Email Address:_____

Pre-requisite (please check one): 6.002 ( ) or 6.071 ( )
Check if you have taken 6.01 ( )
Check if you have taken 6.02 ( )
Check if you have taken 6.004 ( )
Check if you are currently taking 6.004 ( )

6.111 Introductory Digital Systems Laboratory Permission Form (you can change your election during the term). Check and sign YES or NO:

____ **NO**. I do not grant Massachusetts Institute of Technology any rights described herein.

Signature _____ Date_____

____ **YES**. I grant Massachusetts Institute of Technology the rights described herein. I, the undersigned individual, hereby grant Massachusetts Institute of Technology (MIT), located at 77 Massachusetts Avenue, Cambridge, Massachusetts, U.S.A., the perpetual, nonexclusive, royalty-free right and license to:

Record my participation and appearance on video tape, audio tape, film, photograph or any other medium (collectively, the "Recordings").

Use my name, likeness, voice and biographical material in connection with these recordings. Reproduce, distribute, publicly display and/or publicly perform, in print, electronic or any other medium, copies of the Recordings, in whole or in part. Grantor represents that he or she possesses all rights necessary to grant this permission.

Signature _____ Date_____