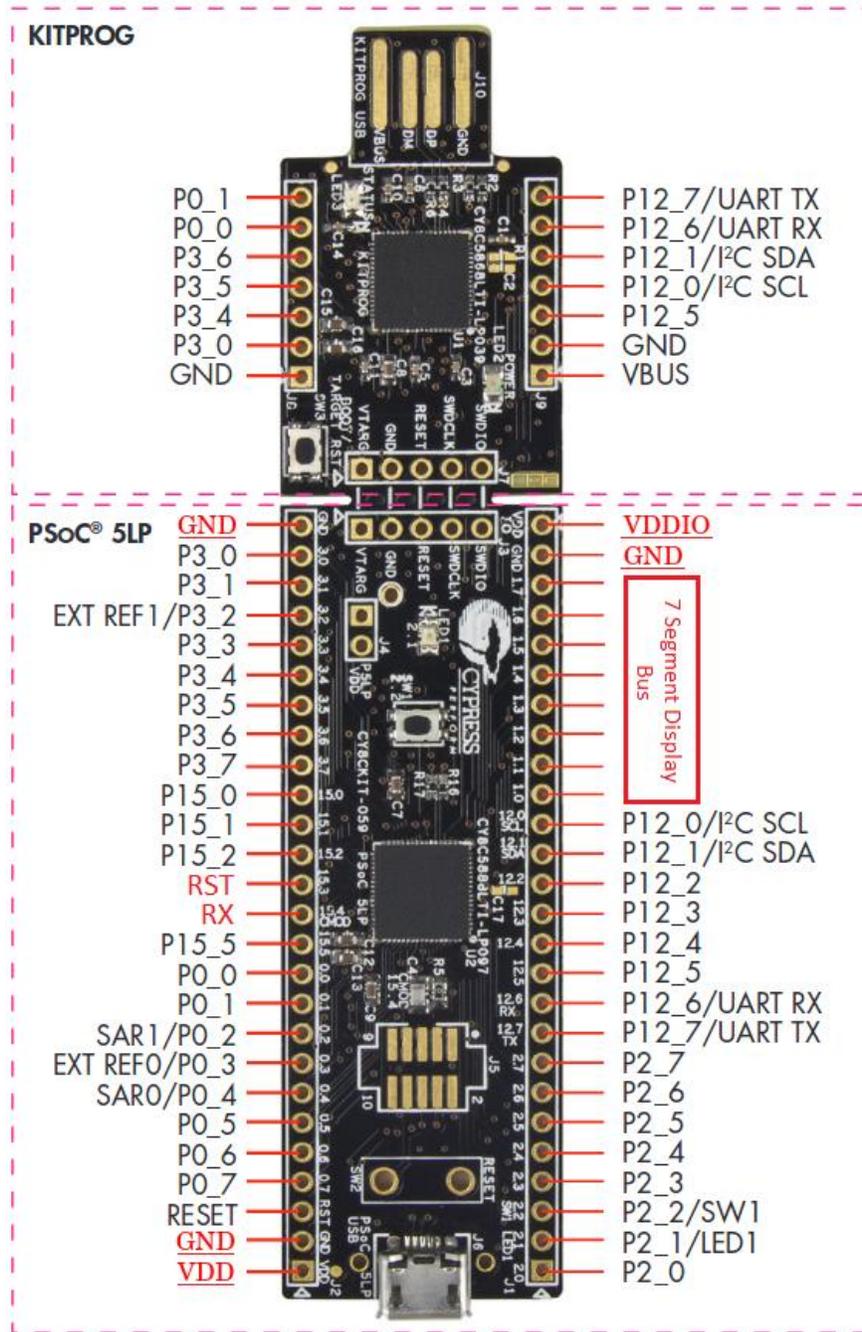


7-Segment Display UART Catcher Manual

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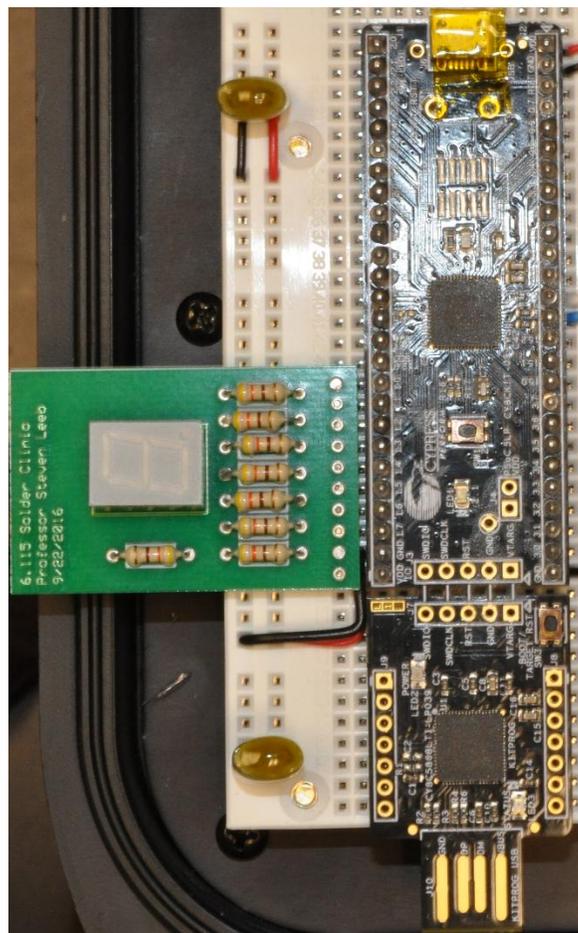
1 Overview

The PSoC based 7 Segment Display UART Catcher is intended to be used for the 6.115 “blinky” laboratory. Its purpose is to Receive bytes through UART and display the character corresponding to the UART byte on the attached 7 segment display.

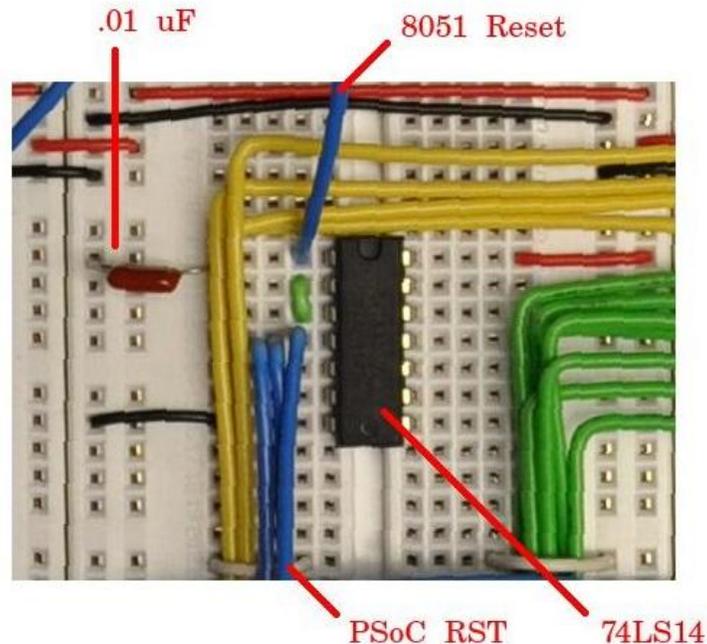
2 Hardware

This UART Catcher requires only a CY8CKIT-059 PSoC 5LP. Many of the pins on this PSoC are not used for this solution and are labeled in black on the pinout shown on page one of this manual. The pins that are used for this solution are labeled with their function in red.

This PSoC is fitted with a RX line where it receives UART bytes at 9600 baud and a port where the 7 segment display plugs directly into the breadboard along the PSoC. The seven segment display should be situated on the breadboard in relation to the PSoC as shown in the image below.



The PSoC Catcher also has a RST line which controls the software reset of the entire PSoC replacement. This RST line should be connected to the 8051 reset pin through two 7414 inverters with a .01 uF capacitance on the 8051 reset line.



In addition to connecting the RX pin to a UART driving device and the designated pins / bus to the 7 segment display, the three GND pins of the PSoC should connect to the ground of the 8051 system. VDD and VDDIO should be tied to +5VDC.

3 Software

The software driving the 7 Segment Display UART Catcher is very simple. A UART module is responsible for receiving bytes at 9600 baud. When a byte is received, the main loop of code determines how to control the 7 segment display based on which byte is received.

For any hex value to be displayed on the 7 segment display, the corresponding byte to send to the Catcher is that hex value. For example, if you wish to display the letter 'A' on the 7 segment display, you would have to send the byte 0x0A to the Catcher at 9600 baud. In addition to being able to display all hex values, the 7 seven segment display can also display the period ('.'). In order to display this, the Catcher PSoC needs to be sent the byte 0x2E at 9600 baud. Any byte sent to the Catcher other than these described above will result in the 7 segment display being cleared.

4 Example

To demonstrate this 7 Segment Display Catcher Module, we will use a PSoC based 16C450 replacement to drive the UART RX pin on the Catcher and sequentially flash through all of the hexadecimal values.

Make all necessary connections described in the hardware section of this manual including: VDD, VDDIO, GND, RST, and the seven segment display. After that is complete, wire the TX pin of a 16C450 Replacement PSoC to the RX pin of this Catcher. Finally, assemble and load the 8051 R31-JP system with this code:

```

.org    000h
ljmp   start

.org    100h
start:
    lcall  init
main:
    mov    a, #0Fh                ; Mask R3 and send it to the P1
                                       ; LED's

    anl    a, R3
    mov    R3, a
    mov    P1, a

    mov    dptr, #0xFE01          ; Send R3 to the seven segment
                                       ; display

    movx   @dptr, a

    mov    R0, #00h              ; Wait a second or two
    mov    R1, #00h
    mov    R2, #0Ah
delay:
    djnz   R0, delay
    djnz   R1, delay
    djnz   R2, delay

    inc    R3                    ; Increment R3
    sjmp   main                  ; Repeat

init:
    mov    dptr, #0xFE00          ; Set up PSoC UART flags for 9600
                                       ; baud communication

    mov    a, #0x15
    movx   @dptr, a

    mov    R3, #00h              ; Set up display value to start at zero

    ret

```

Once this code is loaded onto and running on the 8051 system, the 7 segment display should count up from 0 to F in hexadecimal and wrap back around to 0. The P1 LED's on the 8051 should flash in sync with the 7 segment display showing the hex value in its corresponding binary representation.