ADC0841
8-Bit µP Compatible A/D Converter

General Description
The ADC0841 is a CMOS 8-bit successive approximation A/D converter. Differential inputs provide low frequency input common mode rejection and allow offsetting the analog range of the converter. In addition, the reference input can be adjusted enabling the conversion of reduced analog ranges with 8-bit resolution.

The A/D is designed to operate with the control bus of a variety of microprocessors. TRI-STATE® output latches that directly drive the data bus permit the A/D to be configured as a memory location or I/O device to the microprocessor with no interface logic necessary.

Features
- Easy interface to all microprocessors
- Operates ratiometrically or with 5 Vdc voltage reference
- No zero or full-scale adjust required
- Internal clock
- 0V to 5V input range with single 5V power supply
- 0.3” standard width 20-pin package
- 20 Pin Molded Chip Carrier Package

Key Specifications
- Resolution: 8 Bits
- Total Unadjusted Error: ± 1⁄2 LSB and ± 1 LSB
- Single Supply: 5 Vdc
- Low Power: 15 mW
- Conversion Time: 40 µs

Block and Connection Diagrams
Absolute Maximum Ratings (Notes 1, 2)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V_{CC}$) 6.5V
Voltage at Other Inputs and Outputs −0.3V to $V_{CC} +0.3V$
Input Current Per Pin (Note 3) ±5mA
Input Current Per Package (Note 3) ±20mA
Storage Temperature −65˚C to +150˚C
Package Dissipation at $T_A=25˚C$ 875 mW

Operating Conditions (Notes 1, 2)
Supply Voltage ($V_{CC}$) 4.5 $V_{DC}$ to 6.0 $V_{DC}$
Temperature Range $T_{MIN} \leq T_A \leq T_{MAX}$
$T_{MIN} = T_{A} \leq T_{MAX}$
ADC0841BCN, ADC0841CCN 0˚C $\leq T_A \leq 70˚C$
ADC0841BCV, ADC0841CCV −40˚C $\leq T_A \leq 85˚C$

Electrical Characteristics
The following specifications apply for $V_{CC}=5\ V_{DC}$ unless otherwise specified. **Boldface limits apply from $T_{MIN}$ to $T_{MAX}$; all other limits $T_{A}=T_{J}=25˚C$.**

### CONVERTER AND MULTIPLEXER CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>ADC0841BCN, ADC0841CCN</th>
<th>ADC0841BCV, ADC0841CCV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Total Unadjusted Error</td>
<td>$V_{REF}=5.00\ V_{DC}$ (Note 4)</td>
<td>±1/8</td>
<td>±1/8</td>
</tr>
<tr>
<td>Minimum Reference Input Resistance</td>
<td>2.4</td>
<td>1.2</td>
<td>1.1</td>
</tr>
<tr>
<td>Maximum Reference Input Resistance</td>
<td>2.4</td>
<td>5.4</td>
<td>5.9</td>
</tr>
<tr>
<td>Minimum Common-Mode Input Voltage</td>
<td>$V_{CC}=0.05$</td>
<td>$V_{CC}=0.05$</td>
<td>V</td>
</tr>
<tr>
<td>DC Common-Mode Error</td>
<td>Differential Mode</td>
<td>±1/16</td>
<td>±1/4</td>
</tr>
<tr>
<td>Power Supply Sensitivity</td>
<td>$V_{CC}=5\ V \pm5%$</td>
<td>±1/16</td>
<td>±1/6</td>
</tr>
</tbody>
</table>

### DIGITAL AND DC CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>ADC0841BCN, ADC0841CCN</th>
<th>ADC0841BCV, ADC0841CCV</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{INH}$</td>
<td>Logical “1” Input Voltage (Min)</td>
<td>$V_{CC}=5.25V$</td>
<td>2.0</td>
<td>2.0</td>
</tr>
<tr>
<td>$V_{INL}$</td>
<td>Logical “0” Input Voltage (Max)</td>
<td>$V_{CC}=4.75V$</td>
<td>0.8</td>
<td>0.8</td>
</tr>
<tr>
<td>$I_{INH}$</td>
<td>Logical “1” Input Current (Max)</td>
<td>$V_{IN}=5.0V$</td>
<td>0.005</td>
<td>1</td>
</tr>
</tbody>
</table>

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Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = 5 V_{DC} unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}; all other limits T_{A} = T_{J} = 25˚C.**

### DIGITAL AND DC CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ (Note 6)</th>
<th>Tested Limit (Note 7)</th>
<th>Design Limit (Note 8)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{IN(0)}</td>
<td>Logical &quot;0&quot; Input Current (Max)</td>
<td>V_{IN} = 0 V</td>
<td>−0.005</td>
<td>−1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>V_{OUT(1)}</td>
<td>Logical &quot;1&quot; Output Voltage (Min)</td>
<td>V_{CC} = 4.75 V</td>
<td>2.8</td>
<td>2.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>I_{OUT} = −360 µA</td>
<td>4.6</td>
<td>4.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{OUT(0)}</td>
<td>Logical &quot;0&quot; Output Voltage (Max)</td>
<td>V_{CC} = 4.75 V</td>
<td>0.34</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I_{OUT}</td>
<td>TRI-STATE Output Current (Max)</td>
<td>V_{OUT} = 0 V</td>
<td>−0.01</td>
<td>−0.3</td>
<td>−3 µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{OUT} = 5 V</td>
<td>0.01</td>
<td>0.3</td>
<td>3 µA</td>
<td></td>
</tr>
<tr>
<td>I_{SOURCE}</td>
<td>Output Source Current (Min)</td>
<td>V_{OUT} = 0 V</td>
<td>−14</td>
<td>−7.5</td>
<td>−6.5 mA</td>
<td></td>
</tr>
<tr>
<td>I_{SINK}</td>
<td>Output Sink Current (Min)</td>
<td>V_{OUT} = V_{CC}</td>
<td>16</td>
<td>9.0</td>
<td>8.0 mA</td>
<td></td>
</tr>
<tr>
<td>I_{CC}</td>
<td>Supply Current (Max)</td>
<td>CS = 1, V_{REF} open</td>
<td>1</td>
<td>2.3</td>
<td>2.5 mA</td>
<td></td>
</tr>
</tbody>
</table>

### AC Characteristics

The following specifications apply for V_{CC} = 5 V_{DC}, t_{R} = t_{F} = 10 ns unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}; all other limits T_{A} = T_{J} = 25˚C.**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ (Note 6)</th>
<th>Tested Limit (Note 7)</th>
<th>Design Limit (Note 8)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{C}</td>
<td>Maximum Conversion Time (See Graph)</td>
<td></td>
<td>30</td>
<td>40</td>
<td>60 µs</td>
<td></td>
</tr>
<tr>
<td>t_{WR(RD)}</td>
<td>Minimum WR Pulse Width</td>
<td></td>
<td>50</td>
<td>150</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t_{ACC}</td>
<td>Maximum Access Time (Delay from Falling Edge of RD to Output Data Valid)</td>
<td>C_{L} = 100 pF</td>
<td>145</td>
<td>225</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t_{TH}</td>
<td>TRI-STATE Control (Maximum Delay from Rising Edge of RD to Hi-Z State)</td>
<td>C_{L} = 10 pF, R_{L} = 10k, t_{F} = 20 ns (Note 9)</td>
<td>125</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t_{WR}</td>
<td>Maximum Delay from Falling Edge of WR or RD to Reset of INTR</td>
<td></td>
<td>200</td>
<td>400</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>C_{IN}</td>
<td>Capacitance of Logic Inputs</td>
<td></td>
<td>5</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_{OUT}</td>
<td>Capacitance of Logic Outputs</td>
<td></td>
<td>5</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

**Note 2:** All voltages are measured with respect to the ground pins.

**Note 3:** During over-voltage conditions (V_{IN} < 0 V and V_{IN} > V_{CC}) the maximum input current at any one pin is ± 5 mA. If the current is limited to ± 5 mA at all the pins no more than four pins can be in this condition in order to meet the Input Current Per Package (± 20 mA) specification.

**Note 4:** Total unadjusted error includes offset, full-scale, and linearity.

**Note 5:** For V_{IN} (−) ≥ V_{IN} (+) the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{CC} to 5 V_{CC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{CC} over temperature variations, initial tolerance and loading.

**Note 6:** Typical values are at 25˚C and represent most likely parametric norm.

**Note 7:** Tested limits are guaranteed to National’s AOQL (Average Outgoing Quality Level).

**Note 8:** Design limits are guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

**Note 9:** The temperature coefficient is 0.3%/˚C.

**Note 10:** Human body model, 100 pF discharged through 1.5 kΩ resistor.
Note 11: Read strobe must occur at least 600 ns after the assertion of interrupt to guarantee reset of INTR.

Typical Performance Characteristics

Logic Input Threshold Voltage vs Supply Voltage

Output Current vs Temperature

Power Supply Current vs Temperature

Linearity Error vs \( V_{\text{REF}} \)

Conversion Time vs \( V_{\text{SUPPLY}} \)

Conversion Time vs Temperature
Typical Performance Characteristics (Continued)

Unadjusted Offset Error vs $V_{\text{REF}}$ Voltage

TRI-STATE Test Circuits and Waveforms

t_1H, $C_L = 10 \text{ pF}$

$t_0H, C_L = 10 \text{ pF}$

$t_i = 20 \text{ ns}$
Functional Description
A conversion is initiated via the CS and WR lines. If the data from a previous conversion is not read, the INTR line will be low. The falling edge of WR will reset the INTR line high and ready the A/D for a conversion cycle. The rising edge of WR starts a conversion. After the conversion cycle (tC ≤ 60 μsec), which is set by the internal clock frequency, the digital data is transferred to the output latch and the INTR is asserted low. Taking CS and RD low resets INTR output high and transfers the conversion result on the output data lines (DB0–DB7).

Applications Information

1.0 REFERENCE CONSIDERATIONS
The voltage applied to the reference input of this converter defines the voltage span of the analog input (the difference between V\text{MAX} and V\text{MIN}) over which the 256 possible output codes apply. The device can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the minimum reference input resistance of 1.1 kΩ. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system (Figure 1a), the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V\text{REF} pin can be tied to V\text{CC}. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy (Figure 1b), where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good choices for this purpose. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output reference path. This current spikes of current enter the “+” input and exit the “−” input due to the sampling nature of the analog inputs, short duration spikes of current enter the “+” input and exit the “−” input.

Due to the sampling nature of the analog inputs, short duration spikes of current enter the “+” input and exit the “−” input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ. An op amp active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

2.0 THE ANALOG INPUTS

2.1 Analog Differential Voltage Inputs and Common-Mode Rejection
The differential inputs of this converter actually reduce the effects of common-mode input noise, a signal common to both selected “+” and “−” inputs for a conversion (60 Hz is most typical). The time interval between sampling the “+” input and then the “−” input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

\[ V_{\text{ERROR(MAX)}} = V_{\text{peak}}(2\pi f_{\text{CM}}) \times 0.5 \times \left( \frac{t_c}{\theta} \right) \]

where \( f_{\text{CM}} \) is the frequency of the common-mode signal, \( V_{\text{peak}} \) is its peak voltage value and \( t_c \) is the conversion time.

For a 60 Hz common-mode signal to generate a ¼ LSB error (≈ 5 mV) with the converter running at 40 μS, its peak value would have to be 5.43V. This large common-mode signal is much greater than that generally found in a well designed data acquisition system.

2.2 Input Current
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Applications Information (Continued)

The full-scale adjustment should be made [with the proper \( V_{\text{IN}} (-) \) voltage applied] by forcing a voltage to the \( V_{\text{IN}} (+) \) input which is given by:

\[
V_{\text{IN}} (+) \text{ fs adj} = V_{\text{MAX}} - 1.5 \left( \frac{V_{\text{MAX}} - V_{\text{MIN}}}{256} \right)
\]

where \( V_{\text{MAX}} \) is the high end of the analog input range and \( V_{\text{MIN}} \) is the low end (the offset zero) of the analog range. (Both are ground referenced.)

The \( V_{\text{REF}} \) (or \( V_{\text{CC}} \)) voltage is then adjusted to provide a code change from \( \text{FE}_{\text{HEX}} \) to \( \text{FF}_{\text{HEX}} \). This completes the adjustment procedure.

For an example see the Zero-Shift and Span Adjust circuit below.

Zero Shift and Span Adjust (2V \( \leq V_{\text{IN}} \leq 5V \))

FIGURE 1. Referencing Examples

For a detailed explanation of the circuit diagram, please refer to the manufacturer's documentation.
Applications Information (Continued)

Span Adjust 0V ≤ V_{IN} ≤ 3V

Protecting the Input

High Accuracy Comparator

Diodes are 1N914
Applications Information (Continued)

**Continuous Conversion**

![Diagram of ADC0841 and INS8039 Interface](image)

**Operating with Automotive Ratiometric Transducers**

![Diagram of Ratiometric Transducer Connection](image)

*V_in(−) = 0.15 V_{CC}.
15% of V_{CC} ≤ V_{XDR} ≤ 85% of V_{CC}.

**SAMPLE PROGRAM FOR ADC0841 — INS8039 INTERFACE**

**CONVERTING TWO RATIO METRIC, DIFFERENTIAL SIGNALS**

<table>
<thead>
<tr>
<th>ORG</th>
<th>0H</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>04 10</td>
</tr>
<tr>
<td>BEGIN:</td>
<td>MOV</td>
</tr>
<tr>
<td></td>
<td>JMP</td>
</tr>
<tr>
<td></td>
<td>ORG</td>
</tr>
<tr>
<td>0010</td>
<td>B9 FF</td>
</tr>
<tr>
<td></td>
<td>MOV</td>
</tr>
<tr>
<td></td>
<td>ORL</td>
</tr>
<tr>
<td></td>
<td>MOV</td>
</tr>
<tr>
<td></td>
<td>CALL</td>
</tr>
</tbody>
</table>

;START PROGRAM AT ADDR 10
;MAIN PROGRAM
;LOAD R1 WITH A UNUSED ADDR LOCATION
;A/D DATA ADDRESS
;SET PORT 1 OUTPUTS HIGH
;LOAD THE ACC WITH 00
;CALL THE CONVERSION SUBROUTINE
;CONTINUE MAIN PROGRAM

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Applications Information (Continued)

;CONVERSION SUBROUTINE
;ENTRY: ACC — A/D MUX DATA
;EXIT: ACC — CONVERTED DATA

ORG 50H

0050 99 FE  CONV:  ANL   P1,#0FEH ;CHIP SELECT THE A/D
0052 91    MOVX  @R1,A ;START CONVERSION
0053 09    LOOP:  IN    A,P1 ;INPUT INTR STATE
0054 32 53  JB1   LOOP ;IF INTR = 1 GOTO LOOP
0056 81    MOVX  A,@R1 ;IF INTR = 0 INPUT A/D DATA
0057 89 01  ORL   P1,&01H ;CLEAR THE A/D CHIP SELECT
0059 A0    MOV   @R0,A ;STORE THE A/D DATA
005A 83    RET   ;RETURN TO MAIN PROGRAM
SAMPLE PROGRAM FOR ADC0841 — NSC800 INTERFACE

0010 NCONV EQU 16 ;TWICE THE NUMBER OF REQUIRED CONVERSIONS

000F DEL EQU 15 ;DELAY 60 µsec CONVERSION

001F CS EQU 1FH ;THE BOARD ADDRESS

3C00 ADDTA EQU 003CH ;START OF RAM FOR A/D DATA

0000' 00 DTA: DB 08H ;DATA

0001' 0E 1F START: LD C,CS

0003' 06 16 LD B,NCONV

0005' 21 0000' LD HL,DTA

0006' 11 003C LD DE,ADDTA

000B' ED A3 STCONV: OUTI ;START A CONVERSION

000D' EB EX DE,HL ;HL=RAM ADDRESS FOR THE A/D DATA

000E' 3E 0F LD A,DEL

0010' 3D WAIT: DEC A ;WAIT 60 µsec FOR THE

0011' C2 0013' JP NZ,WAIT ;CONVERSION TO FINISH

0014' ED A2 INI ;STORE THE A/D’S DATA

0016' EB EX DE,HL

0017' C2 000E' JP NZ,STCONV ;IF NOT GOTO STCONV

END

Note 12: A conversion is started, then a 60 µs wait for the A/D to complete a conversion and the data is stored at address ADDTA for the first conversion, ADDTA + 1 for the second conversion, etc. for a total of 8 conversions.
## Ordering Information

<table>
<thead>
<tr>
<th>Temperature Range</th>
<th>Total Unadjusted Error</th>
<th>Package Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>±1/2 LSB</td>
<td>±1 LSB</td>
<td>N20A Molded Dip</td>
</tr>
<tr>
<td>0°C to +70°C</td>
<td>ADC0841BCN</td>
<td></td>
</tr>
<tr>
<td>±1 LSB</td>
<td>ADC0841CCN</td>
<td></td>
</tr>
<tr>
<td>-40°C to +85°C</td>
<td>ADC0841BCV</td>
<td>V20A Molded Chip Carrier</td>
</tr>
<tr>
<td>±1 LSB</td>
<td>ADC0841CCV</td>
<td></td>
</tr>
</tbody>
</table>
Physical Dimensions  inches (millimeters) unless otherwise noted

Molded Dual-In-Line Package (N)
Order Number ADC0841BCN or ADC0841CCN
NS Package Number N20A

Molded Chip Carrier Package (V)
Order Number ADC0841BCV or ADC0841CCV
NS Package Number V20A
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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