PIC16F62X

PIC16F62X Silicon/Data Sheet Errata

The PIC16F62X (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS40300**B**), except for the anomalies described below.

1. Module: I/O Ports

A read of the PORTB Data Direction Register (TRISB) returns the Data Direction state on the port pins themselves and not the contents of the TRISB register latch.

FIGURE 1: BLOCK DIAGRAM OF RB0/INT PIN

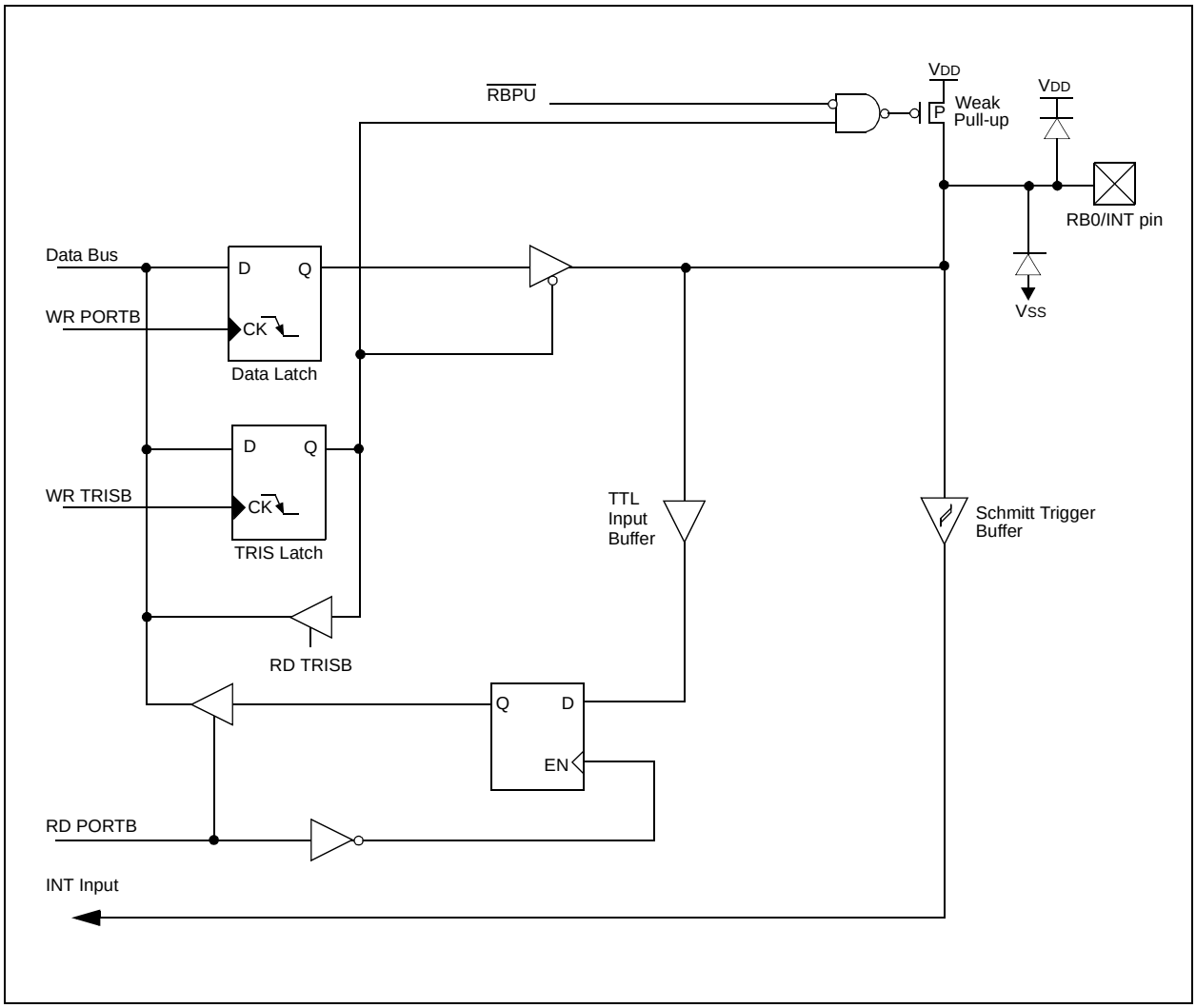
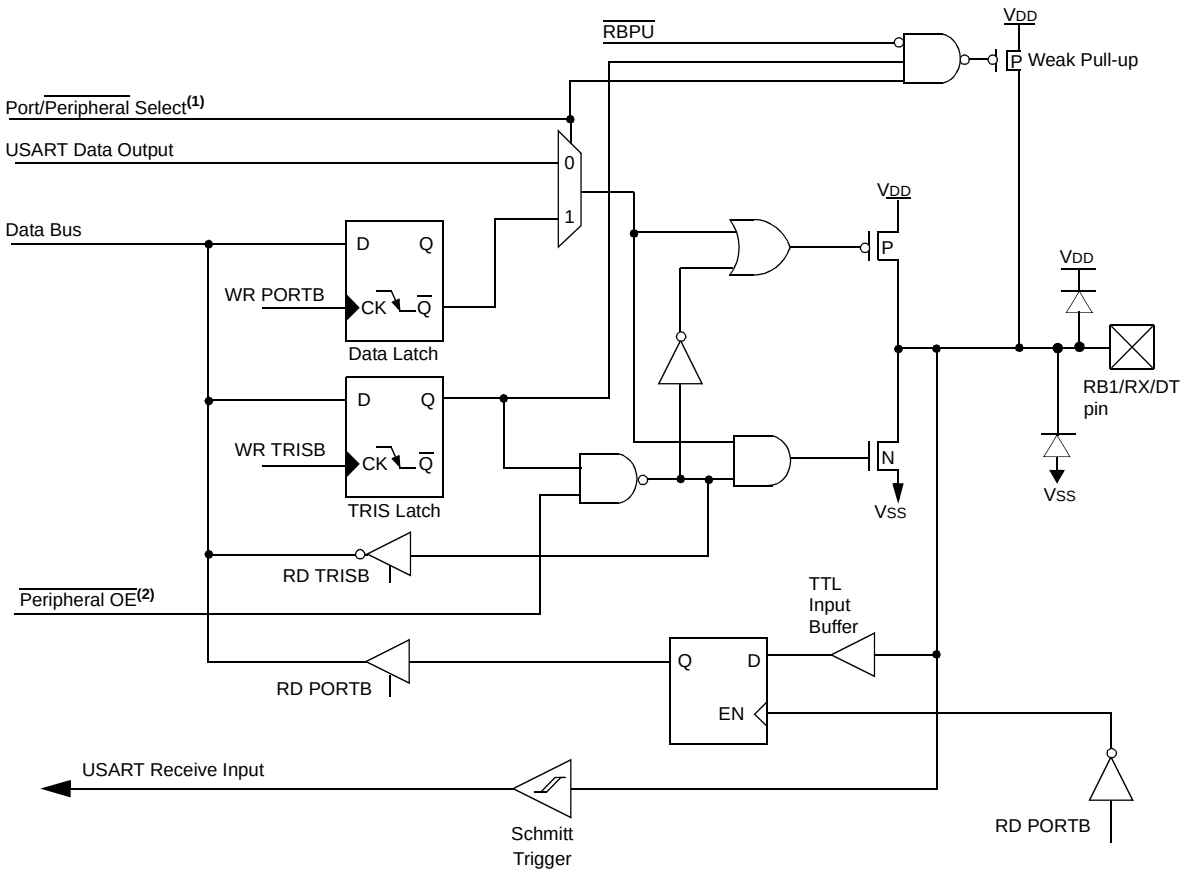
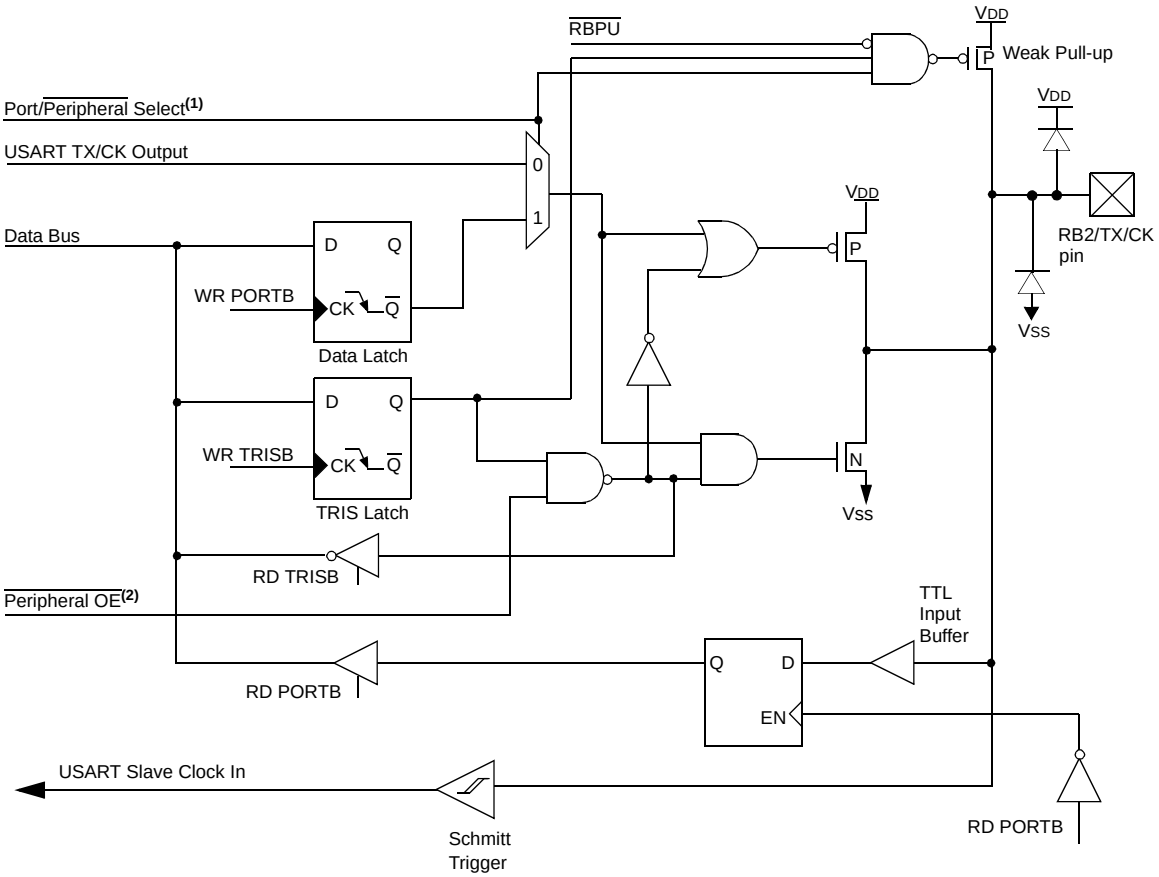


FIGURE 2: BLOCK DIAGRAM OF RB1/TX/DT PIN



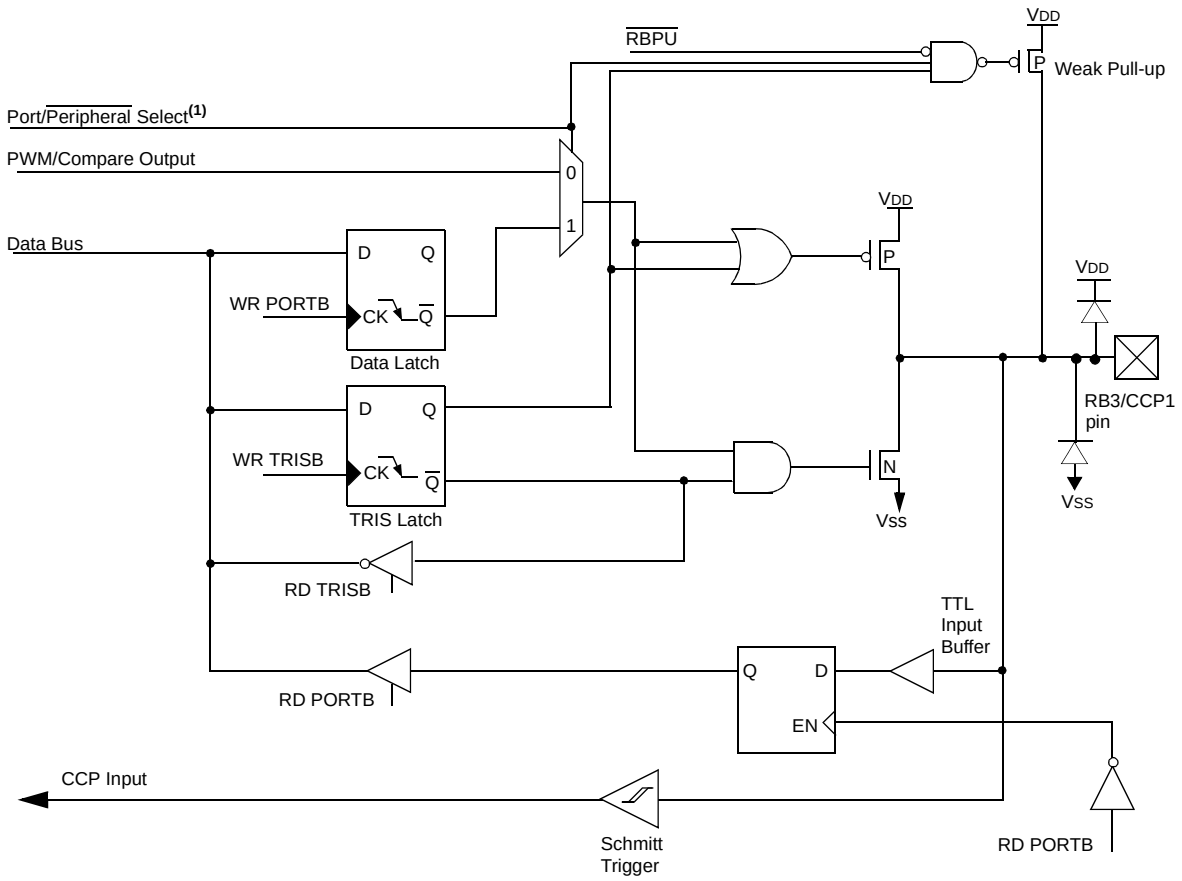
Note 1: Port/Peripheral select signal selects between port data and peripheral output.
2: Peripheral OE (output enable) is only active if peripheral select is active.

FIGURE 3: BLOCK DIAGRAM OF RB2/TX/CK PIN



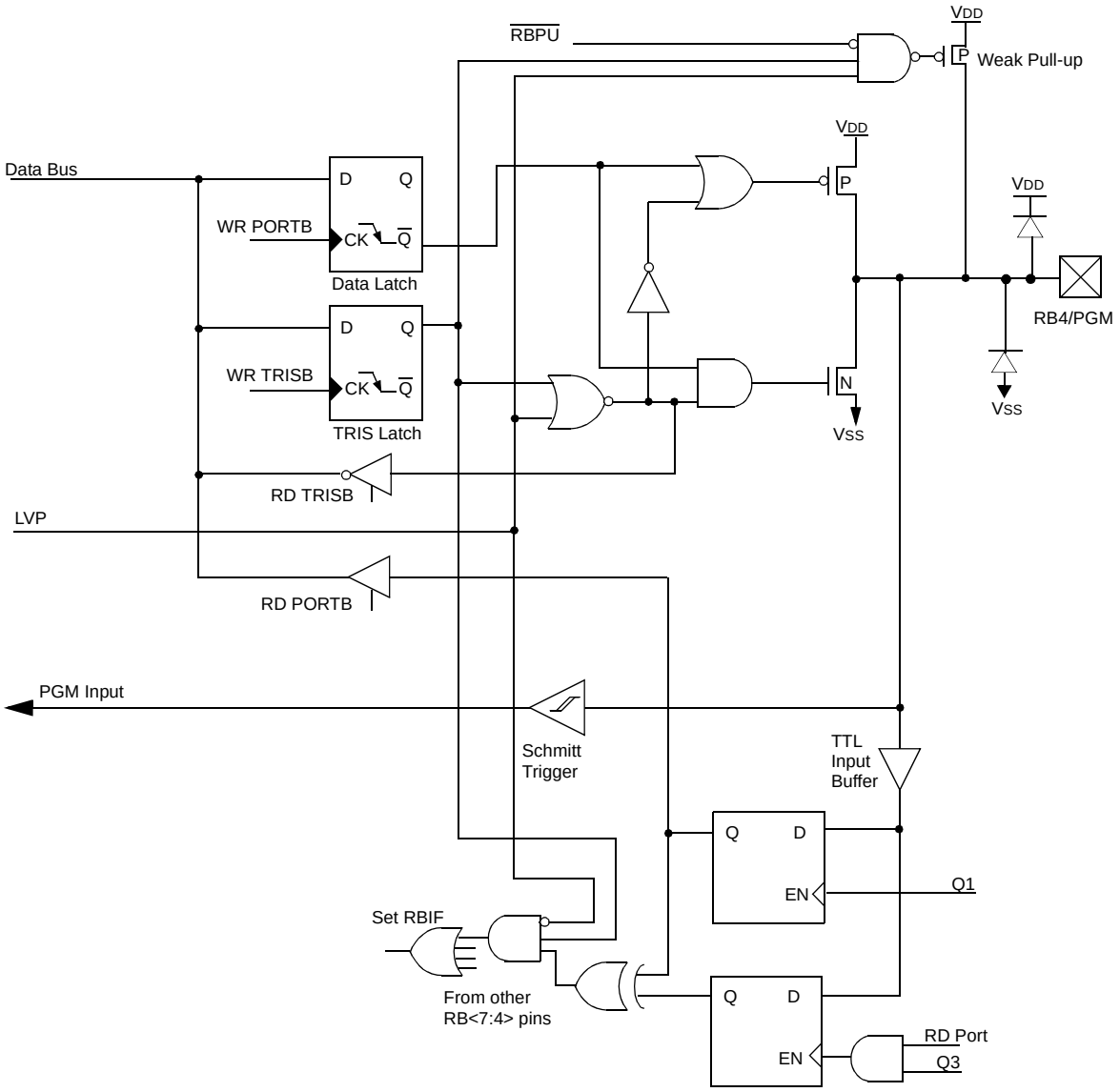
Note 1: Port/Peripheral select signal selects between port data and peripheral output.
2: Peripheral OE (output enable) is only active if peripheral select is active.

FIGURE 4: BLOCK DIAGRAM OF THE RB3/CCP1 PIN



Note 1: Peripheral select is defined by CCP1M3:CCP1M0 (CCP1CON<3:0>).

FIGURE 5: BLOCK DIAGRAM OF RB4/PGM PIN



Note 1: The Low Voltage Programming disables the interrupt-on-change and the weak pull-ups on RB4.

FIGURE 6: BLOCK DIAGRAM OF RB5 PIN

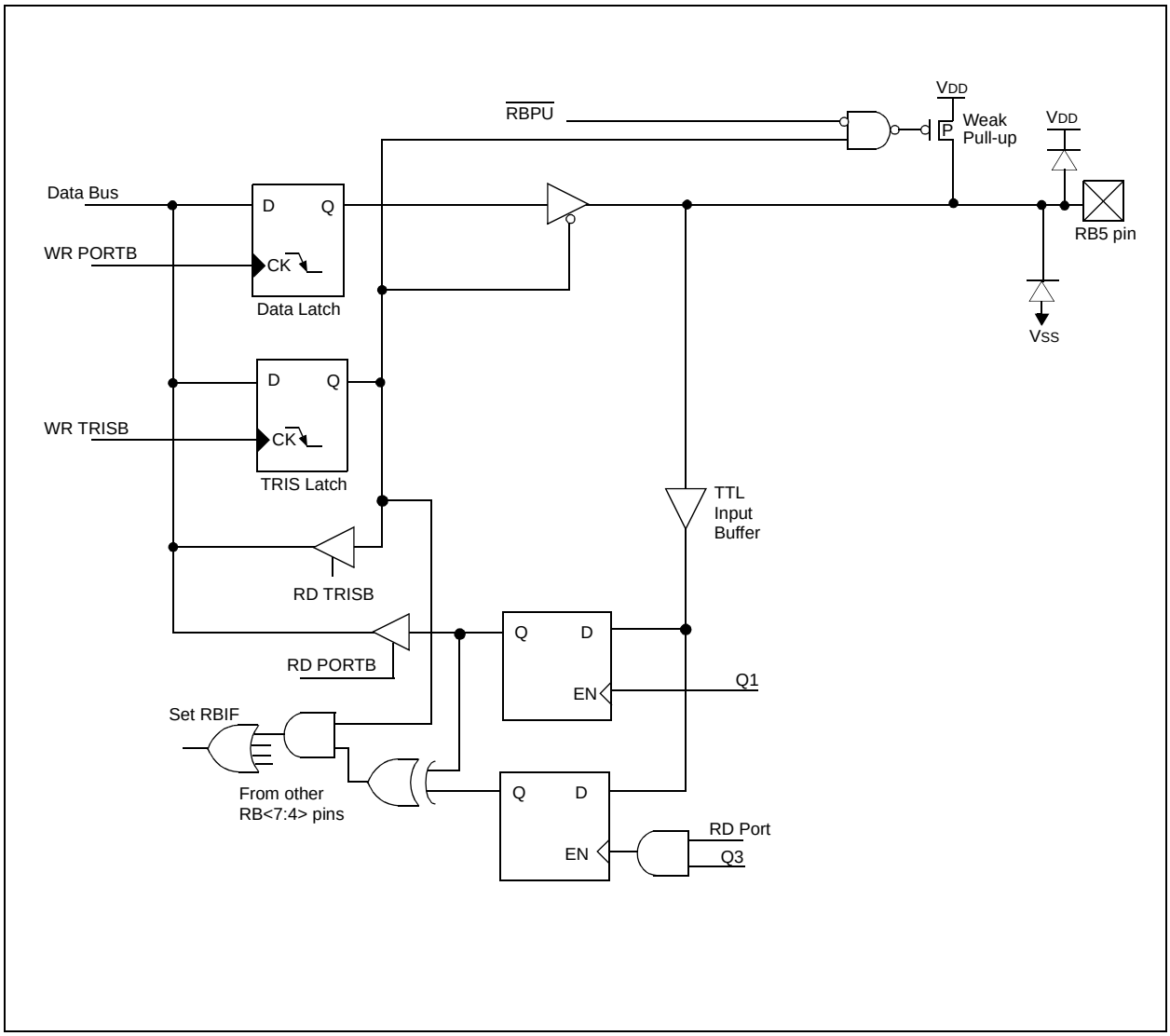


FIGURE 7: BLOCK DIAGRAM OF RB6/T1OSO/T1CKI PIN

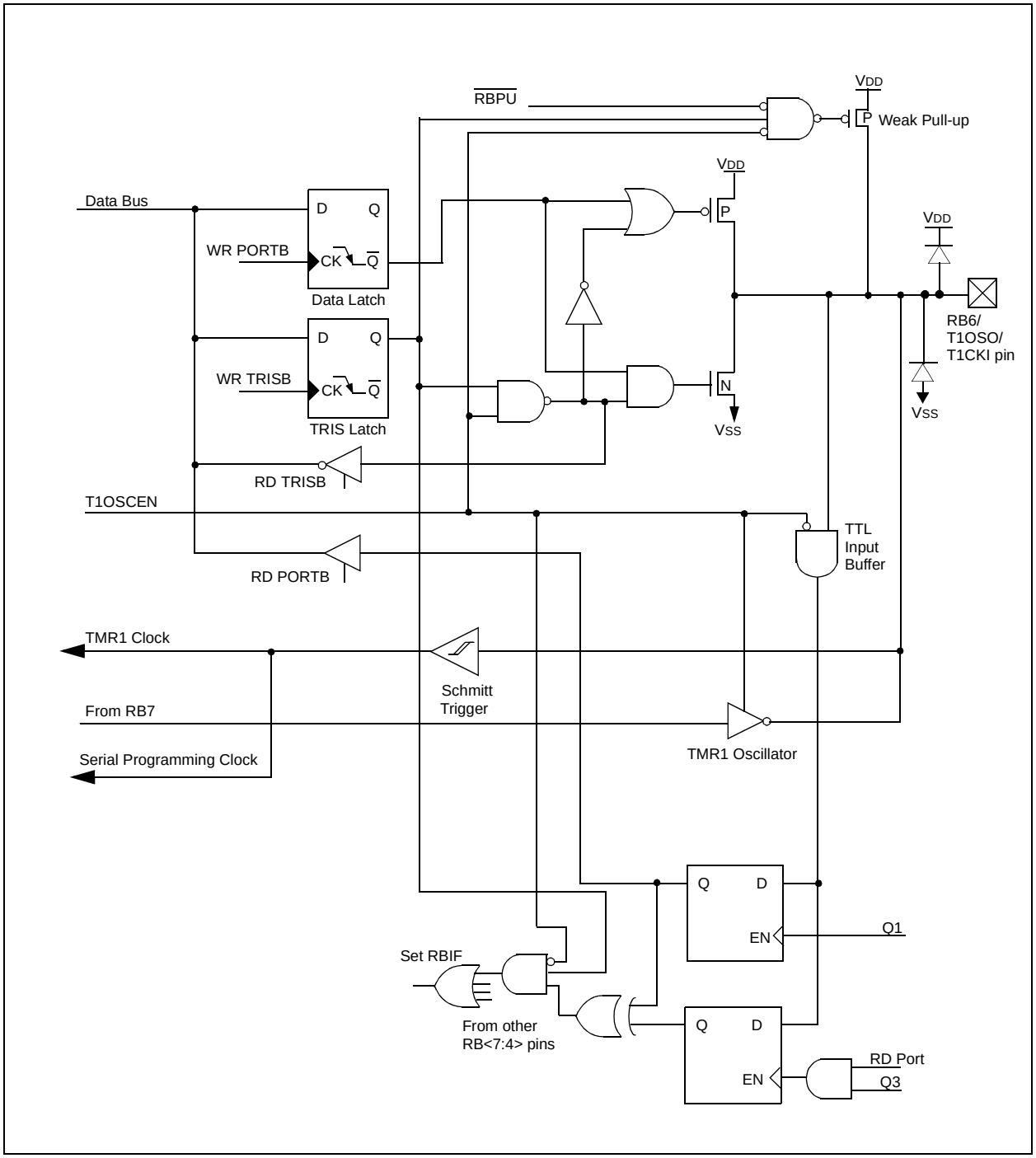
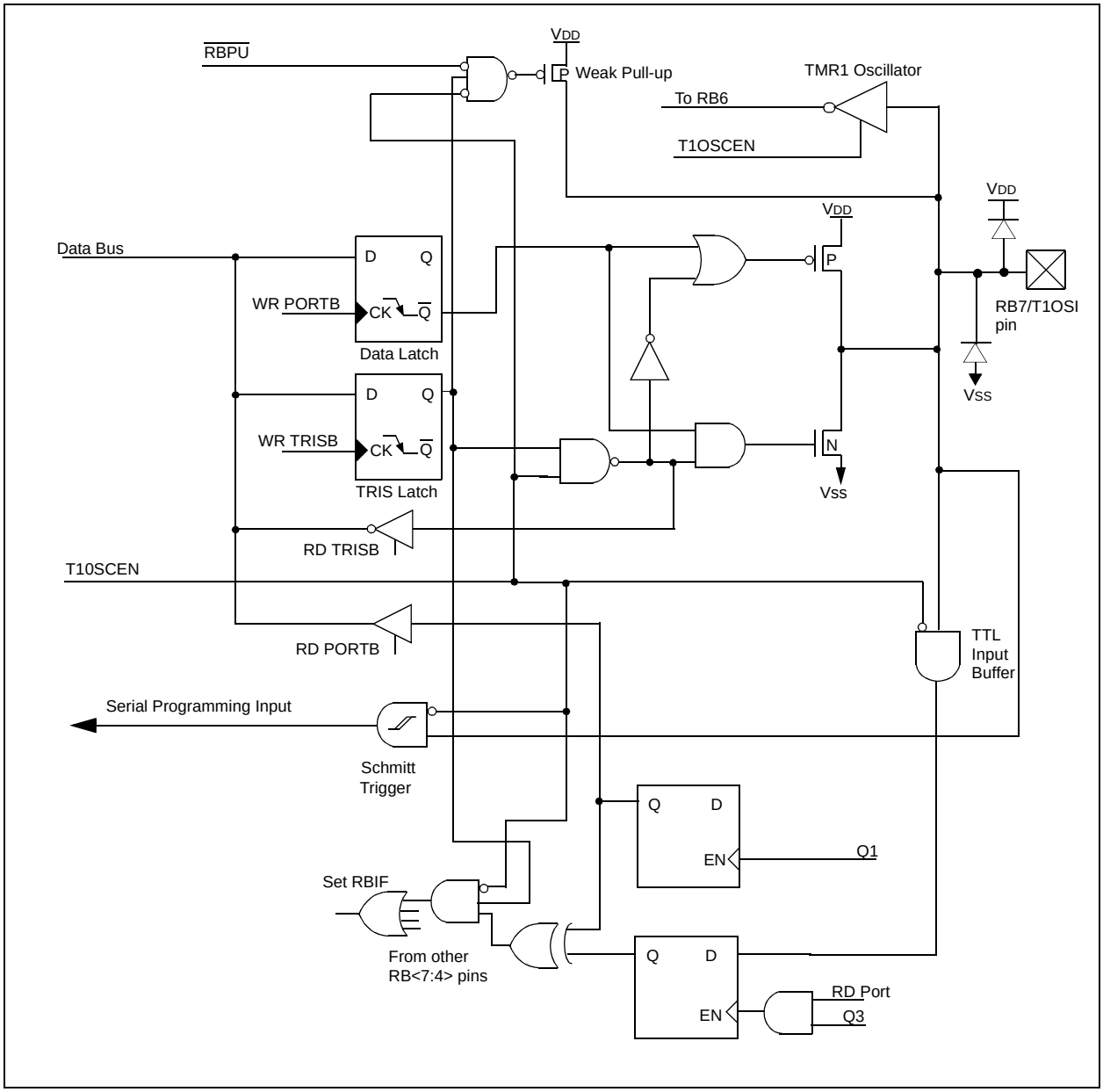


FIGURE 8: BLOCK DIAGRAM OF THE RB7/T10SI PIN



2. Module: Comparator Mode 1

Mode 1 allows AN2 to drive the (+) inputs of both comparators. AN1 continues to drive the (-) input of Comparator 2, but AN0 and AN3 can be switched into the (-) input of Comparator 1. The state of the CIS bit chooses which input is to be connected to the comparator. When CIS = 0, AN0 is attached and the comparator functions correctly. When CIS = 1, AN3 is not completely connected to the comparator, resulting in incorrect behavior.

Mode 2 is also a Multiplex mode using the CIS bit. This mode functions correctly.

All other modes are unaffected by this Errata.

3. Module: Low Voltage Programming Mode

The high voltage override for low voltage programming does not operate as specified in the programming specification. In the Low Voltage Programming (LVP) mode, the device can be programmed without using 12V on VPP (pin 4). However, when high voltage programming is used while the part has low voltage programming enabled, the Low Voltage mode is not overridden. If RB4 goes high for any reason during high voltage programming with LVP enabled, the programming will be interrupted.

Work around

Pull RB4 (pin 10) to ground during the initial programming to prevent programming interruptions. Once LVP has been disabled, it remedies this issue with RB4.

4. Module: CCP (Compare Mode)

The CCP1 output latch, observed on RB3/CCP1/P1A, can change unexpectedly when the CCP module is changed from a set output on match (CCP1CON<3:0> = “1000”) to clear output on match (CCP1CON<3:0> = “1001”) or vice versa. This condition will occur following a CCP Reset at the beginning of the third iteration of the following sequence.

- CCPR1<3:0> is changed from “1001” to “1000” or vice versa.
- The TMR1H:TMR1L register pair matches the CCP1R1H:CCPR1L register pair.

Step 1 of the third iteration will cause the CCP1 output latch to immediately and erroneously change to the inverse of the CCPR1<0> bit. This gives the appearance of an inverted CCP response to the third and subsequent compare match events.

The apparent inverted response will persist until the CCP1CON<3> bit is cleared (exiting Compare mode). Interrupts always occur correctly on the match condition. The error is only in the state of the CCP1 output latch.

Work around

Option 1

Use the CCP toggle output on Compare Match mode (CCP1CON<3.0> = “0010”).

Option 2

Since the problem occurs after two changes to the Compare and Match mode, it is only necessary to reset the CCP1CON register before the third change is made. To remain backwards compatible with earlier versions of the CCP module, always reset the CCP1CON register when changing from the clear output on Match mode to the set output on Match mode, as described in the following steps.

1. Ensure the RB3 data latch is set to 0.
2. Clear the CCP1CON register (`clrf CCP1CON`).
3. Set the CCP1CON<3:0> bits to ”1000” for set output on match.

5. Module: $\overline{\text{MCLR}}$/RA5 in LVP Mode

When the PIC16F62X device has LVP enabled, $\overline{\text{MCLR}}$ is always enabled, regardless of the CONFIG register settings.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS40300**B**), the following clarifications and corrections should be noted.

1. Module: T1SYNC (Register T1CON)

The bit T1SYNC in the Register T1CON (address 10h) should be asserted logic low (i.e., $\overline{\text{T1SYNC}}$). Table 4-1, page 15, and Table 10-2, page 65, of DS40300B should be listed as follows:

2. Module: ADEN (Register RCSTA)

The bit ADEN in Register RCSTA (address 18h), Table 4-1, is misspelled. The correct spelling should be ADDEN. This also appears in Figures and text on pages 72, 79, 80, 81, 82, 83, 84, 85, 86 and 89.

TABLE 4-1: SPECIAL REGISTERS SUMMARY BANK0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS(1)
Bank 0											
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	--00 0000	--uu uuuu
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 -00x	0000 -00x

Legend: x = unknown, u = unchanged, - = unimplemented locations, read as '0', q = value depends on condition, shaded = unimplemented

Note 1: Other (non power-up) RESETS include $\overline{\text{MCLR}}$ Reset, Brown-out Detect and Watchdog Timer Reset during normal operation.

TABLE 10-2: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, AND TIMER1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other RESETS
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	--00 0000	--uu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by Capture and Timer1.

17.1 DC Characteristics: PIC16F62X-04 (Commercial, Industrial, Extended) PIC16F62X-20 (Commercial, Industrial, Extended)

DC Characteristics			Standard Operating Conditions (unless otherwise stated) Operating temperature –40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and –40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	3.0	—	5.5	V	
D002	VDR	RAM Data Retention Voltage(1)	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	Vss	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	—	V/ms	See section on Power-on Reset for details
D005	VBOD	Brown-out Detect Voltage	3.65 3.65	4.0 —	4.35 4.4	V V	BODEN configuration bit is set BODEN configuration bit is set, Extended
D010	IDD	Supply Current(2)	— —	— —	0.7 2.0	mA mA	FOSC = 4.0 MHz, VDD = 3.0 FOSC = 4.0 MHz, VDD = 5.5*
D013			— —	4.0 —	7.0 6.0	mA mA	FOSC = 20.0 MHz, VDD = 5.5 FOSC = 20.0 MHz, VDD = 4.5*
D014			— —	— —	2.0 10	mA µA	FOSC = 10.0 MHz, VDD = 3.0*, Commercial FOSC = 32 kHz, VDD = 3.0*
D020	IPD	Power-down Current(3)	— — — —	— — — —	2.2 5.0 9.0 30.0	µA µA µA µA	VDD = 3.0, Commercial, Industrial VDD = 4.5*, Commercial, Industrial VDD = 5.5, Commercial, Industrial VDD = 5.5, Extended
D022	ΔIWDT	WDT Current(4)	—	6.0	20 25	µA µA	VDD = 4.0V, Commercial, Industrial VDD = 4.0V, Extended
D022A	ΔIBOD	Brown-out Detect Current(4)	—	75	125	µA	BOD enabled, VDD = 5.0V
D023	ΔICOMP	Comparator Current for each Comparator(4)	—	30	50	µA	VDD = 4.0V
D023A	ΔIVREF	VREF Current(4)	—		135	µA	VDD = 4.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active Operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD, $\overline{MCLR}$ = VDD;
WDT disabled.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

17.2 DC Characteristics: PIC16LF62X-04 (Commercial, Industrial)

DC Characteristics			Standard Operating Conditions (unless otherwise stated) Operating temperature –40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec Table 17-1 and Table 12-2				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	2.0	—	5.5	V	
D002	VDR	RAM Data Retention Voltage(1)	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	Vss	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	—	V/ms	See section on Power-on Reset for details
D005	VBOD	Brown-out Detect Voltage	3.65	4.0	4.35	V	BODEN configuration bit is cleared
D010	IDD	Supply Current(2)	—	—	0.6	mA	FOSC = 4.0 MHz, VDD = 2.0
			—	—	0.7	mA	FOSC = 4.0 MHz, VDD = 5.5*
D013			—	4.0	7.0	mA	FOSC = 20.0 MHz, VDD = 5.5
			—	—	6.0	mA	FOSC = 20.0 MHz, VDD = 4.5*
			—	—	2.0	mA	FOSC = 10.0 MHz, VDD = 3.0, Commercial
D014			—	—	TBD	µA	FOSC = 32 kHz, VDD = 2.0*
D020	IPD	Power-down Current(2), (3)	—	—	1.98	µA	VDD = 2.0
			—	—	9.0	µA	VDD = 5.5
D022	ΔIWDT	WDT Current(4)	—	6.0	15	µA	VDD = 3.0V
D022A	ΔIBOD	Brown-out Detect Current(4)	—	75	125	µA	BOD enabled, VDD = 5.0V
D023	ΔICOMP	Comparator Current for each Comparator(4)	—	30	50	µA	VDD = 3.0V
D023A	ΔIVREF	VREF Current(4)	—		135	µA	VDD = 3.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active Operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD,
MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

17.3 DC Characteristics: PIC16F62X (Commercial, Industrial, Extended) PIC16LF62X (Commercial, Industrial)

DC Characteristics			Standard Operating Conditions (unless otherwise stated) Operating temperature –40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and –40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC spec Table 17-1 and Table 12-2				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Unit**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O ports:					
D030		with TTL buffer	VSS	—	0.8 0.15 VDD	V	VDD = 4.5V to 5.5V otherwise
D031		with Schmitt Trigger input	VSS		0.2 VDD	V	
D032		$\overline{MCLR}$, RA4/T0CKI,OSC1 (in ER mode)	VSS	—	0.2 VDD	V	
D033		OSC1 (in XT and HS)	VSS	—	0.3 VDD	V	
		OSC1 (in LP)	VSS	—	0.6 VDD-1.0	V	
	VIH	Input High Voltage					
		I/O ports:		—			
D040		with TTL buffer	2.0V .25 VDD + 0.8V	—	VDD VDD	V	VDD = 4.5V to 5.5V otherwise
D041		with Schmitt Trigger input	0.8 VDD	—	VDD		
D042		$\overline{MCLR}$ RA4/T0CKI	0.8 VDD	—	VDD	V	
		OSC1 (EC mode)	0.8 VDD	—	VDD	V	
D043		OSC1 (XT, HS and LP)	0.7 VDD	—	VDD	V	
D070	IPURB	PORTB weak pull-up current	50	200	400	µA	VDD = 5.0V, VPIN = VSS
	IIL	Input Leakage Current(1), (2) I/O ports (except PORTA)					
					±1.0	µA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance
D060		PORTA	—	—	±0.5	µA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance
D061		RA4/T0CKI	—	—	±1.0	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1, $\overline{MCLR}$	—	—	±5.0	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	VOL	Output Low Voltage					
D080		I/O ports	—	—	0.6	V	IOL=8.5 mA, VDD=4.5V, -40° to +85°C
			—	—	0.6	V	IOL=7.0 mA, VDD=4.5V, +125°C
D083		OSC2/CLKOUT (ER only)	—	—	0.6	V	IOL=1.6 mA, VDD=4.5V, -40° to +85°C
			—	—	0.6	V	IOL=1.2 mA, VDD=4.5V, +125°C
	VOH	Output High Voltage(2)					
D090		I/O ports (except RA4)	VDD-0.7	—	—	V	IOH=-3.0 mA, VDD=4.5V, -40° to +85°C
			VDD-0.7	—	—	V	IOH=-2.5 mA, VDD=4.5V, +125°C
D092		OSC2/CLKOUT (ER only)	VDD-0.7	—	—	V	IOH=-1.3 mA, VDD=4.5V, -40° to +85°C
			VDD-0.7	—	—	V	IOH=-1.0 mA, VDD=4.5V, +125°C
*D150	VOD	Open Drain High Voltage		—	8.5*	V	RA4 pin PIC16F62X, PIC16LF62X
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin		—	15	pF	In XT, HS and LP modes when external clock used to drive OSC1
D101	CIO	All I/O pins/OSC2 (in ER mode)		—	50	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

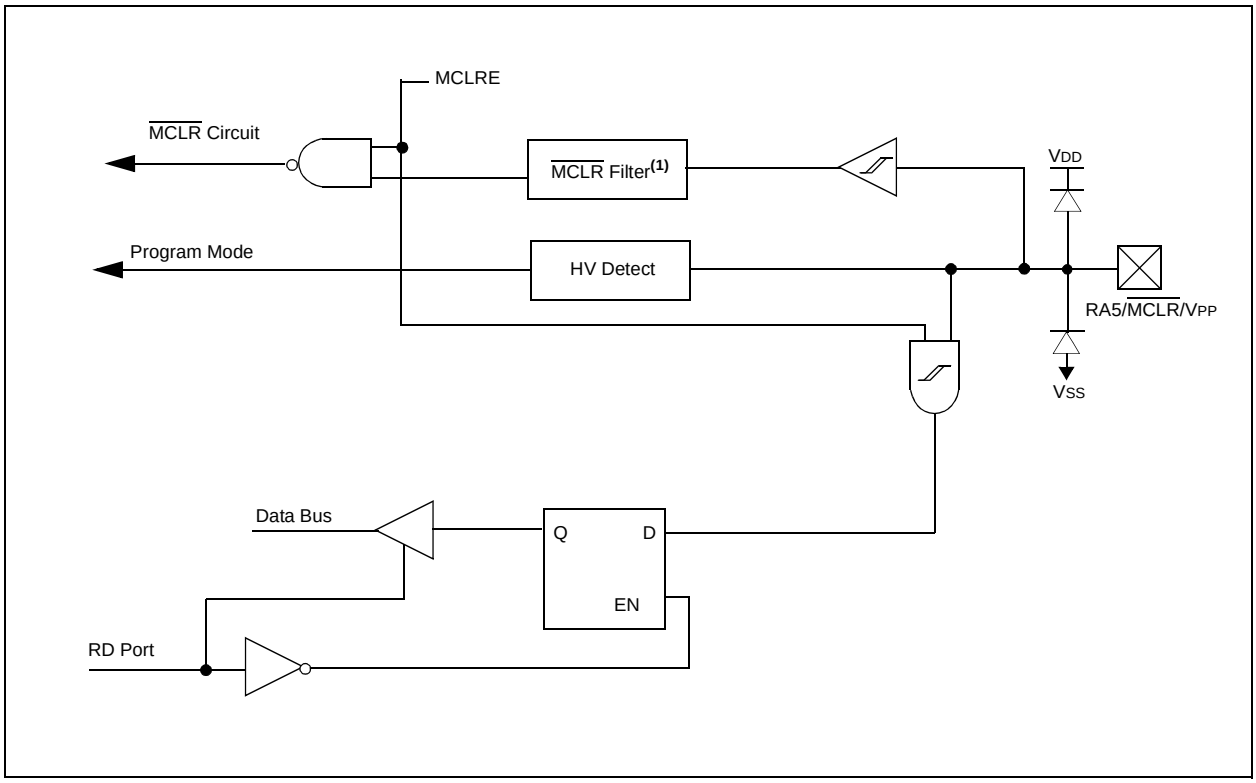
Note 1: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

2: Negative current is defined as coming out of the pin.

3. Module: I/O Ports (RA5/$\overline{\text{MCLR}}$/VPP)

The following block diagram shown in Section 5, Figure 5-5 is incorrect. The following figure should be used instead.

FIGURE 5-5: BLOCK DIAGRAM OF THE RA5/$\overline{\text{MCLR}}$/VPP PIN



4. Module: Comparator

The example given in Section 9, Example 9-1, concerning “Initializing the Comparator Module” is incorrect. The following code example should be used instead.

EXAMPLE 9-1: INITIALIZING COMPARATOR MODULE

```
        BCF         INTCON,GIE      ; Turn OFF Global Interrupts
        BCF         INTCON,PEIE     ; Turn OFF Peripheral Interrupts
        CLRF        PORTA           ; Init Port A
        MOVLW       0X03            ; Init comparator mode
        MOVWF       CMCON           ; CM<2:0> = 011
        BSF         STATUS,RP0      ; Select BANK 1
        MOVLW       0x07            ; Initialize Port A Direction
        MOVWF       TRISA           ; Set RA<2:0> as Inputs
                                    ; RA<4:3> as outputs
                                    ; TRIS<5> always reads ’0’
        BCF         STATUS,RP0      ; Select BANK 0
        CALL        DELAY10         ; Wait 10us for comparator output to become valid
                                    ; See Table 17-1 Parameter 301
        MOVF        CMCON,F         ; Read CMCON to end change condition
        BCF         PIR1,CMIF       ; Clear pending interrupts
        BSF         STATUS,RP0      ; Select BANK 1
        BSF         PIE1,CMIE       ; Enable Comparator Interrupts
        BCF         STATUS,RP0      ; Select BANK 0
        BSF         INTCON,PEIE     ; Enable Peripheral Interrupts
        BSF         INTCON,GIE      ; Global Interrupt Enable

        ; Insert Your code....

        ; Helper function is the Delay for 10us routine show below.

DELAY10             ; burns 8 cycles + the call for 10 cycles or 10us at 4Mhz
        goto $+1    ; goto the next instruction and burn 2 cycles
        call retlbl ; goto the next instruction and burn 2 more cycles
retlbl  return      ; go back and burn 2 cycles (actualy done 2x for 4 cycles consumed)
```

5. Module: Data EEPROM

The examples given in Section 13, concerning the Data EEPROM are incorrect. The EEPROM registers are all located in Bank 1. The examples show the registers in Bank 0 and Bank 1. The following code examples should be used instead to use this feature.

EXAMPLE 13-1: DATA EEPROM READ

```
BSF     STATUS, RP0  ; Bank 1
MOVLW   CONFIG_ADDR  ;
MOVWF   EEADR        ; Address to read
BSF     EECON1, RD   ; EE Read
MOVF    EEDATA, W    ; W = EEDATA
BCF     STATUS, RP0  ; Bank 0
```

EXAMPLE 13-2: DATA EEPROM WRITE

```
; set up the data and the address
BSF     STATUS, RP0  ; Bank 1
MOVLW   CONFIG_ADDR  ;
MOVWF   EEADR        ; Address to write
MOVLW   CONFIG_DATA  ;
MOVWF   EEDATA       ; Data to write

                     ; perform the write
                       operation
BSF     EECON1, WREN ; Enable Write
BCF     INTCON, GIE  ; Disable INTs
MOVLW   055h         ;
MOVWF   EECON2       ; Write 55
MOVLW   0AAh         ;
MOVWF   EECON2       ; Write AA
BSF     EECON1, WR   ; Set WR bit
BCF     STATUS, RP0  ; Bank 0
```

EXAMPLE 13-3: DATA EEPROM VERIFY

```
; after the write in complete (i.e. in the
  write interrupt)
  BSF     STATUS, RP0  ; Bank 1
  MOVF    EEDATA, W    ; load the last
                         written value into W
  BSF     EECON1, RD   ; start a read
;
; Is the value written (in W Reg) and
; read (in EEDATA) the same?
;
  SUBWF   EEDATA, W    ; the EEDATA has fresh
                         data
  BTFSS   STATUS, Z    ; Is the Zero flag set?
  GOTO    WRITE_ERR    ; NO, Write Error
                       ; YES, Good Write
                       ; continue program
```

6. Module: Comparator

Under Section 9.5 Comparator Outputs, in the fourth sentence, “When the CM<2:0> = 110 or 001, multiplexors...”, remove “or 001”.

REVISION HISTORY

Rev A Document (6/00)

Original errata document.

Rev B Document (11/00)

Issue 3 (CCP Compare Mode), Table 1 and 2 were added (page 2).

Under the Clarifications/Corrections Section, Item 1, Table 15-12 was updated with additional information (page 3).

Under the Clarifications/Corrections Section, the following Items were added:

Rev C Document (6/01)

Issues 2 and 3 were added.

Under Clarifications/Corrections, Items 2 and 3 were changed and Item numbers were renumbered accordingly.

Rev D Document (9/01)

Item 3 was rewritten (page 9).

Under the Clarifications/Corrections to the Data Sheet Section, the following items were changed:

Item 2, Tables 17.1 and 17.2, were updated with minor changes (page 11 and page 12).

Item 6 was added (page 16).

Rev E Document (2/02)

Item 4 was added, $\overline{\text{MCLR}}$/RA5 in LVP mode (page 9).

Rev F Document (4/02)

Under Clarifications/Corrections, Item 2, Tables 17-1, 17.2 and 17.3 were updated with minor changes (pages 11, 12 and 13).

NOTES:

Note the following details of the code protection feature on PICmicro® MCUs.

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable”.
- Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our product.

If you have any further questions about this matter, please contact the local sales office nearest to you.

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Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company’s quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001 certified.

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