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UNIVERSAL COINCIDENCE

Model 1446

Section 1
INTRODUCTION

The Canberra Model 1446 Universal Coincidence unit is a single-width module having five DC coupled inputs. Associated with each input is a three-position toggle switch to select coincidence (COINC), anticoincidence (ANT), or out (OUT) mode. Coincidence analysis is of the overlap type, in which an output is generated when the inputs overlap in time.

The resolving time of input A is variable from 100 nanoseconds to 2 microseconds via a single-turn screwdriver-adjustable potentiometer. A test jack is provided to permit observation of the adjustment of the pulse at input A. Resolving times of the remaining four inputs are determined by their pulse's widths.

An output pulse is obtained wherever the number of coincident pulses meets or exceeds the number selected by the COINCIDENCE EVENTS REQD rotary switch. For example, if this switch is set at "3" position, and all five inputs are being utilized in the COINC mode, the output will fire whenever a coincidence occurs between any three of the inputs. If any one or more inputs are selected for anticoincidence, the output will be inhibited while such signals are present. Two output pulses are provided—one on the front panel, and one on the rear panel. Output width and amplitude are standardized, regardless of the input widths or amount of overlap.
2.1 INPUTS

**SIGNAL INPUTS**

Five, front panel BNC connectors
Amplitude: accept +4V to +10V pulses
Pulse width: 50 nanoseconds, minimum
Input impedance: 1000 ohms; DC coupled

2.2 OUTPUTS

**OUTPUT**

Two BNC connectors (one located on the front panel and one on the rear panel)
Amplitude: +10V
Pulse width: 1 to 5 microseconds (variable via an internal potentiometer)
Output impedance: 10 ohms; DC coupled

2.3 CONTROLS

**INPUT CONTROLS**

Five three-position toggle switches (one for each input) to select Coincidence, Anti-coincidence or Out mode; selection of Out mode disables the respective input

A (Resolving Time, Input A)

A single-turn screwdriver adjustable potentiometer to adjust the resolving time of the signal at Input A over a range of 100 nanoseconds to 2 microseconds

**COINCIDENCE EVENTS REQD**

Front panel rotary switch to select the number of coincident events which must occur before an output pulse will be obtained

2.4 PERFORMANCE

**OPERATING TEMPERATURE**

0 to +50°C

2.5 CONNECTORS

**SIGNAL INPUTS**

Five front panel BNC UG-1094/U

**OUTPUT**

One front and one rear panel BNC UG-1094/U

2.6 POWER

+24V = 0mA
-24V = 0mA
+12V = 130mA
-12V = 70mA

2.7 PHYSICAL

**SIZE**

Standard single-width module (1.35 inches wide)
per TID-20893 (Rev.)

**WEIGHT**

2 lbs (0.9 kgs)
Section 3

CONTROLS AND CONNECTORS

OUTPUT
Logic signal +10V, 1 to 3 pmv.

ΔT0
Reaching zero monitor point +4.5V, 100 msec to 2 pmv.

LOGIC FUNCTION
CONTROL SWITCHES

COINCIDENCE EVENTS
RECOV
Selection of voting majority required.

ΔT0
Resolving time adjustment 100 usec to 2 msec.

REFERENCE SIGNAL
INPUT

INPUT
LOGIC SIGNAL
+4.5V, +10V, 750 nsec,
Z0 = 100 ohms, D.C.
4.1 GENERAL

The purpose of this section is to familiarize the user with the controls of the Model 1446 Coincidence module and to verify that it is operating correctly. Since it is difficult to determine the exact system configuration in which the module will be used, explicit operating instructions cannot be given. However, if the following procedures are carried out, the user will gain sufficient familiarity with the instrument to permit its proper use in the system at hand.

4.2 INITIAL OPERATION

4.2.1 SETUP

1. Insert the Model 1446 Universal Coincidence unit into an AEC compatible base unit/power supply such as Canberra Model 2000. Set the Power switch to ON.

2. Connect a Data Pulser positive output to all 5 inputs on the Model 1446 by means of coax and "T" connectors and properly terminate this line with 50 ohms.

3. Set the Data Pulser to produce a positive pulse, 1 μsec wide, at a rep rate of 10kHz, and an amplitude of 4V. Note that there is no output from the front panel output BNC.

4. Turn the input switch for Input A to COINC. Connect the 'scope to the front panel TR test point. Adjust the Δ TR pot for a pulse width of 1 μsec.

4.3 PERFORMANCE CHECK

1. Set the Model 1446 controls as follows:

   All input switches to OUT.

   COINCIDENCE EVENTS REQUIRED switch to 1

   Turn the input switch for Input A to COINC. Note that there is an output. Turn the COINC EVENTS REQD switch to 2 and note that the output disappears. Return input switch A to OUT and input switch B to COINC. Note that there is no output. Turn the COINC EVENTS REQD switch to 1 and note that the output appears. Return switch B to OUT and continue as above with C, D, and E. Each time note that there is an output when the COINC EVENTS REQD switch is in the 1 position, but no output for the 2 position.

2. Switch any two input switches to COINC; all others to OUT. Rotate the COINC EVENTS REQD switch through all 5 positions and note that there is an output for positions 1 and 2, but no output for 3, 4, and 5.

3. Switch any three input switches to COINC; all others to OUT. Rotate the COINC EVENTS REQD switch through all 5 positions and note that there is an output for positions 1, 2, and 3, but no output for 4 and 5.

4. Switch any four input switches to COINC, and the remaining input switch to OUT. Rotate the COINC EVENTS REQD switch through all 5 positions and note that there is an output for all positions except position 5.
5. Switch all five input switches to COINC. Retest the COINC EVENTS REQD switch through all 5 positions and note that there is no output for all positions.

6. Set COINC EVENTS REQD switch to 1.

a. Set input switch A to COINC and all other switches to OUT. One at a time, switch input switches B through E from OUT to ANTI to OUT and notice that the output disappears when any input switch is in the ANTI position.

b. Set input switch B to COINC and all other switches to OUT. One at a time, switch input switches A, C, D, and E from OUT to ANTI to OUT and notice that the output disappears when any switch is in the ANTI position.
5.1 GENERAL

The Model 1446 will yield an output pulse only when the number of coincident pulses, as selected by the front panel controls, overlap by at least 50 nanoseconds. The coincidence unit is made up of nine sections: Input Circuits, Resolving Circuit, Unit Gates, Summing Amp., Level Discriminator, Anti Single Shot, Wired OR Anti Circuit, Output Single Shot, and the Output Drivers. The Block Diagram of the instrument is shown in figure 1.

5.2 INPUT CIRCUIT

There are five input circuits, one for each input. They are all identical; Input A’s input circuit is made up of Q5; input B’s of Q4; input C’s of Q3; input D’s of Q2; input E’s of Q1. These input transistors are emitter followers; therefore their driving impedance is low. R1, R9, R16, and R30 provide the 1k input impedance for each input BNC. Diodes D1, D4, D7, and D10 are protection diodes by preventing the pulses to the following circuitry from exceeding 5 volts peak.

5.3 RESOLVING INPUT A

The pulse widths fed into the input BNC’s are used in the overlap coincidence measurement. This is true of all inputs except input A whose width is controlled by the Resolving Single Shot. The input circuitry of input A (Q5), is fed into Q6, which inverts input A and feeds the Resolving Single Shot made up of A3A, A3D and Q7. The two gates alone (A3A and A3D) would make a single shot, but Q7 was added to allow the range of pulse widths to be 20-1, i.e., 0.1 to 2.0usec.

The output of the Resolving Single Shot at pin 3 of A3A is inverted by A3B and appears at the Δ TR test point on the front panel, and the wiper of R5. The width of this pulse is determined by the setting of the Δ TR pot and is independent of input pulse width.

5.4 UNIT GATES

With switches S1 through S5 in CONC position, the pulses are fed to the unit gates made up of A2A, A2B, A2C, and A3C. The outputs of these gates are held high (+6 volts) by the 8.2k resistor (R6, R13, R20, R27, and R40) on each gate input which is tied to -12 volts. An input pulse to one of these gates will cause the gate output to go low (0 volts). The gate outputs only swing to ±4 volts in the high state because the two resistors tied to the output of each gate (R7 and 8 for instance) form a voltage divider from the ±5 volt supply to virtual ground. Virtual ground is formed by the summing point of the summing amplifier (junction of R50 and R53).

5.5 SUMMING AMPLIFIER

The summing amplifier is made up of Q8, Q9, and Q17. The summing amplifier is a feedback amplifier. The voltage gain of a feedback amplifier is basically $R_F/R_{in}$. Where $R_F$ is R53 which is 1k and $R_{in}$ is each 3.9k (R8, 15, 22, 29, and 77). Therefore, the basic gain of the summing amplifier for one input is $R_F/R_{in} = 1k/3.9k$ (actually 3.25) = 0.25. since the input swing, as mentioned earlier, is ±4V to GND, the output voltage swing is 4V x 0.25 = 2V for two inputs.

The same is true for inputs 3, 4, and 5. That is, for each input we will have a 3.9k resistor in parallel. So the voltage output of the summing Amp for N number of inputs is:

\[
V_{out} = \frac{N \times 4V}{3.9k} = \frac{N}{0.25}V
\]
**DESCRIPTION**

<table>
<thead>
<tr>
<th>WAVEFORM</th>
<th>WAVEFORM</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>INPUT A</td>
</tr>
<tr>
<td>2</td>
<td>INPUT B</td>
</tr>
<tr>
<td>3</td>
<td>INPUT C</td>
</tr>
<tr>
<td>4</td>
<td>OUTPUT FROM INPUT A</td>
</tr>
<tr>
<td>5</td>
<td>INPUT OF LEVEL DISC.</td>
</tr>
<tr>
<td>6</td>
<td>SUMMING AMP. OUTPUT + INPUT OF LEVEL DISC.</td>
</tr>
<tr>
<td>7</td>
<td>LEVEL DISC. OUTPUT</td>
</tr>
<tr>
<td>8</td>
<td>POSSIBLE ANTI INPUT</td>
</tr>
<tr>
<td>9</td>
<td>ANTI SS OUTPUT</td>
</tr>
<tr>
<td>10</td>
<td>ROUTING SS OUTPUT</td>
</tr>
<tr>
<td>11</td>
<td>OUTPUT TO BNC</td>
</tr>
</tbody>
</table>

**Conventions:**
- a. 3 inputs applied as shown.
- b. Coinc. events Req'd switch set to 3.
- c. No Anti inputs.

*Any width, 50ns, minimum*

* Determined by Coinc. Events Req'd switch

*Sum. Amp. inputs are waveforms 2, 3, & 4

*Indicating 3 Coinc. Events, this width is the overlapping of 3 Events

*If this occurred, waveforms 9, 10, & 11 would not exist.*

*Figure 2. Waveforms, Model 1446.*
from
\[ E_{in} \frac{R_f}{R_{in}} = E_o \]
we get
\[ 4V \times \frac{1k}{N}/4k = E_o \]
where \( N \) is the number of simultaneous inputs
Therefore
\[ E_o = \frac{N}{4} \times 4V = NV \]
This is
\[ E_o = NV \]
Therefore each input produces a one volt change in the output of the summing Amp (TF2). The summing amplifier output is at - 5V with no input and goes 1V in the positive direction for each input pulse.

5.6 LEVEL DISCRIMINATOR

The level discriminator is made up of a 710 I.C. (A5). A5 compares its two inputs; the summing Amp output (TF2) and a DC level (TP4) selected by the COINC EVENTS REQD switch (S6). Whenever the + (Positive) input of the 710 (TF2) is greater than the - (negative) input (TP4), the 710 will produce a positive pulse out. Thus, we are able to select any number of coincident inputs to yield an output. The output of the level discriminator is inverted and shaped by A4D and then fed to the anti single shot (TF3).

5.7 ANTI SINGLE SHOT

The anti single shot is made up of A6C and A6D. This single shot has a very short ON time. It also has an anti input (TF1). If the anti input is positive approximately 5V, then the anti single shot will fire for every level discriminator pulse and generate a pulse to the output circuitry. However, if the anti input is held low during the time the level discriminator is triggering the anti single shot, then the anti single shot is inhibited from firing. The anti line performs this inhibit enable function.

5.8 WIRED "OR" ANTI CIRCUIT

This circuit is similar to the unit gates in that it is made up of 5 gates (A1A, A1B, A1C, A1D, and A4B) which are held off by 8.2k resistors to -12 volts (R4, R12, R19, R26, and R39). The outputs of these gates are high (approximately +5V). However, all the outputs are tied together in wired "OR" fashion. This means that any one input can be used to arrest the coincidence circuit.

5.9 OUTPUT SINGLE SHOT

The output single shot is driven by the anti single shot. It is made up of A6A, A6B, and Q11. The width can be adjusted from 1 to 5usec by means of RV1. The output of the single shot is only approximately 5V so Q12 increases the amplitude to 10 volts.

5.10 OUTPUT BUFFERS

The output buffers are used to drive the OUTPUT BNC's. They are made up to Q13 and Q14 for the front panel BNC and Q15 and Q16 for the rear panel BNC. These buffers exhibit very low output impedances and prevent output loading from affecting the amplitude and risetime of the output pulse.
6.1 GENERAL

The purpose of this section is to provide the user with some guidelines for troubleshooting this instrument. It is not intended to be a comprehensive analysis of the circuit, but rather general outline of some quick tests that will aid a qualified technician locate a problem.

6.2 INITIAL CHECK

1. Measure the DC voltage output of the Ninbin. The Model 1446 requires ±12 volts for operation.

2. Inspect the Model 1446 for opens and/or shorts across the power input connectors. Examine all connectors to front and rear panel. Look for shorts or damaged components on the PC board.

6.3 ELECTRICAL CHECK

1. Apply power to the unit and measure the supply currents. They should be:

   +12V  —  130mA ±10%
   -12V  —  70mA ±10%

   A significant increase in current indicates a shorted component. Less current is probably an open connection. Carefully check the decoupling networks L5, C22, C23, and L6, C24, C25.

2. Measure, with the digital voltmeter, the emitter of Q10 (2N2219). It should be:

   +5V  ±0.5V

   This is the DC supply for all the integrated logic. The circuit consists of R69, X70, Q10, D23, D24, D25, C26 and C27.

3. Measure, with the digital voltmeter, Pin 6 of A5. It should be:

   -6V  ±0.6V

   This voltage is provided to the computer by R68, D22, D24, C20, and C21.

4. Connect a pulse generator to all inputs as in Section 4.

5. Set all input switches to GUT. Rotate the COINC EVENTS REQD switch through all positions and measure, with the digital voltmeter, the voltage at TP4 for each switch position. The voltage at TP4 for each position should be:

   COINC EVENTS REQD switch position = TP4 Volts

   1 = +4.62V±.323V
   2 = +3.63V±.323V
   3 = +2.64V±.323V
   4 = -1.56V±.323V
   5 = -1.67V±.323V

   If these voltages are in error, check voltage divider R60 through R65.

6-1
6. Set the COINC EVENTS REDD switch to 5. Set the ΔTR pot to 2msec width. Set all input switches to OUT and set the input pulse width and amplitude to 2msec and +10V peak. Measure, with 'scope, the level at TP2. Then switch input A to COINC and measure the positive peak on TP2. Now, add input B by switching its switch to COINC. This gives two inputs into the Model 1466.

Measure the positive peak on TP2. Then, add a third input and measure the positive peak on TP2; continue until the peak is measured for all 8 inputs. The following table lists the level for zero inputs and the level of the positive peaks on TP2 for various inputs:

<table>
<thead>
<tr>
<th>No. of Inputs</th>
<th>TP2 Volts</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-5.20V±0.35V</td>
</tr>
<tr>
<td>1</td>
<td>-4.21V±0.35V</td>
</tr>
<tr>
<td>2</td>
<td>-3.22V±0.35V</td>
</tr>
<tr>
<td>3</td>
<td>-2.23V±0.35V</td>
</tr>
<tr>
<td>4</td>
<td>-1.25V±0.35V</td>
</tr>
</tbody>
</table>

Refer to waveform timing diagram 6.

Malfunction here indicates failure of the summing amplifier or the input logic gates.

7. Connect the 'scope to the front panel ΔTR test point. Adjust ΔTR pot from one extreme to the other. The width of the pulse at ΔTR should be < 10µsec at one extreme and > 2µsec at the other. The amplitude of the ΔTR pulse should go from <+0.8V in the LOW state to >+2.5V in the HI state. Set the ΔTR width to 100msec. The ΔTR pulse is generated by the A input logic and single shot A3D, Q7, and A3A.

8. Look, with the 'scope, at the front panel output BNC and terminate this output in 93 ohms. This output should have an amplitude 10V±1V with a rise and fall time of less than 25nsec. Turn RV1 from one extreme to another and note that the output pulse width will vary from a minimum of < 1µsec to a maximum of > 5µsec. Then, set the pulse width to 2.0µsec. This signal is generated by the output Single Shot A6A, Q11, A6B, and Q12. Output drivers for the front panel are Q13 and Q14; for the rear panel are Q15 and Q16.

9. Repeat the above for the rear panel output BNC, except for varying RV1.

6.4 RETURN INSTRUCTION

In the event that you are unable to troubleshoot this instrument, you may contact the factory for technical advice or you may wish to return the instrument. Please read our warranty policy before shipping the instrument. Be sure to include a detailed description of the problem. This will help us diagnose the failure and repair the instrument quickly. For information, contact:

Customer Service Manager
Cybernet Industries, Inc.
45 Gracey Avenue
Merriden, Connecticut 06450
(203) 238-2351
Request for Schematics

Schematics for this unit are available directly from Canberra. Write, call or FAX:

Training and Technical Services Department
Canberra Industries, Inc.
800 Research Parkway, Medford, CT 06450
Telephone: (800) 255-6370 or (203) 639-2467
FAX: (203) 235-1547

If you would like a set of schematics for this unit, please provide us with the following information.

Your Name

Your Address

Univ’s model number

Unit's serial number

Note: Schematics are provided for information only. If you service or repair any to service or repair this unit without Canberra’s written permission you may void your warranty.
This warranty covers Canberra hardware and software shipped to customers within the United States. For hardware and software shipped outside the United States, a similar warranty is provided by Canberra's local representative.

DOMESTIC WARRANTY

Equipment manufactured by Canberra's Instruments Division, Detector Products Division, and Nuclear Systems Division is warranted against defects in materials and workmanship for one year from the date of shipment.

Canberra warrants proper operation of its software only when used with software and hardware supplied by Canberra and warrants software media to be free from defects for 90 days from the date of shipment.

If defects are discovered within 30 days of the time you receive your order, Canberra will repair the equipment. After the first 30 days, you will have to pay the transportation costs. This is the only warranty provided by Canberra; there are no other warranties, expressed or implied. All warranties of merchantability and fitness for an intended purpose are excluded. Canberra shall have no liability for any special, indirect or consequential damages caused by failure of any equipment manufactured by Canberra.

EXCLUSIONS

This warranty does not cover equipment which has been modified without Canberra's written permission or which has been subjected to unusual physical or electrical stress as determined by Canberra's Service Personnel.

Canberra is under no obligation to provide warranty service if adjustment or repair is required because of damage caused by other than ordinary use or if the equipment is serviced or repaired, or if an attempt is made to service or repair the equipment, by other than Canberra personnel without the prior approval of Canberra.

This warranty does not cover detector damage caused by abuse, neutrons, or heavy charged particles.

SHIPPING DAMAGE

Examine shipments carefully when you receive them for evidence of damage caused in transit. If damage is found, notify Canberra and the carrier immediately. Keep all packages, materials and documents, including your freight bill, invoice and packing list. Although Canberra is not responsible for damage sustained in transit, we will be glad to help you in processing your claim.

OUT OF WARRANTY REPAIRS

Any Canberra equipment which is no longer covered by warranty may be returned to Canberra freight prepaid for repair. After the equipment is repaired, it will pass through our normal pre-shipment checkout procedure.

RETURNING EQUIPMENT

Before returning equipment for repair you must contact your Regional Service Center or one of our factories for instructions. For detector repair, contact the Canberra Detector Division in our Meriden, Connecticut, factory for instructions. If you are going to return the equipment to the factory, you must first get an Authorized Return Number (ARN).

When you call us, we will be glad to suggest the best way for you to ship the equipment and will expedite the shipment in case it is delayed or lost in transit. Giving you shipping advice does not make us responsible for the equipment while it is in transit.

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