


Simple Low-Voltage High-Speed High-Linearity V – I Converter with S/H for Analog Signal Processing Applications
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Abstract—This paper presents a simple, high-speed, high-linear V – I converter that has the sample/hold (S/H) function and can be operated under low voltage supply. The converter will be used as the “front end” of current-mode signal processors. The proposed V – I converter circuit is comprised of a current copier and a small resistor that can be realized on chip by using polysilicon. The current copier employed in this implementation has a very small input impedance (≤50 Ω) and is settled within 0.1% in 15 ns under a power supply of 3.3 V; The high-linear V – I conversion is achieved by using a small resistor (2 kΩ). Simulation results show that, with the transistor parameters of MOSIS 2 μm CMOS technology, the converter achieves a small low-frequency THD (<−65 dB) at a sample rate of 25 MSamples/s, and consumes about 2.5 mW under a power supply of 3.3 V.

I. INTRODUCTION

As pressures increase on VLSI designers to use a lower supply voltage of 3.3 V rather than the present 5 V, current-mode signal processing techniques will become increasingly important and attractive [1]. Circuits designed to exploit current-mode techniques improve operating speed and can be implemented in low-cost digital CMOS fabrication process. Traditionally, however, most analog signal processing has been accomplished by using voltage as the signal variable. In order to maintain compatibility with voltage processing circuits, it is often necessary to convert the input and output signals of a current-mode signal processor to voltage [2]. The objective of this paper is to present a simple, fast, and high-linearity V – I converter (or, transconductor) that has the sample/hold (S/H) function, i.e., it is capable of holding the converted current, and can be operated under low power supply. The converter will be used as the “front end” of current-mode signal processors.

Numerous transconductor design schemes have been proposed and implemented [2]. However, a simple high-linear V – I converter can be realized by using a resistor and a current copier, as shown in Fig. 1, where the circuit incorporates the S/H function. The circuit is operated in two modes: sampling/conversion mode and holding mode. During the sampling period, S1 is closed and S5 is opened, the copier is in its calibration state. Note that if the copier has a very small input impedance during calibration, its input/output node “G,” serving as a virtual ground, has a potential that is virtually not affected by the input current Ii. Therefore, the relationship between the variations of Ii and VI will be solely determined by the resistor R and thus the circuit achieves high-linear conversion. On the other hand, during the holding period, switches S5 and S1 are respectively turned on and off to deliver the held current to the load. Apparently, the choice of the current copier is important for high-performance V – I converter. Numerous current copiers have been presented recently [3]–[5]. However, in addition to simple structure and high-speed operation, the current copier must have a very low input impedance during calibration and can be operated under low power supply. Therefore, this paper presents an alternative copier, differential current-storage unit, using negative feedback approach to achieve this design goal. To demonstrate the high-speed operation, the settling behavior of the V – I converter is analyzed, where the nonidealities of the switches are taken into consideration and the switches are modeled by the small-signal linearized circuit model [6]. The analysis provides a guideline for selecting appropriate device parameters.

II. PROPOSED CIRCUITS

Fig. 2 illustrates the proposed current-copier-based V – I converter. The current copier is comprised of a differential current-storage unit and a feedback amplifier. PMOS transistors M1, M2, and M4,

Fig. 1. Proposed current-copier-based V – I converter with S/H function.
constitute the differential current-storage unit, where the capacitance \( C \) memorizes the voltage needed by \( M_2 \) to support the input current flowing through \( M_1 \). The capacitor \( C \) is connected between the gate and source nodes of \( M_2 \), while the drain node of \( M_1 \) is grounded. The circuit is operated as follows. When switches \( S_1, S_2, \) and \( S_3 \) are closed, and \( S_4 \) and \( S_5 \) are opened, referred to as the sampling period, the output tracks the input. When \( S_1, S_2, \) and \( S_3 \) are opened, referred to as the holding period, the converted current is sampled and held by the current copier. During the holding period, the sampled current is read by turning on switch \( S_5 \). The amplifier is used to accurately transfer the sampled current to a current copier load by turning on switch \( S_4 \).

During the sampling period, the input node \( X \) serves as a virtual ground. The input current variation \( \Delta I_i \) can be expressed in term of the input voltage variation \( \Delta V_i \) as

\[
\Delta I_i = \frac{\Delta V_i}{R + r}
\]

where the small signal input impedance, \( r \), of the copier is

\[
r = \frac{1}{g_{M1} g_{M2} / (g_{M1} + g_{M2})}
\]

\( g_{M1} \) (or \( g_{M2} \)) is the transconductance of \( M_1 \) (or \( M_2 \)), and \( A \) is the voltage gain of the feedback amplifier. Since the sum of both drain currents, \( I_{D1} \) and \( I_{D2} \), of the transistors \( M_1 \) and \( M_2 \), is constant, increasing \( I_{D1} \), equivalent to the input current, results in decreasing \( I_{D2} \). Thus, by \( (1) \) and \( (2) \), the first-order dependence of the transconductance on the input current can be cancelled off. Equation \( (1) \) also implies that the linearity of the \( V-I \) conversion is increased with a larger resistance. In practice however, a larger resistance causes an increase of the feedback loop gain and the time constant associated with node \( X \) which decrease the loop stability and result in a longer settling time. A larger resistance also needs a larger input voltage swing to achieve the same range of dynamic output currents. This leads to a significant design trade-off among linearity, dynamic range, and conversion speed.

For high-frequency applications, large distortion may occur due to the modulation of the sample time through the input signal. To keep the distortion small it is essential that the potential at both ends of the sampling switch \( S_2 \) be only little affected by the input. Note that the potential of \( S_2 \) is determined by the gate voltage of \( M_2 \) and the variation \( \Delta V_{g2} \) can be expressed as a function of the input voltage variation \( \Delta V_i \):

\[
\Delta V_{g2} = \frac{\Delta V_i}{R g_{M1} g_{M2} / (g_{M1} + g_{M2})}
\]

Apparently, choosing large transconductances, \( g_{M1} \) and \( g_{M2} \), can reduce the variation \( \Delta V_{g2} \). Since the variation, \( \Delta V_i / R \), is determined by the dynamic range given in a design specification, sufficiently large transconductances are then selected for both \( M_1 \) and \( M_2 \) to reduce the variation \( \Delta V_{g2} \). Note that the use of large transconductance \( g_{M2} \) does not imply the increase in the charge injection error, due to \( S_2 \), because the error depends on the time constant \( g_{M1} C_2 \) [6], not on \( g_{M2} \) only. Thus, the charge injection error can still be kept reasonably small even though large \( g_{M2} \) is chosen.

For high-speed applications, fast settling time of the converter is needed. Settling time depends on the bandwidth of the CMOS inverter and the time constant \( g_{M2} C_2 \), and it may also be affected by the use of practical switches which have nonzero on-resistances and gate capacitances. The following subsection discusses the settling behavior of the proposed \( V-I \) converter and describes the design principles of choosing the device parameters for achieving fast settling time.

To study the settling behavior of the proposed converter, the non-ideal switches are modeled by the small-signal linearized equivalent circuit, as shown in Fig. 3(a) [6], where \( r_{a_k} \) and \( C_{a_k} \) are respectively the on-resistance and the half of the on-gate-capacitance of the switch \( S_k \). Based on the switch model, Fig. 3(b) illustrates the equivalent circuit of the proposed \( V-I \) converter during the sampling period. (Due to the space limitation, the detail derivations are not shown, but they are available in [7] for readers.) Based on the node-voltage equations of the equivalent circuit, we obtain a second order open-loop transfer function that can be used to estimate the main poles of the \( V-I \) converter,

\[
H(S) = \frac{I_f(S)}{I_i(S)} = \frac{(1 + \tau_{M2,g2} S)(1 - \tau_{M2,g2} S)}{\tau_{a_2} S (1 + \tau_{a_2} S)}
\]

where \( \tau_{a_k} \) denotes the time constant generated by \( r_{a_k} \) (or \( g_{a_k} \)) and \( C_{a_k} \), \( \tau_{M2,g2} = \tau_{M2} + \tau_{g2} \) and \( C_{g2} = C_{g2} + C_{g2} \). If we assume that

\[
\tau_{a_2,g2} \gg \tau_{a_2,y_1}(\text{for all } x \neq y_2 \text{ and } y \neq g_2),
\]

then both \( \tau_{a_0} \) and \( \tau_{a_1} \) can be approximated as

\[
\tau_{a_0} = \frac{\tau_{M2} g_2}{R g_{M34}}
\]

and

\[
\tau_{a_1} = \tau_{R,X_{tot}} + \tau_{M1,g2} + \tau_{R,G} + \tau_{M2,g2} + \tau_{M3,g2}
\]

where \( C_{X_{tot}} \), contributing to the time constant \( \tau_{R,X_{tot}} \), is the total capacitance on node \( X \) when both \( r_{a_1} \) and \( r_{a_2} \) are shorted, and \( C_G \) is the total capacitance on node \( G \). In the calculation of \( C_G \), the capacitance \( C_{g2} \) must be multiplied by a factor \( \beta (= g_{M2} + r_{a_2}) \) to take the Miller effect into account.

The assumption in \( (5) \) suggests that a small switch \( S_3 \) be employed to reduce the charge injection error. On the other hand, based on \( (6) \), the width of \( S_2 \) should be chosen appropriately so that the value of \( \tau_{a_1} \) is minimum. More specifically, the increase of the width of \( S_2 \) results in decreasing the corresponding on-resistance \( r_{a_2} \) and increasing the gate capacitance \( C_{X_{tot}} \). Note that the time constant \( \tau_{R,G} \) decreases as \( r_{a_2} \) decreases, while the time constant \( \tau_{R,X_{tot}} \) increases as \( C_{X_{tot}} \) increases. In other words, in \( (6) \), the term \( \tau_{R,G} \) decreases and \( \tau_{R,X_{tot}} \) increases as the width of \( S_2 \) increases. Otherwise, the term \( \tau_{R,G} \) increases and \( \tau_{R,X_{tot}} \) decreases. Therefore, there exists an optimum width of \( S_2 \) such that the value of \( \tau_{a_1} \) is minimum.
In order for the copier to achieve the shortest settling time, the optimum resistance \( R \) is chosen as follows. Consider the poles in (8). The poles can be approximated as

\[
p_{1,2} \approx -\sigma \pm j\omega
\]

where

\[
\sigma = \frac{1 + R_{GM}}{2\alpha_1} \quad \text{and} \quad \omega = \sqrt{\frac{1}{\alpha_0\alpha_0} - \sigma^2}.
\]

For a large \( R \), where \( R_{GM} \gg 1 \), the first term of the value \( \alpha_1 \) in (6) dominates. Therefore, \( \sigma \) can be represented as

\[
\sigma \approx \frac{R_{GM}}{2C_{Xtot}}
\]

and the settling time is limited by the time constant of the amplifier. On the other hand, as \( R \) decreases, \( \sigma \) becomes a constant, where

\[
\sigma \approx \frac{1}{2(\tau_{d1,sl} + \tau_{d2,sl} + \tau_{d3,sl} + \tau_{d4,sl})}
\]

The time constants associated with the device \( M_1 \) dominates and thus limits the settling time. Due to the Miller effect and the parasitic capacitances at the input, the amplifier may have a smaller bandwidth than the device \( M_1 \). Thus, the use of small \( R \) is preferred. However, as \( R \) decreases, the value of \( \alpha_0 \), in (6), increases. This may cause \( w \) to become an imaginary number even though a sufficiently small time constant \( \tau_{d1,sl} \) may be chosen. Note that the settling time is determined by the smaller absolute value of the two main poles. By (8), the lower bound of the resistance \( R \) should be limited by the condition that \( w \) is a real number. In other words, fast settling time can be achieved by choosing a small \( R \) that keeps \( w \) as a real number.

### III. Simulation Results

The proposed transconductor for \( V-I \) conversion has been simulated by PSpice, where the process parameters of MOSIS 2 \( \mu m \) CMOS technology are assumed, and the following parameters are chosen: \( R = 2 \) K\( \Omega \), \( V_{b1} = 2.1 \) V, and \( V_{b2} = 1.5 \) V. To determine its viability for low-voltage operation, the circuit uses a single 3.3 V power supply. The transistor \( M_1 \) has a bias current, \( I_{bias1} = 270 \) pA, and a constant voltage, 1.43 V, the bias voltage of the amplifier, is used as the load. The above choice is, in fact, appropriate for the use of a current copier load whose output voltage is stabilized by the amplifier while \( S_4 \) is closed. The dimensions of each transistor were chosen as follows: \( (W/L)_1 = (W/L)_2 = 500 \) \( \mu m \); \( (W/L)_3 = 600 \) \( \mu m \); \( (W/L)_4 = 30 \) \( \mu m \); and \( (W/L)_5 = 20 \) \( \mu m \). The switches are realized by CMOS transistors. Since the circuit settles within 0.1% at 15 ns, a sampling frequency 25 MHz is used in this simulation, where the control pulses for the switches have a rise and fall time of 1 ns. For a case that an input sine-wave voltage ranged between 0.55 V and 1.25 V is applied with an input frequency 200 KHz, the simulation results show that the output currents swing between 96 and 440 pA, and the total power consumption is less than 2.5 mW.

Fig. 4 shows the transconductance vs. the input frequency, where the transconductance is defined as the ratio of the amplitude of \( Ax \) over that component of the held output current \( AI_{o} \), where both have the same frequency. In this simulation, the sample frequency is 25 MHz and the sine-wave input current has a peak-to-peak value of 0.4 \( I_{bias1} \). Results show that the input impedance is about 50 \( \Omega \) for the input frequency of 2 MHz, while it is approximately 57 \( \Omega \) for 10 MHz. Since the feedback loop has a large bandwidth, a very flat frequency response is obtained, where a roll-off of about 0.05 dB results when the Nyquist frequency is reached.

Fig. 5 illustrates the THD (total harmonic distortion) versus the amplitude of the relative input currents, where the relative input current is defined as the peak-to-peak input current divided by 2\( I_{bias1} \).
the sampling frequency is 25 MHz, and the input frequency is 25/128 MHz (or, ~200 KHz). Results show that a small THD ($<-65$ dB) is obtained for input currents which swing a range of 300 $\mu$A. As the amplitude of the relative input currents is larger than 0.8, the corresponding THD increases rapidly because the small drain currents of $M_1$ or $M_2$ cause a significant settling error for the current copier.

Fig. 6 describes the THD versus the input frequency, where the sampling frequency is 25 MHz, and the amplitude of the relative input current is 0.2 (or 0.4 $I_{bias1}$). As input frequency increases, the current flowing through the gate capacitance $C$ of $M_2$ causes a voltage drop at $V_{DS}$ of $S_2$. The nonlinear relationship between the voltage drop and the capacitive current variation increases the THD. This concludes that the THD increases with the input frequency.

In summary, results show that the circuit achieves a high sampling rate, 25 MHz, large dynamic range, and low power consumption with a low power supply (3.3 V).

IV. CONCLUSION

This paper presents a simple transconductor circuit for $V-I$ conversion. The circuit is comprised of a simple yet high-linear current copier and a resistor, where the resistor can be realized on chip. Results show that a high-linearity of the $V-I$ conversion is achieved even though a small resistor is implemented. With the small resistance, a large dynamic range of the converted currents is obtained with a small swing of the input voltages. Thus, the circuit is viable for low-voltage operation. The sampling frequency of the $V-I$ conversion can be increased if the channel length of the devices is further reduced. Based on the salient features described above, the proposed circuit is well suited for high-speed and low-power signal processing applications.

REFERENCES