High Precision Voltage-to-Frequency Converter

Sidong Cai, I. M. Filanovsky
University of Alberta, Edmonton
Alberta, Canada, T6G 2E1

Abstract -- A bipolar high precision voltage-to-frequency converter is described. The circuit includes an input voltage-to-current conversion stage followed by a current-controlled multivibrator. The multivibrator trigger includes a window comparator with a limiter of the output voltage swing, and the timing capacitor discharge current is switched simultaneously with the window comparator bias. This allows to obtain high resolution near both trigger thresholds. The circuit simulation shows that the converter provides an accuracy better than 2% in the range 100Hz-100kHz of the output frequency. The breadborded circuit was tested in the temperature range -25°C to 75°C and provided the temperature coefficient of the output frequency less than 60 ppm/°C. The converter can be fabricated using an ASIC process.

I. INTRODUCTION

A lot of work has been done to develop the design methods of the circuits where the oscillation parameters (amplitude, frequency, phase, and, in multivibrators, duty cycle) provide information on the values of passive (usually resistors and capacitors) or active (current and voltage sources) external sensor elements. These values are usually functions of some other factors (mechanical force, electric or magnetic field, temperature, etc.), and the modification of oscillation parameters gives the information about these factors.

Many integrated sensors can be used as the above mentioned elements [1] and the oscillating circuits driven from such sensors became important interface circuits. The oscillating circuits with linearly controlled frequency are usually required. The frequency output being noise immune satisfies the current trend in realization of integrated sensors, namely, the demand for communication with a microprocessor. The preference is given to multivibrator circuits because the rectangular multivibrator output is easier convertible in the final digital form. Besides the multivibrators do not require an amplitude stabilization circuit, the amplitude and frequency transients are very short (their duration is about one oscillation period) and a wide frequency control can be achieved by modification of the current which is charging the timing capacitor [2]. If a multivibrator is preceded by a transconductance amplifier (i.e a voltage-to-current converter) the multivibrator becomes a voltage-to-frequency converter which can be used with wide variety of sensors.

The voltage-to-frequency converter described in this paper also includes a voltage-to-current conversion stage and a modified current-controlled oscillator proposed in [3]. Instead of a simple Schmitt trigger used in the switching circuit of [3] it was decided to use a window comparator which includes two separate input stages and a common output stage. This output stage drives the the switch of the current source discharging the timing capacitor and, simultaneously, drives a switch of the bias current for the window comparator input stages. The voltage swing of the output stage is limited which allows to keep the comparator out of saturation. This solution creates two positive feedback loops with separated switching operation near the comparator thresholds. As a result of such approach the voltage swing on the timing capacitor is nearly equal to the voltage difference between the comparator thresholds. Thus, the capacitor voltage swing, in our case, does not include a small thermodependent term distorting the converter voltage-to-frequency characteristic. The stability of the voltage difference between the thresholds was provided by a separate current source included in the circuit.

Other measures improving the linearity of the converter characteristic and its thermal behavior included introduction of the input current compensation in the window comparator and very careful design of the follower in the voltage-to-current converter feedback.

II. CIRCUIT OPERATION

A block diagram of the converter is shown in Fig. 1. The input signal is applied between $+V_{CC}$ power supply line and the operational amplifier input. The operational amplifier feedback is closed via an emitter follower. If the amplifier gain is high one can write that

$$I_T = \frac{V_{in}}{R_T} \tag{1}$$

If it is possible to neglect the feedback transistor base current (this is achieved using a compound transistor; the detailed description is given below) then the current supplied to the bottom current mirror will be equal to I_T. This current mirror supplies two currents. The first current, I_T, is mirrored by the top current mirror, and is supplied to the timing capacitor C_T. The direction of the second current, $2I_T$, is controlled by the switch S_T. During the first half of oscillation period the switch S_T in the position 1 (as shown in the Fig. 1) and the timing capacitor is charged by the current I_T from the top current mirror. During the second half of oscillation period the switch S_T is in the position 2 and the current $2I_T$ is sourced from C_T. The capacitor C_T is, hence, discharged by the current $I_T = 2I_T - I_T$. The position of the switch S_T is controlled by the window comparator output voltage v_o.

This window comparator includes two input stages and a common output stage. The timing capacitor voltage v_c is applied to the common point of the input stages. A stable reference current I_R creates the voltage drop $\Delta V_{TH} = V_H - V_L = I_R R_{TH}$. The second

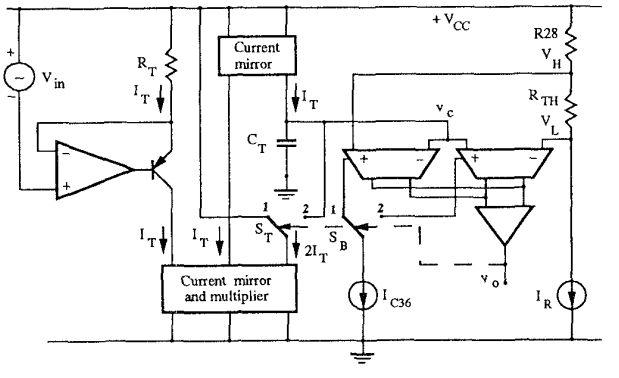

Fig. 1. Block diagram of the voltage-to-frequency converter

input of the left input stage has the potential V_H, the second input of the right input stage has the potential V_L. The voltage v_c is swinging between V_H and V_L and the swing of v_c is practically equal to ΔV_{TH}. The charge balance, thus, gives the oscillation frequency

$$f_0 = \frac{I_T}{2C_T \Delta V_{TH}} \tag{2}$$

Substituting (1) into (2) one obtains the equation of the voltage-to-frequency converter characteristic

$$f_0 = \frac{V_{in}}{2C_T R_T \Delta V_{TH}} \tag{3}$$

0-7803-2428-5/95 $4.00 © 1995 IEEE

The switching operation is following. When v_c is increasing and heading toward V_H the switch S_B which is also controlled by the output voltage v_o is in the position 1 providing the bias current I_{C36} to the left input stage. When the voltage v_c is equal to V_H the output voltage v_o changes state (in reality, this happens when v_c is slightly less than V_H). Now the switch S_T is connected to the timing capacitor and the switch S_B is in the position 2 providing the bias current to the right input stage of the window comparator. This switching of bias only is faster than switching of bias combined with switching of thresholds [4]. The bias provided to the right input stage confirms the new position of switches and the timing capacitor starts to discharge. When the voltage v_c becomes equal to V_L the output voltage changes state again, the switches S_T and S_B return to the position shown in Fig. 1, and the timing capacitor starts to charge again.

III. THE CIRCUIT IMPLEMENTATION

Implementation of the above described voltage-to-frequency converter circuit includes the following blocks.

A. Input voltage-to-current converter

The circuit of the input voltage-to-current conversion stage is shown in Fig. 2. It is a one-stage operational amplifier with external feedback via transistors Q9 to Q13. The amplifier gain is high and in the steady-state condition the base potentials of Q1 and Q2 are equal and the current I_T is determined by (1). Transistors Q11 and Q13 are connected as a combination transistor [5] which has the properties of pnp transistor and has high current gain. This allows to avoid an excessive base current (which is especially important at high I_T currents, when the current gain of pnp transistors is low). As a result the current entering the bottom current mirror (transistors Q17, Q18) is nearly equal to I_T. The Darlington circuit Q14, Q15 allows to avoid the base current losses and to repeat the current I_T at the collector of Q18. The current $2I_T$ at the collector of Q19 is obtained by proper

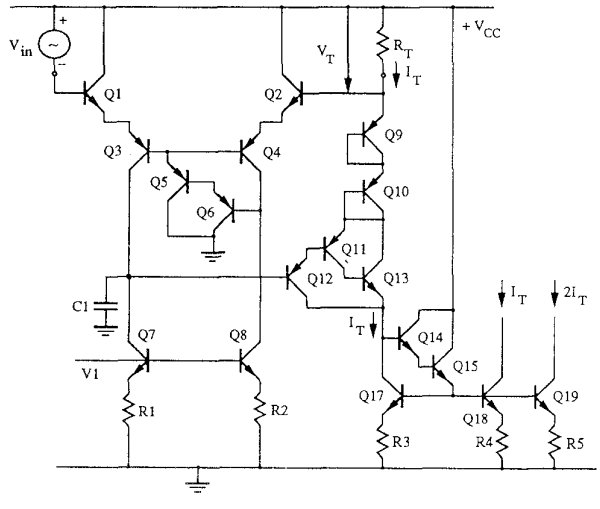

Fig. 2. Input voltage-to-current converter

design of the emitter resistance R5. The voltage V_1 is taken from the reference voltage circuit.

Capacitor C1 is used for the operational amplifier frequency compensation .

B. Timing capacitor charge and discharge circuit

The circuit which is used to charge and discharge the timing capacitor C_T is shown in Fig. 3. It includes a current mirror (transistors Q24 to Q27) which is sinking the current I_T into C_T, and a transconductance amplifier (transistors Q20 to Q23) which is used as a switch for the tail current $2I_T$ (both currents are supplied from the input voltage-to-current converter stage). The base of Q20 is driven by the voltage v_s, the base of Q22 has the potential V_R. Both are provided from the window comparator circuit described below.

When the voltage v_s is HIGH, transistors Q22 and Q23 are OFF, transistors Q20 and Q21 are ON and the current $2I_T$ is sourced from

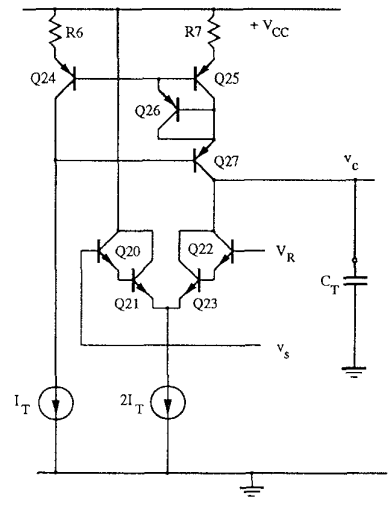

Fig. 3. Timing capacitor charge and discharge circuit

the $+V_{CC}$ line. The current I_T is mirrored by the current mirror and appears in the collector of Q27. The collector current of Q27 is charging the timing capacitor. When v_s is switched to LOW, transistors Q22 and Q23 are ON, transistors Q20 and Q21 are OFF. The tail current $2I_T$ is now intercepted by Q22 and Q23 and the timing capacitor is discharged by the difference of the tail current and the collector current of Q27. Thus, the timing capacitor is discharged by the current of the same value as the charge current.

C. Window comparator circuit

The voltage v_s driving the switching transconductance amplifier described in the previous section is obtained in the window comparator circuit (Fig. 4). This circuit includes two input transconductance stages (transistors Q50 to Q56 and transistors Q61 to Q67). The bias current of these stages is supplied by the switching transconductance amplifier (transistors Q57 to Q60). The outputs of the input transconductance stages are connected in parallel and then connected to the window comparator output stage (transistors Q68 to Q70). The timing capacitor voltage v_c is applied to the common point of the input transconductance stages. Left input of the left input stage is connected to the reference voltage V_H via an emitter follower Q49, right input of the right input stage is connected to the reference voltage V_L via a follower Q76. The bias currents I_{C35}, I_{C36}, and I_{C37} for the comparator and followers are referring to the collectors of the corresponding transistors in the full converter circuit.

Besides, the circuit includes a limiting clamper (transistors Q40 to Q43) which clamps the switching voltage v_s to a constant voltage V_R and limits the swing of v_s by $V_R \pm 2V_{BE(ON)}$.

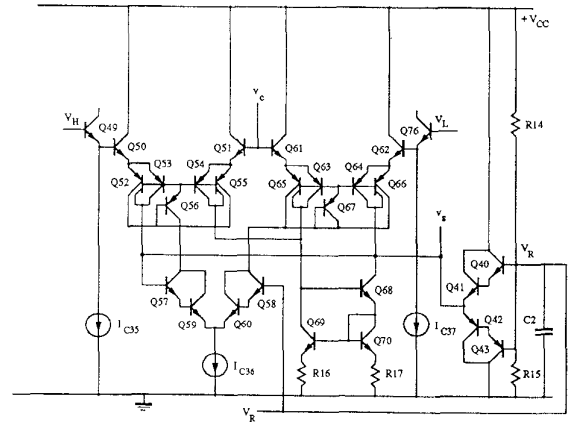

Fig. 4. Window comparator circuit

Assume that the timing capacitor is charging. Then the voltage v_s should be HIGH. If it is so then the current I_{C36} is intercepted by the transistors Q57, Q59 and supplied to the left window comparator input stage. The voltage v_c is less than V_H and the current I_{C36} will be supplied to the transistor Q52 and Q50. The transistor Q53 will develop a current which will be sinked by the transistors Q42, Q43 of the clamped limiter and the HIGH state of the voltage v_s will be confirmed (in other words, positive feedback which is necessary for the correct operation of the timing capacitor charge and discharge circuit is provided).

When the voltage v_c approaches the value of V_H the collector current of Q57, Q59 will be diverted into Q55 and Q51. The current in Q53 will disappear. The collector current in the transistor Q54 will emerge and will enter into the window comparator output stage. The voltage v_s becomes LOW and the collector current of the output stage will be sinked by Q41 and Q42.

When the voltage v_s is LOW the current I_{C36} is supplied to the right input stage of the window comparator. The voltage v_c is higher than V_L and, hence, this current will enter Q62 and will force to operate the transistor Q63. The current to the output stage will be provided. At the same time Q64 will be without current and the LOW state of v_s will be confirmed.

This change of state results in the timing capacitor discharge. The voltage v_c is decreasing now. When v_c approaches the value of V_L the collector current of Q58, Q60 will be directed into Q65 and Q67. The current in Q63 will disappear. The collector current in the transistor Q64 will emerge, the voltage v_s becomes HIGH again and all the processes will be repeated.

D. Reference voltage circuit

The reference voltage circuit (Fig. 5) includes a temperature compensated Zener diode (transistors Q84 and Q85) with the current determined by resistor R19 and series connected diodes Q79 to Q83. Transistors Q86 to Q100 represent two current mirrors: one is providing the mirroring of the current developed in the resistor R19 to Zener diode, another is providing a stable current I_{TH} (the design details can be found in [5]) in the resistor R_{TH}. Hence, a stable voltage difference $\Delta V_{TH} = V_H - V_L$ is created.

If one substitutes $\Delta V_{TH} = I_{C100} R_{TH}$ in (3) and obtains

$$f_0 = \frac{V_{in}}{2C_T R_T I_{C100} R_{TH}} \qquad (4)$$

then this results allows to estimate the stability of the oscillation frequency. The current I_{C100} is approximately inversely proportional

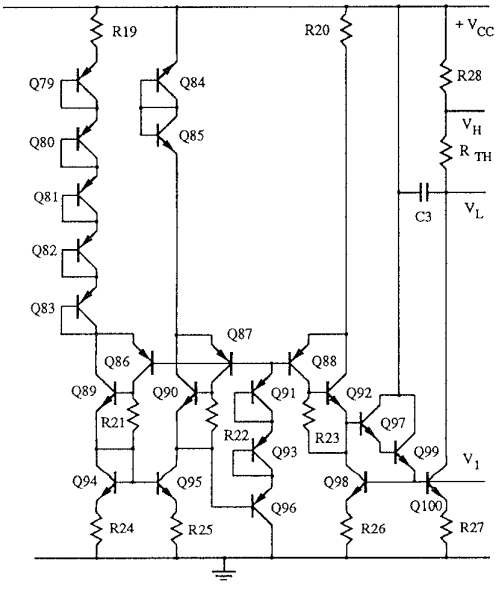

Fig. 5. Reference voltage circuit

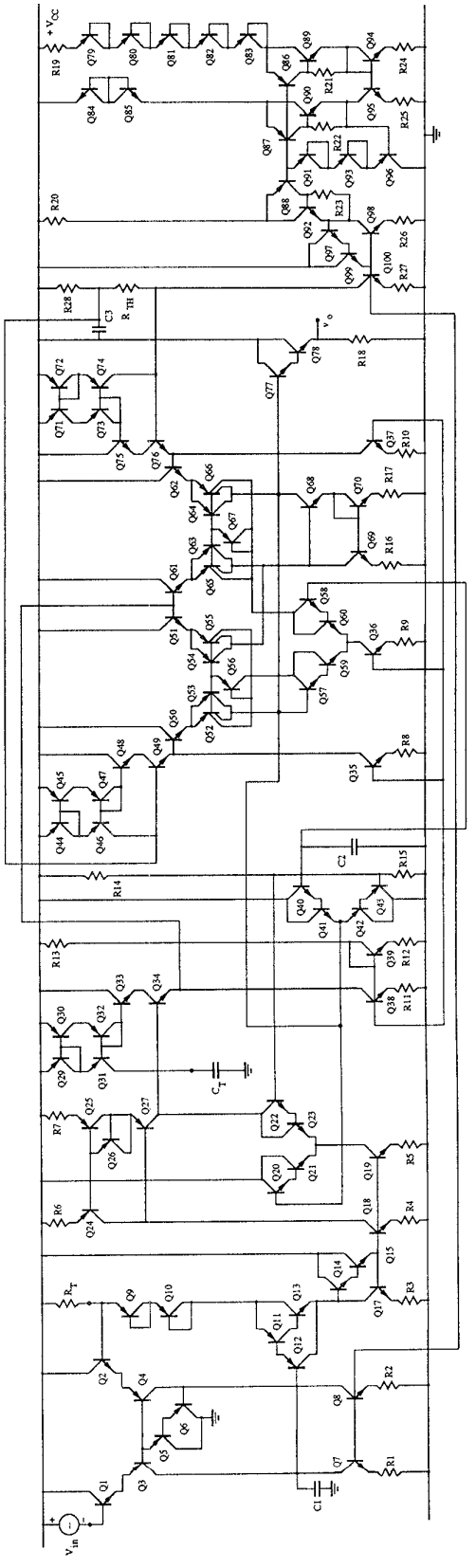

Fig. 6. The voltage-to-frequency converter circuit

to R19, then as it follows from (4), if the resistors R19 and at R_{TH} are located in the geometric vicinity on the chip the design will provide good temperature stability if the oscillation frequency (assuming that the time constant C_TR_T due to the external elements C_T and R_T have low temperature coefficient).

E. The voltage-to-frequency converter circuit

The whole circuit of the voltage-to-frequency converter is shown in Fig. 6.

In addition to the previously described subcircuits it includes an emitter follower with bias cancellation (transistors Q29 to Q34) between the timing capacitor and the window comparator. The voltages V_H and V_L are applied via similar followers as well. The output voltage is taken from the Darlington follower Q77, Q78.

The circuit design was done assuming realization by Semicustom Analog Array developed by Ferranti Interdesign [6].The circuit resistors are $R1=R2=R_{TH}=2k\Omega$, $R3=R4=400\Omega$, R5=R6=R7=R8=R9=R10=R11=R12=R16=R17=R24=R25=R26=R27=200Ω, R13=44kΩ, R14=8.5kΩ, R15=3.5kΩ, R18=6kΩ, R19=3kΩ, R20=6.3kΩ, R21=R22=R23=10kΩ, R28=3kΩ. The capacitors C1=C2=C3=47pF (polarized on-chip capacitors). The npn transistors Q19, Q98, Q100 should be double sized, as well as the pnp transistors Q24, Q25, Q27.

The circuit is designed to operate with V_{CC}=15V.

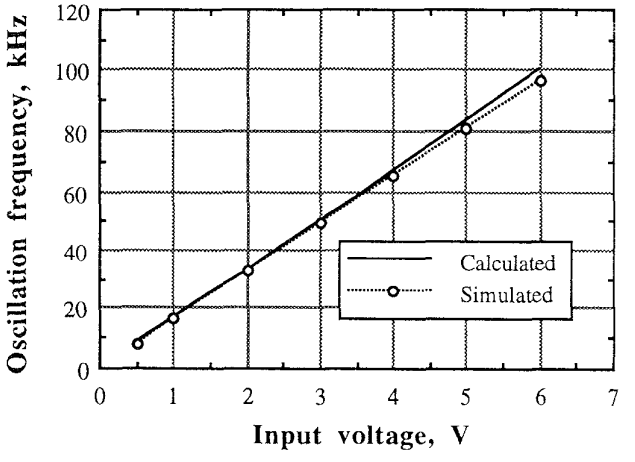

Fig. 7. SPICE simulated converter characteristic

IV. SIMULATION AND BREADBORDING RESULTS

The circuit design was verified using SPICE simulation program. The simulation results for C_T=5nF and R_T=3kΩ are shown in Fig. 7. They are compared with the calculated results obtained from (3) using C_T=5nF, R_T=3kΩ and ΔV_{TH}=2V .

The converter should provide an output square wave whose frequency is directly proportional to an input control voltage. The simulation shows that the converter operates in the range 100Hz-100kHz with the deflection from the proportionality law not more than 2% (taking into consideration that all simulation results are below the calculated line).

Besides, the circuit was breadborded and tested over -25°C to 75°C temperature range. The test shows that the temperature coefficient of the output frequency is less than 60 ppm/°C.

V. CONCLUSION

Using a window comparator with an output voltage swing limiter in the triggering circuit of a current-controlled multivibrator allows to make the voltage swing on the timing capacitor equal to the difference between threshold voltages. This difference can be done very stable applying the well known design methods for reference current sources and voltage references. The approach gives a low temperature coefficient of the oscillation frequency. Besides, this solution forces to use the window comparator bias switching. This results in a high operation speed of the triggering circuit.

REFERENCES

[1] L. Ristic, Editor, *Sensor technology and devices,* Artech House, Boston, 1994.

[2] I. M. Filanovsky, "A current-controlled multivibrator for low voltage power supply", *Int. J. Electronics,* vol.65, No 1, pp. 37-43, 1985.

[3] J. F. Kukielka, R. G. Meyer, "A high-frequency temperature-stable monolithic VCO", *IEEE J. Solid-State Circuits,* vol. SC-16, No 6, pp. 639-647, 1981.

[4] *301 analog IC designs*, Ferranti Interdesign, Inc., Scotts Valley, CA, 1987.

[5] P. R. Gray, R. G. Meyer, *Analysis and design of analog integrated circuits*, Third edition, J. Wiley, New York, 1993.

[6] *Macrochip design manual.* Ferranti Interdesign, Inc., Scotts Valley, CA, 1986.