1-Volt Ratiometric Temperature Stable Current Reference

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Abstract - **This paper presents a current reference achieving excellent behavior with regards to its temperature stability, which is able to operate under ultra-low voltage supply conditions (down to 0.9 V). Simulated results are verified by measurements on a full-custom integrated circuit. The latter includes a current reference of roughly 42 µA, and measurement depicts a temperature coefficient (TC) down to 120 ppm/°C without any adjustment, upon the military range. Due to the ratiometric property, this reference is highly reproducible. In addition, this current reference was designed to be power supply independent.**

I. INTRODUCTION

THE advent of portable electronic yields an important increase in low-voltage and low-power circuits demand. Moreover, the impressive improvements of microelectronic process lead to a sensible reduction of component dimensions. It induces a drastic reduction of the associated breakdown voltage, and therefore a need for low supply voltage. Consequently, the field of low-voltage circuit appears nowadays to be of paramount importance [1]. Due to the reduced supply voltage, the natural trend is to take advantage of the current, rather than voltage, as the main signal. Nevertheless, there is a lack in current reference able to deal with low-voltage constraints, despite their availability in more classical supply voltage range [2, 3]. This paper describes a current reference with temperature compensation, based on the ratio of resistors to provide good reproducibility. The circuit has TC in the range of 100-200 ppm/°C within the military range without external adjustment. It is fully integrable, operating under 1-Volt supply voltage, and power supply independent.

II. THE TEMPERATURE COMPENSATION PRINCIPLE

The principle we brought into play relies on the summation of two currents. Each current provides a specific temperature dependence. Assuming opposite dependencies, the sum current can depict a small, even null, temperature relationship. A positive temperature dependence can be obtained with the famous 'ΔV_{BE}' related current reference. Such a reference takes advantage of the voltage difference between two base-emitter junctions. It leads to

$$\Delta VBE = VBE1 - VBE2 = Vt \ln\left(\frac{N2 \cdot I1}{N1 \cdot I2}\right)$$

with $I1$, $N1$ and $I2$, $N2$ are respectively the current and the area of each bipolar junction, and Vt is the thermal voltage kT/q. Whenever the logarithm term is set constant, we have

$$\Delta VBE = \frac{k}{q} \ln\left(\frac{N2 \cdot I1}{N1 \cdot I2}\right) \times T = C \times T \quad (1)$$

with C to be a constant. If this voltage is applied across a resistor Rp, the associated current Ip is

$$Ip = \frac{\Delta VBE}{Rp} = \frac{C \times T}{Rp} = C' \times T \quad (2)$$

Let us assume that the resistor temperature dependence only induces second order effects, negligible within the typical range of temperature. Hence, we can write

$$\frac{dIp}{dT} = C' \quad (3)$$

and C' is clearly a positive constant. This current is generally called 'proportional to absolute temperature' (PTAT), thanks to this remarkable relationship.

On the other hand, a negative temperature dependence can be built with a V_{BE} related current reference. Indeed, it is well-known that a bipolar junction voltage provides a negative temperature coefficient. Therefore, if this voltage is applied across a resistor Ri, an associated current Ii can be related to the base-emitter voltage as $Ii = V_{BE} / Ri$.

We find $dV_{BE}/dT = (V_{BE} - V_{BG})/T$ in the literature [4], where V_{BG} is the bandgap voltage. Following the previous assumption on the temperature dependence of the resistor, we have

$$\frac{dIi}{dT} = \frac{1}{Ri}(VBE - VBG) \times \frac{1}{T} = \frac{F(T)}{T} \quad (4)$$

Although it is not a constant with regards to the temperature, it is always negative. So, it can be used to compensate the PTAT current source positive dependence.

As a matter of fact, summing Ip and Ii in a single Ic current leads to the following expression

$$\frac{dIc}{dT} = \frac{dIp}{dT} + \frac{dIi}{dT} = C' + \frac{F(T)}{T}$$

Solving for $\left[\frac{dIc}{dT}\right]_{T=T0} = 0$, we have $F(T) = -C'.T0$

Thus, with (1), (2) and (4), we obtain the relationship

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$$\frac{Ri}{Rp} = \frac{\left(V_{BG} - V_{BE}\right)}{\ln\left(\frac{N2 \cdot I1}{N1 \cdot I2}\right) \cdot Vt_0} \qquad (5)$$

So *Ic* current will present a zero temperature coefficient at a given T_0 temperature.

As (5) depends only on a resistors ratio, it implies good reproducibility as well as temperature stability. We called it the 'ratiometric temperature stable current reference', noted RTSCR.

III. Application to the Design of a Low-Voltage Current Reference

A. The PTAT Current Reference.

The Widlar's topology retained in [2] appears well suited for low-voltage application. Therefore, the same approach is merely used, with only minor changes. The chosen topology is depicted in Fig. 1.

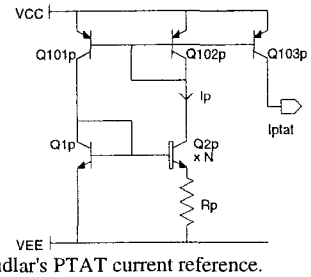

Fig. 1. The Widlar's PTAT current reference.

Assuming insignificant base currents and (Q101p, Q102p) identical pnps, it compels the currents in both Q1p and Q2p to be equal. Associated with a large geometry transistor for Q2p, it lays down to a voltage drop across Rp of $\Delta VRp = Rp.Ip = Vt.\ln(N)$, where *Vt* is the thermal voltage kT/q, and *N* the number of elementary npn used to build Q2p.

Analyzing this expression proves that the current flowing through *Rp* is perfectly PTAT, assuming that second order effects are negligible.

This PTAT current biases the overall transistors, yielding a power supply independence.

Assuming the evenness of surface for all pnps within the circuit of Fig. 1 leads to the availability of the PTAT current source at the collector of Q103p.

B. The Inverse PTAT Current Reference.

Unfortunately, the V_{BE} related current sink of [2] is no longer applicable in a low-voltage architecture.

Indeed, a 1-Volt power supply only allows the sum of a single base-emitter voltage with, at most, two collector-emitter voltages. In most cases, solely one collector-emitter voltage is allowed [1].

Therefore, as a classical V_{BE} related current source requires a base-emitter voltage across a resistor plus another base-emitter voltage for the in-line current sensor, it seems an onerous task to design a 1-Volt inverse PTAT current reference.

The principle depicted in Fig. 2 yields such a reference, even in the case of ultra-low voltage environment. The way *Ri* is connected, a base-emitter voltage is applied across it, thanks to Q1i. Of course, the current flowing through *Ri* is the sum of *Ii* and ε, assuming an insignificant base current for Q1i. Thereby, whether *Ii* is controlled by ε within a high current gain feedback loop, this leads to an insignificant ε.

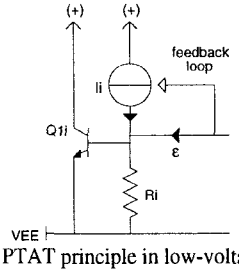

Fig. 2. The inverse PTAT principle in low-voltage environment.

On account of this value for ε, we have $\Delta VRi = Ri.Ii = VBE_{Q1i}$ which is the relationship we were looking for.

In order to build the high current gain loop, we can take advantage of the attendance of Q1i. However, as we need a negative feedback loop, another current stage is necessary to avoid a positive loop. This leads to the schematic shown in Fig. 3.

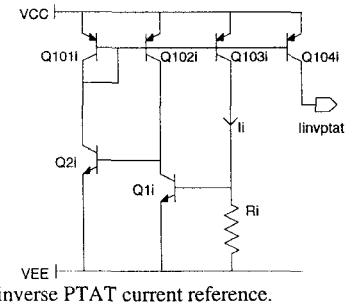

Fig. 3. The inverse PTAT current reference.

In this circuit, never more than one base-emitter voltage and one collector-emitter voltage are summed in succession. Accordingly, this topology is appropriate down to 1-Volt power supply voltage operation. This topology also provides a power supply independence, thanks to self-biasing methodology.

C. The Low-Voltage Buffered Current Mirror.

Adding both previous current generators can lead to a TC0 current reference, according to the above theoretical analysis. We only have to ensure the correct ratio for the resistors.

Nonetheless, we deal with a current reference. So its output must be buffered in order to be able to

provide biasing for numerous subcircuits within a large low-voltage integrated circuit. That is a buffered current mirror.

A classical approach, which fulfills previous requirements despite a simple arrangement, is the Emitter Follower Augmented (EFA) current mirror [5].

However, this solution is not suitable for 1-Volt supply voltage, as it overlaps two base-emitter voltage. The low-voltage mandatory adjustment consists of converting the 'column' approach of the EFA mirror in a 'row' arrangement. This is shown in Fig. 4.

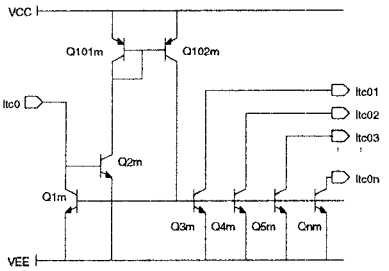

Fig. 4. The low-voltage buffered current mirror.

Supposing that the collector current of Q1m is not equal to the input *Itc0*, an error current appears which sources the base of Q2m. This error is amplified with the current gain of the BJT, mirrored within the current mirror built around Q101m and Q102m, and injected back into the base of Q1m. Hence the error current is related with the input current by $1/\beta^2$, the same way as in the classical EFA, but it works down to 800-900 mV supply voltage. As Q1m conducts the input current, connecting others BJT as (Q3m-Qnm) yields a large amount of available current sinks.

D. The Overall 1-Volt RTSCR.

Merging both previous current sources, using the buffered current mirror whenever needed, leads to the 1-Volt ratiometric temperature stable current reference depicted in Fig. 5.

This schematic shows the compensation network we connected to ensure frequency stability of the biasing cell.

In addition, start-up circuits are also depicted in Fig. 5, as the power supply independence of the RTSCR leads to a non-unique operating point for both PTAT and inverse PTAT sources.

IV. Simulated And Experimental Results

A. Parameters Computation.

According to [4], we have $V_{BG} = V_{G0} + V_t(\gamma - \alpha)$ wherein γ value is 3.2, and α is the temperature exponent of the current flowing throughout the junction. Hence, the value for α is -1 here, as the inverse PTAT source assumes self-biasing.

As Q2p is chosen twice an elementary transistor, we have at T = 300 K : V_{BG} = 1.314 Volt and $N = 2$.

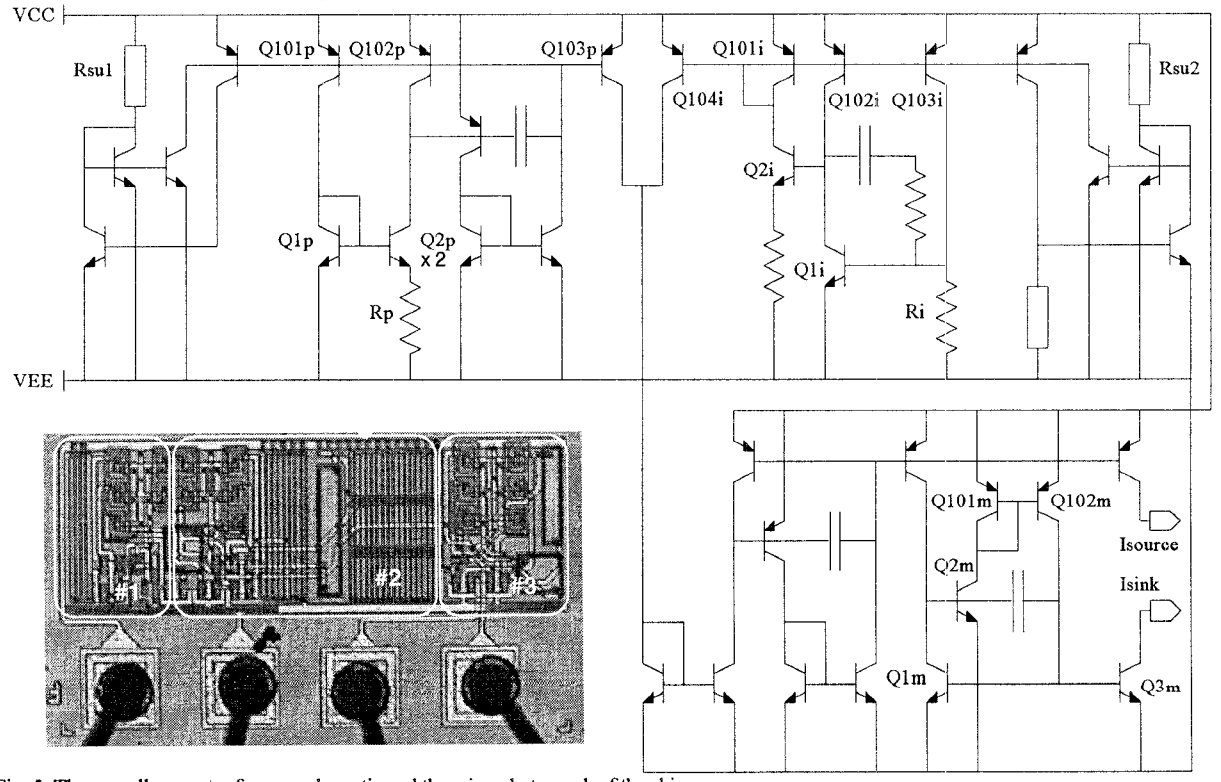

Fig. 5. The overall current reference schematic and the microphotograph of the chip.

Looking for a reference current of approximately 40 µA, with a BiCMOS technology from SGS THOMSON, it yields a V_{BE} of roughly 740 mV. According to (5), we find $Ri / Rp = 31.86$, thus $Ri / Rp \approx 32$. It is obtained with a 780 Ω for *Ri* and a 25 kΩ for *Rp*. Once simulated, these values lead to a quite perfect TC0 for the summation current of the (Q103p, Q104i) collectors.

These values are then optimized with simulations to include both temperature dependence of the output current mirrors and second order effects. This optimization is made with *Isink* reference emphasis.

B. The Integrated Circuit.

Fig. 5 shows the microphotograph of the chip. Its area is about 0.2 mm^2 (256 µm x 786 µm).We may identify 3 sections from left to right :

- section #1 is the PTAT current source,
- section #2 is the inverse PTAT current source,
- section #3 represents the two low-voltage buffered output current mirrors.

The measured overall circuit consumption, in 1-Volt supply voltage operation, is 384 µA.

C. Temperature compensation.

Assuming a 1-Volt supply voltage, the integrated circuit of Fig. 5 is simulated with HSPICE. It gives the results depicted in Fig. 6.

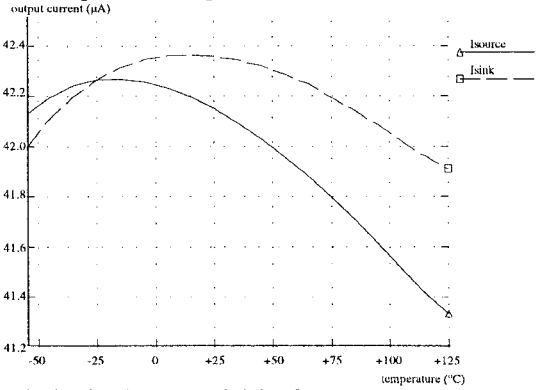

Fig. 6. Simulated source and sink references versus temperature

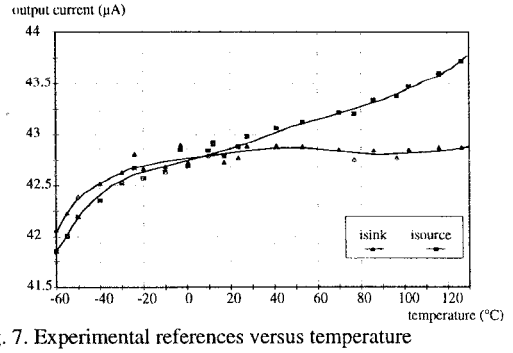

Fig. 7. Experimental references versus temperature

Using the temperature coefficient definition proposed in [4], we calculated 53 and 119 ppm/°C for *Isink* and *Isource* respectively, within the military range of temperature. Assuming identical conditions than simulation ones, experimental results are depicted in Fig. 7. TC of 120 and 250 ppm/°C for *Isink* and *Isource* has been respectively measured.

Despite the fact that these values are higher than the expected ones, it is still a remarkable result, as no external adjustment was done to obtain these temperature coefficients.

D. Power Supply sensitivity.

Experimental measurements depicted in Fig. 8 show that the current references are scarcely dependent of the supply voltage, and perform correctly down to 875 mV supply voltage. This proves the efficiency of the low-voltage approach used to design the RTSCR.

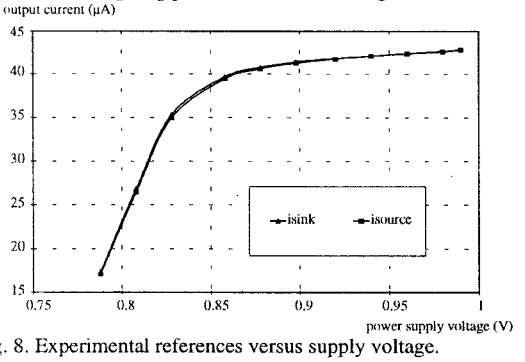

Fig. 8. Experimental references versus supply voltage.

V. CONCLUSION

A 1-Volt ratiometric temperature stable current reference has been designed and fabricated. TC of 120 and 250 ppm/°C are measured without external adjustment. Moreover, it is power supply independent and works down to 875 mV supply voltage. This will be integrated within ultra-low voltage current-mode circuits, providing an excellent stability with regards to temperature.

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