Stable Differential Voltage to Frequency Converter with Low Supply Voltage and Frequency Offset Control

D. McDonagh and K. I. Arshak

Abstract—In this paper, the circuit for a new bipolar differential voltage-to-frequency converter is presented. The circuit operation and the calculation of the operating frequency are described. The circuit design is also realized using Zetex transistor array integrated circuits and a 3.3-V power supply. This circuit incorporates an adjustable operating frequency via an external capacitor. The operating frequency varied from 15 to 368 kHz by changing the external capacitor from 1 µF to 22 pF. The circuit was tested with an applied differential voltage of ±15 mV. The deviation about the center frequency changed from ~±2.1 Hz to ~±38.22 kHz as the external capacitor was varied over the same range. The frequency offset control feature was implemented using a 4-bit current DAC (iDAC). As the iDAC input code was increased from 0 to 1111, the operating frequency varied quite linearly from ~156.5 to ~77.9 kHz. Thermal simulations with worst-case analysis were performed in PSPICE in order to estimate the thermal coefficient of frequency for the circuit. These simulations yielded a TC of ±192 ppm/°C for the operating frequency.

Index Terms—Current-to-frequency converter, frequency offset control, VCO, voltage-to-frequency converter.

I. INTRODUCTION

VOLTAGE-to-frequency conversion is desirable for many applications such as phase-locked loops in communications and sensor-based data acquisition systems including biomedical instrumentation and telemetry. Extensive work has been reported in the literature on bipolar voltage-to-frequency conversion [1]–[7]. Most of these circuits are based on the classical emitter coupled multivibrator with floating capacitor or grounded capacitor topologies. The emitter coupled multivibrators have a wide range of linear frequency control (about four decades) and operate at high frequencies (up to 10 MHz). However, they require a power supply of 15 V. Different techniques for temperature stability of the output frequency have been reported yielding temperature coefficient (TC) values as low as 20 ppm/°C below 100 kHz [1]–[3]. However, as the oscillation frequency increases, the TC deteriorates quickly due to the effect of parasitic capacitance.

The grounded capacitor topologies can work at lower supply voltage (5 V) and still have three to four decades of frequency control [5]–[7]. Van Dijk and Huijsing [7] have designed an AC bridge-to-frequency converter system based on a relaxation oscillator. The highest reported operating frequency for a grounded capacitor topology circuit has been 20 MHz with a TC of ±60 ppm/°C over a temperature range of 0–75°C [5]. However, most commercial IC’s have an upper operating frequency usually limited to 100 kHz with typical values of 10 kHz in frequency control application [8], [9].

In recent years, low-voltage and very-low-current design has become a major issue, especially in data acquisition systems and short-range low-frequency radio communications [10]. This trend is mainly driven by an urgent need for portability and the growing relative cost of power supplies and heat removal systems. It has now become essential to design new systems with strict requirements on low power and at least the same performance, accuracy, and dynamic range.

In this work, a new bipolar differential voltage-to-frequency converter with a low supply voltage and a low temperature coefficient (TC) of frequency is designed as the signal conditioning circuitry for an external transducer, i.e., strain gauge. In general, the mechanical balancing of bridge networks may be difficult due to electrical interference and possible physical constraints, hindering mechanical changes of some network elements. To overcome these drawbacks, the balancing procedure should be automated using hardware and/or software techniques. Discrete hardware bridge balancing techniques have been reported in the literature [11], [12]. These techniques involve discrete differential amplifiers, ADC’s, DAC’s, and computers/microcontrollers. As part of this work, the strain gauge network is balanced, i.e., differential input voltage ∼0 V, using a current DAC (iDAC), thus eliminating the need for conventional mechanical balancing of network components.

II. CIRCUIT OPERATION AND IMPLEMENTATION

The bipolar differential voltage-to-frequency converter described in this work includes a transconductance amplifier, a current-to-frequency converter with a grounded capacitor, a selectable TC voltage reference, and a 4-bit iDAC. All the circuits work from a 3.3-V supply. The input is compatible with common transducers, i.e., strain gauges, photocells, etc., and is well suited for applications such as remote sensing or
telemetry. Fig. 1 illustrates the transconductance amplifier (Q1 to Q11 and R3, R2) and the selectable TC voltage reference (Q12 to Q20 and R3 to R6). The differential stage Q1/Q2 is used to convert the input differential voltage (V_{in}) to a current I_{o} that is linear over a small voltage range (approximately ±30 mV). The input differential voltage may be produced by such circuits as resistor dividers or Wheatstone bridge networks containing transducers such as strain gauges. In Fig. 1, the differential input voltage is provided by the voltage reference (collector voltage of Q3) and the resistor divider containing R0 and a strain gauge resistor (Rg + ΔRg). The value ΔRg is the resistance deviation from the nominal Rg when the gauge is under strain. The bias current is set by the resistor R1 and fed into the differential stage via the current mirror Q10/Q11/R2. The subscript “3” beside transistor Q11 refers to a Zetex n-p-n transistor with three emitters. This bias current sets the gain of the transconductance amplifier. This current is split by the differential stage into I_{1} and I_{2} (currents through Q1 and Q2, respectively), passed through a network of current mirrors and then subtracted to form the output current I_{o}. The current through Q1 is mirrored by Q2/Q5, whereas the current through Q2 is mirrored twice, i.e., the Wilson current mirrors Q4/Q6 and Q5/Q8/Q9 and subtracted from I_{1} at the output. It should also be noted that the positive temperature coefficient of the current mirror Q10/Q11/R2 compensates for the temperature dependence of g_{m}, which is the transconductance of the differential stage.

The demand for a stable voltage reference is almost universal for electronic design. The voltage reference in Fig. 1 is based on the IC bandgap reference by Brokaw [13]. For the purpose of the discussion, Q17 will be referred to as a single transistor having an emitter area of four times that of the transistor Q28. When implemented, Q17 is composed of two identical Zetex 700 Series n-p-n transistors, each with two emitters connected in parallel. The emitter scaling ratio of Q17 and Q18 generates a ΔV_{BE} of [13]

\[ \Delta V_{BE} = \frac{kT}{q} \ln \left( \frac{4I_{BE18}}{I_{BE17}} \right) \]  

which is developed across the resistor R6. At low currents during the start-up stage, the current through Q17 will be greater than that through Q18 and, thus, activates the current mirror Q14 and Q15. The resulting current through Q16 forces Q19 and Q20 to raise the output voltage at the emitter of Q20. The common rising voltage at the bases of Q17 and Q18 will cause Q18 to conduct more current. When the currents through Q17 and Q18 are equal, the common voltage at the bases will no longer increase. The current in Q18 can only equalize that of Q17 since the loop is closed; therefore, (1) becomes

\[ \Delta V_{BE} = \frac{kT}{q} \ln(4) \approx 36 \text{ mV}. \]  

Hence, the voltage across R7 is

\[ V_{IT} = 2 \frac{R_{7}}{R_{6}} \frac{kT}{q} \ln(4). \]  

The voltage at the base of Q18 is the sum of V_{BE} and V_{IT} and is temperature dependent. The TC value of this voltage can be selectable set by varying R6/R6. The output voltage is determined by the ratio of R6 to R0. The start-up circuit Q12 and Q23 is automatically rendered inactive as the reference voltage settles.

Fig. 2 illustrates the current-to-frequency converter. This circuit has separate charging and threshold subcircuits. The external capacitor C is charged and discharged via the switch current mirrors Q26 to Q20, Q32 and Q33. The threshold circuit involves the resistor ladder R_{10} to R_{12}, the differential amplifier Q21 and Q22, and feedback to the switching current and resistor ladder are via Q_{30}, R_{13}, and R_{14}. The threshold circuitry effectively acts as a Schmitt trigger. These two subcircuits (charge and threshold) are driven in parallel by the capacitor voltage V_{c}, hence, maintaining high switching speed and low-voltage power supply operation. At the first moment when V_{cc} is switched on, the capacitor C is discharged, and V_{c} > 0. The transistor Q21 of the differential pair is off while transistor Q22 is on. The threshold voltage V_{th} is at its maximum value (V_{th})

\[ V_{th} \approx \frac{(V_{cc} - V_{BE33})R_{11}}{(R_{10} + R_{11})} + V_{BE33}. \]  

In (4), the base current of transistor Q22 is neglected. In addition, the transistors Q30, Q31, and Q32 are off, and Q33 is on. Since the transistor Q22 is off and Q33 is on, I_{in} is mirrored twice, i.e., through the transistors Q28 and Q26, and
the capacitor $C$ charges. The voltage $V_c$ increases linearly, and when it is close to the upper threshold voltage $V_{sH}$, transistor $Q_{22}$ of the differential pair starts to turn on. The bias current set up by $Q_{21}/Q_{22}/R_{17}/R_{18}$ then flows via $Q_{21}$, and the collector current of $Q_{22}$ decreases. At this point, $Q_{30}$, $Q_{31}$, and $Q_{32}$ all turn on while $Q_{33}$ turns off. The transistor $Q_{31}$ effectively shunts $R_{12}$ to near ground since $Q_{31}$ is in saturation, and the collector node of the transistor appears to be a low impedance ($\approx 20$ to $500 \, \Omega$, depending on the device structure and the collector current [14]). The voltage $V_s$ jumps down to its lower threshold value ($V_{sL}$)

$$V_{sL} \approx \frac{(V_{oe} - V_{CE(sat)31})R_{14}}{(R_{10} + R_{11})} + V_{CE(sat)31}. \quad (5)$$

With the transistor $Q_{32}$ on and $Q_{33}$ off, the current $I_o$ is mirrored through $Q_{21}$. This discharges the capacitor $C$, and the voltage $V_c$ linearly decreases. When it becomes approximately equal to $V_{sL}$, the transistor $Q_{21}$ switches off. As a result, $Q_{30}$, $Q_{31}$, and $Q_{32}$ switch off, $Q_{33}$ switches on, the voltage $V_s$ returns to its upper threshold value $V_{sH}$, and the periodic cycle begins again.

The frequency of oscillation can be calculated with satisfactory precision if the upper and lower threshold values of the capacitor voltages, i.e., $V_{cH}$ and $V_{cL}$, are known at the moment of the jumps. In this case, the deviation of the charging and discharging current in the short period of time just before a transition is neglected in the calculation. Even though the current-to-frequency converter contains a Schmitt trigger, the upper and lower threshold capacitor voltages $V_{cH}$ and $V_{cL}$ are not equal to the Schmitt trigger threshold voltages at $V_{sH}$ and $V_{sL}$. Fig. 3 illustrates the Schmitt trigger differential pair setup for the switching between $V_{sH}$ and $V_{sL}$ and visa versa. From this figure, the relation between the capacitor threshold voltages and the Schmitt trigger threshold voltages can be realized as

$$V_{cH} \geq V_{sH} + \delta V_+ \quad (6)$$
$$V_{cL} \leq V_{sL} + \delta V_- \quad (7)$$

where $\delta V_+$ and $\delta V_-$ are equal to $(V_{be21(off)} - V_{be22(on)})$ and $(V_{be21(on)} - V_{be22(off)})$, respectively. Expressions for the collector currents $I_{c21}$ and $I_{c22}$ at the moment of jumps must be calculated in order to find the values of $\delta V_+$ and $\delta V_-$. This calculation can be performed using the loop transfer function [3], [4]. In breaking the closed loop between the base of $Q_{22}$ and the node labeled $V_s$, the loop gain ($V''/V'$) can be estimated to be

$$\frac{V''}{V'} \approx \frac{R_{10}/R_{11}}{1/gm21 + 1/gm22}. \quad (8)$$

At the moment of jumps, the loop gain is equal to unity, and therefore

$$R_{10}/R_{11} = 1/gm21 + 1/gm22. \quad (9)$$

It is assumed that the transistors $Q_{21}$ and $Q_{22}$ are matched; hence, $gm21 = L_{21}/V_T$ and $gm22 = L_{22}/V_T$, where $V_T$ is
26 mV at room temperature [14]. From the circuit, it is also clear that

\[ I_{24} = I_{c21} + I_{c22}. \]  

(10)

From (9) and (10), and the expressions for \( g_{m21} \) and \( g_{m22} \), the collector currents \( I_{c21} \) and \( I_{c22} \) have the quadratic form

\[ P_{21} - I_{24}I_{21} + \frac{I_{24}V_T}{R_{10}||R_{11}} = 0 \]  

(11)

\[ P_{22} - I_{24}I_{22} + \frac{I_{24}V_T}{R_{10}||R_{11}} = 0 \]  

(12)

yielding

\[ I_{21\pm} = \frac{I_{24}}{2} \left( 1 \pm \sqrt{1 - \frac{4V_T}{(R_{10}||R_{11})I_{24}}} \right) \]  

(13)

\[ I_{22\pm} = \frac{I_{24}}{2} \left( 1 \mp \sqrt{1 - \frac{4V_T}{(R_{10}||R_{11})I_{24}}} \right) \]  

(14)

for both transitions of the capacitor voltage. The values of \( \delta V_+ \) and \( \delta V_- \) can now be calculated as

\[ \delta V_+ = V_T \ln \left( \frac{I_{21+}}{I_{c21+}} \right) \]

\[ = V_T \ln \left( \frac{1 + \sqrt{1 - 4V_T/(R_{10}||R_{11})I_{24}}}{1 - \sqrt{1 - 4V_T/(R_{10}||R_{11})I_{24}}} \right) \]

\approx V_T \ln \left( \frac{I_{24}(R_{10}||R_{11})}{V_T} \right) \]  

(15)

\[ \delta V_- = V_T \ln \left( \frac{I_{21-}}{I_{c21-}} \right) \]

\[ = -V_T \ln \left( \frac{1 + \sqrt{1 - 4V_T/(R_{10}||R_{11})I_{24}}}{1 - \sqrt{1 - 4V_T/(R_{10}||R_{11})I_{24}}} \right) \]

\approx -V_T \ln \left( \frac{I_{24}(R_{10}||R_{11})}{V_T} \right). \]  

(16)

The difference between the upper and lower capacitor threshold voltages is

\[ \Delta V_c = V_{cH} - V_{cL} = V_sH - V_sL + [\delta V_+ - \delta V_-] \]  

(17)

and can be simplified to

\[ \Delta V_c = (V_{BE33} - V_{CE(sat)33}) \left( 1 - \frac{R_{11}}{R_{10} + R_{11}} \right) + 2V_T \ln \left( \frac{I_{24}(R_{10}||R_{11})}{V_T} \right). \]  

(18)

The capacitor \( C \) is charged by the current \( I_0 \); hence, the charge current \( I_c \) is

\[ I_c = I_0 \]  

(19)

and the charge time \( T_C \) is equal to

\[ T_C = C\Delta V_c / I_c. \]  

(20)

The discharge current \( I_D \) is

\[ I_D = I_0 + \frac{I_{CE21}}{\beta_{F21}} \]  

(21)

where the base current of \( Q_{21} \) is included. This current has a detrimental effect when \( I_0 \) is of the same order of magnitude. The discharge time becomes

\[ T_D = C\Delta V_c / I_D. \]  

(22)

Hence, the oscillating frequency is

\[ f_0 = \frac{1}{T_c + T_D} = \frac{I_c I_D}{C\Delta V_c (I_c + I_D)}. \]  

(23)

Fig. 4 illustrates the 4-bit iDAC. This iDAC is based on binary-weighted current sources (\( Q_{20} \) to \( Q_{24} \)) in conjunction with an \( R-2R \) ladder (\( R_{31} \) to \( R_{38} \)). The subscript beside the transistors \( Q_{20} \) to \( Q_{24} \) indicates the number of emitters in order to achieve the binary-weighted currents. Differential current switching [15] is implemented using a lateral p-n-p voltage comparator stage (\( Q_{36}, Q_{37}, R_{10} \) to \( R_{21} \)) driving an n-p-n differential pair (\( Q_{34} \) and \( Q_{35} \)). The circuit diagram for the voltage reference \( V_r \) has been omitted since it has the same circuit configuration as the voltage reference in Fig. 1. It can be observed in Fig. 1 that the output of the iDAC is connected to the base of transistor \( Q_1 \) and the resistor divider containing \( R_Q \) and a strain gauge resistor \( (R_g + \Delta R_g) \) (the node labeled “\( x' \)”). The function of the 4-bit iDAC is to provide control over
III. EXPERIMENTAL AND SIMULATED RESULTS

The circuits in Figs. 1, 2, and 4 were realized using Zetex 700 series bipolar transistor arrays and simulated using PSPICE. The circuits were tested and simulated using $V_{cc} = 3.3$ V. Fig. 5 illustrates the output current $I_o$ from the transconductance amplifier versus the input voltage $V_{in}$. From the graph, it can be observed that the output current $I_o$ is linear over a range of $\sim 60$ mV, and the gain is $0.0888$ mA/V. This linear range is sufficient since the typical range of $V_{in}$ is $\pm 15$ mV for the strain gauge used in this work [16]. The strain gauge is a thick film planar piezoresistive device ($R_g = 5 \, k\Omega$) exhibiting a $\Delta R_g/R_g$ value of $\sim 1.1 \times 10^{-2}$ for a microstrain ($\mu e$) of 1000. This corresponds to a gauge factor (GF) of 11 (GF = $|\Delta R_g/R_g|/\varepsilon$).

Fig. 6 illustrates the output frequency versus the input differential voltage for the circuits implemented using Zetex transistors and a PSPICE simulation ($C = 0.1$ nF). The input differential voltage $V_{in}$ is controlled by sinking a current that is proportional to the iDAC binary input from this node, hence achieving control over the output frequency of the current to frequency converter.

The output current $I_o$ from the transconductance amplifier versus the input differential voltage is shown in Fig. 5. From the graph, it can be observed that the output current $I_o$ is linear over a range of $\sim 60$ mV, and the gain is $0.0888$ mA/V. This linear range is sufficient since the typical range of $V_{in}$ is $\pm 15$ mV for the strain gauge used in this work [16]. The strain gauge is a thick film planar piezoresistive device ($R_g = 5 \, k\Omega$) exhibiting a $\Delta R_g/R_g$ value of $\sim 1.1 \times 10^{-2}$ for a microstrain ($\mu e$) of 1000. This corresponds to a gauge factor (GF) of 11 (GF = $|\Delta R_g/R_g|/\varepsilon$).

Fig. 6 illustrates the output frequency versus the input differential voltage for the circuits implemented using Zetex transistors and a PSPICE simulation ($C = 0.1$ nF). The output frequency is calculated to be 140.350 kHz, whereas the experimental value was 135.723 kHz.

Fig. 7 illustrates the output frequency versus the input differential voltage at different $C$ values. From Fig. 7(a) and (b), it can be noticed that the central frequency can be varied from 15 Hz to 368 kHz (five decades) by decreasing the capacitor $C$ from 1 nF to 22 pF. The maximum deviation in frequency from the central frequency increases from $\sim 2.1$ Hz to $\sim 38.22$ kHz as the capacitor $C$ decreases over the same range.

The effect of temperature on the output frequency was also an important issue in the design since temperature would have a direct consequence on the accuracy of the circuit. Fig. 9 illustrates the simulated output frequency versus ambient temperature of the differential voltage-to-frequency converter. The capacitor $C$ was set to 0.1 nF, whereas the output frequency increases. In addition, close matching is observed between the simulation results and the circuits implemented using Zetex transistor arrays. Any deviation between the two results can be attributed to differences in the actual and the ideal transistor and resistor tolerances. The linearity of the implemented circuit results was calculated to be $0.186\%$. It is easy to verify that (23) gives frequency values that are in very good agreement (<3.5%) with those obtained from the implemented circuit. For one particular circuit setup, the values of $V_{in} = 15$ mV, $I_o = 13.197 \mu A$, $V_{BE33} = 0.71915$ V during charging, and $C = 0.1$ nF. The current $I_{CF21}$ is equal to the bias current setup by $Q_{24}/Q_{25}$ (9 \mu A) since no current flows in $Q_{22}$ during discharge. The gain $\beta_{F21} = 190$ at 9 \mu A (from the Zetex data sheet). The resistor ladder $R_{40}$, $R_{11}$, and $R_{12}$ are set to $5R_b$, $2R_b$, and $16R_b$, where $R_b$ is the 700 Series resistor value (750 $\Omega$). The value $V_{CE33(sat)}$ is obtained from a Zetex data sheet ($V_{CE33(sat)}$ versus $I_{CE}$). The initial estimate of $I_{CF21}$ is equal to the current flowing in the resistor ladder during charging, which is $(V_{cc} - V_{BE33})/(R_{40} + R_{11})$ and yields a value of 491.59 \mu A. From the data sheet, the initial estimate of $V_{CE(sat)33}$ is 0.125 V. The current $I_{CF21}$ is recalculated using the equation $(V_{cc} - V_{CE(sat)33})/(R_{40} + R_{11})$ for discharging, and the more accurate value of $V_{CE33(sat)}$ is estimated from the data sheet. This value is finally 0.132 V. From the values given, the frequency $f_o$ was calculated to be 140.350 kHz, whereas the experimental value was 135.723 kHz.
resistor $R_7$ was varied in selectable TC voltage reference. Both the resistors $R_6$ and $R_7$ are external resistors. The temperature range of interest was centered around room temperature ($25^\circ$C). From the figure, it is clear that when $R_7$ is 1.1 kΩ, the output frequency deviation about 25°C is quite minimal.

Subsequently, the resistor $R_7$ was set to 1.09 kΩ to achieve the ideal minimum temperature coefficient of frequency (TCF), and a worst-case analysis with a parametric temperature sweep was executed in PSPICE. This simulation yielded a TC of $\pm 192$ ppm/°C for the output frequency. This TC value may be considered excellent for a semi-custom circuit design where only diffused resistors are available and not thin film resistors, which can be laser trimmed.

**IV. CONCLUSIONS**

The design, implementation, and simulation of a new differential voltage to frequency converter ($\delta$VFC) with frequency offset control has been presented. The calculation of the operating frequency was also described. The differential voltage-to-frequency conversion was performed using a transconductance amplifier and a current-to-frequency converter while the frequency offset control was implemented using a current DAC. An external capacitor was used to vary the operating frequency of the $\delta$VFC circuit. The maximum frequency deviation achieved about the center frequency for an input voltage of $\pm 15$ mV was $\sim \pm 38.22$ kHz. The iDAC varied the operating frequency of the circuit quite linearly over its effective linear range. The thermal coefficient of frequency for the circuit was simulated using PSPICE, producing a excellent value of $\pm 192$ ppm/°C.

**REFERENCES**


D. McDonagh received the B.Eng. degree in electronic engineering (microelectronics) in 1991 from the University of Limerick, Limerick, Ireland. In 1994, he received the Ph.D. degree in the modeling of resolution enhancement processes in microlithography while working in the Microelectronic and Semiconductor Research Group at the University of Limerick.

From 1994 to mid-1998, he was a Research Fellow at the University of Limerick. He continued his research in microlithography and worked in CMOS and bipolar analog circuit design. He now works for Integrated Device Technology, Inc., Atlanta Design Center, Atlanta, GA.

K. I. Arshak received the B.Sc. degree in physics from Basrah University, Basrah, Iraq, in 1968, the M.Sc. degree from the University of Salford, Salford, U.K., in 1979, and the Ph.D. degree in solid state electronics from Brunel University, London, U.K., in 1986. He received the D.Sc. degree from Brunel University in 1998.

He has worked as a Lecturer of Physics at Basrah University and a Senior Research Scientist at Novotech Ltd., Limerick, Ireland. Currently, he is a Senior Lecturer in semiconductor technology and solid state electronics at the University of Limerick, where he is the leader of the Microelectronic and Semiconductor Research Group. He has published numerous papers in solid-state devices, VLSI process, and thin-film and thick-film technology.

Dr. Arshak was elected a Fellow of the Institute of Physics in 1998.