Level Shifters for High-Speed 1-V to 3.3-V Interfaces in a 0.13-μm Cu-Interconnection/Low-k CMOS Technology

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ABSTRACT

Level shifters for 1.0-V to 3.3-V high-speed interfaces are proposed. Level-up shifter uses zero-Vt 3.3-V NMOSs as voltage clamps to protect 1.0-V NMOS switches from high voltage stress across the gate oxide. Level-down shifter uses 3.3-V NMOSs as both pull-up and pull-down devices with supply voltage of 1.0-V and gate voltage swing from 0-V to 3.3-V. The zero-Vt NMOS is a standard MOSFET device in a 0.13-μm CMOS process without adding extra mask or process step to realize it. Level-up transition from 0.9-V to 3.6-V takes only 1 ns in time, and the level-down transition has no minimum core voltage limitation. These circuits do not consume static DC power, therefore they are very suitable for low-power and high-speed interfaces in the deep sub-quarter-micron CMOS technologies.

INTRODUCTION

As demand on integrating more functions onto a chip increases, very deep sub-quarter-micron process becomes more attractive. While process shrinks, the voltage of the core logic must shrink to avoid hot carriers and gate-oxide breakdown. At the same time, 3.3-V output level is still the main stream of I/O interfaces. Level shifters are the bridges that transform signals from low core voltage (VDD) to high I/O voltage (VDDQ), and vice versa (see Fig. 1). However, conventional level shifters (Fig. 2) do not work any more as the core voltage decreases to 1-V. This is due to VDD scales too rapidly, while the threshold voltages (Vt) of 3.3-V MOSFETs stay at the same value that 3.3-V NMOSs in level-up shifter and 3.3-V PMOSs in level-down shifter cannot turn on.

There are two approaches to reduce the gap between VDD and Vt of 3.3-V NMOSs for level-up shifters. First is to use core NMOSs instead of 3.3-V NMOSs to get a lower threshold voltage. Second is to pump up VDD to 2VDD, to get a higher voltage to turn on 3.3-V NMOSs.

An I/O using 2-V MOSFETs to drive 3.3-V output level has been reported [1]. Pull-up part of post-driver and the related level shifter are simplified as shown in Fig. 3. A cascode configuration of PMOMs is used for post-driver to avoid high voltage stress. VBIAS limits the gate voltage of PT between 1.6-V and 3.3-V to protect PT2. Though this circuit doesn't have the drawback in conventional level-up shifter because Vt of 2-V NMOSs is much lower than Vt of 3.3-V NMOSs, it takes tens of μAmps DC current to generate VBIAS, and need extra circuits, such as previously reported design [2], to turn-off DC bias voltage in the sleep mode.

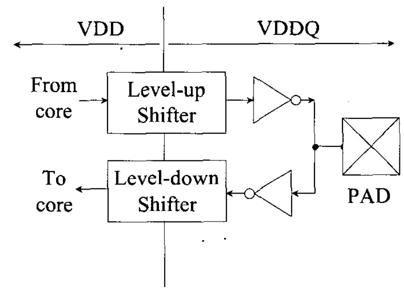
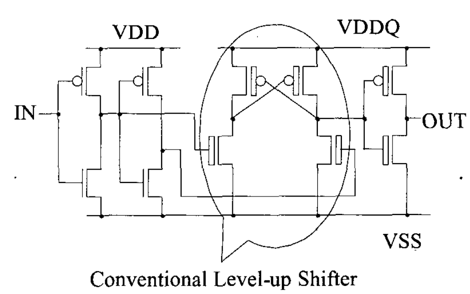
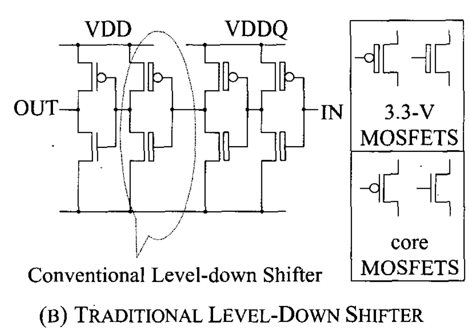


FIGURE 1. LEVEL SHIFTERS USED IN AN I/O BUFFER.



(A) TRADITIONAL LEVEL-UP SHIFTER



(B) TRADITIONAL LEVEL-DOWN SHIFTER

FIGURE 2. THE TRADITIONAL LEVEL SHIFTERS, (A) THE LEVEL-UP SHIFTER, AND (B) THE LEVEL-DOWN SHIFTER.

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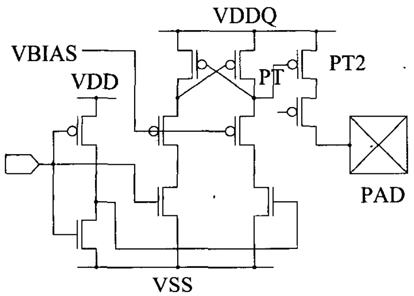


FIGURE 3. OUTPUT BUFFER AND LEVEL-UP SHIFTER FOR PULL-UP USING 2-V MOSFETS TO DRIVE 3.3-V.

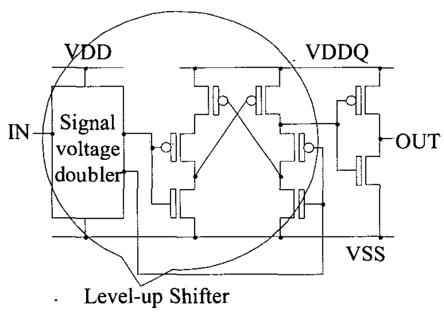


FIGURE 4. LEVEL-UP SHIFTER USING PUMP-HOPPING.

Recently, a pump-hopping level-up shifter has been introduced [3]. It includes a signal voltage doubler to pump up a differential pair to 2VDD, and a conventional level-up shifter to transform these differential signals to a single-ended output (Figure 4). This approach doubles the effective VDD and thus reduces the gap between VDD and Vt of 3.3-V NMOSs in the conventional level-up shifters. However, it takes 5-ns in the worst PVT condition that can be too slow for hundreds MHz applications. On the other hand, if input doesn't toggle for a long time, pumped charges will leak because of the junction reversed-bias leakage. That will cause the effective VDD back to VDD, not 2VDD at the beginning, and make this circuit susceptible to noises [4].

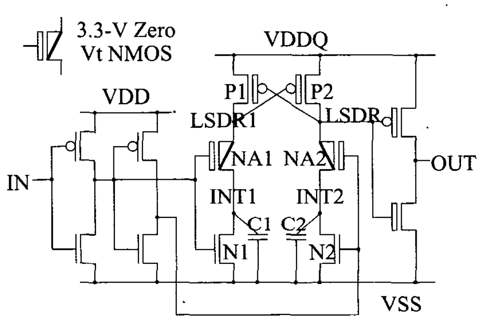
We have developed a level-up shifter using zero-Vt 3.3-V NMOSs to protect 1.0-V NMOS switches from high voltage stress [Fig. 5(a)]. Another version to provide further protection to 1.0-V NMOS switches is shown in Fig. 6. 3.3-V zero-Vt NMOS is the key element which is a standard MOSFET in a 0.13-μm dual-gate oxide CMOS process [5]. Therefore, no extra process is needed. Level-down shifter uses 3.3-V NMOSs as both pull-up and pull-down devices with supply voltage of 1.0-V and gate voltage swing from 0-V to 3.3-V [Fig. 5(b)]. Level-up shifter achieves a short propagation delay of 1-ns, which is five times faster than the previous reported [3]. Level-down shifter without minimum VDD limitation is also described.

At the end of this work, we describe the guidelines to enable stable operations of the core logic where I/O noises approach the core voltage, VDD. It is important to note that, when I/Os operate above 100MHz with 3.3-V swings, simultaneously switching noises (SSN), as high as 0.8-V, will seriously disturb the logic operations in core with supply voltage of only 1.0-V if no proper protections are implemented.

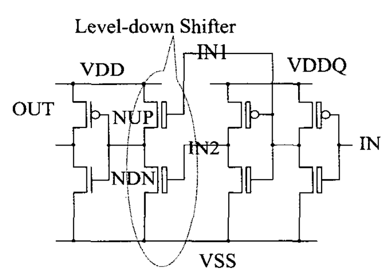
NEW LEVEL-UP SHIFTER

Figure 5 (a) is the level-up shifter. Zero-Vt 3.3-V NMOSs NA1 and NA2 are used to protect 1.0-V NMOSs N1 and N2 from high voltage stress. The gate of NA1 (NA2) is not fixed to VDD because INT1 (INT2) will approach VDD+ G V where the gate voltage of NA1 (NA2) is at VDD and N1 (N2) is off that causes gate-oxide breakdown of N1 (N2). G V is the balanced voltage when the subthreshold leakage of NA1 (NA2) is equal to the junction reversed-bias leakages of NA1 plus N1 (NA2 plus N2). Turning off NA1 (NA2) when P1 (P2) pulls up can isolate the parasitic capacitance C1 (C2) from the node LSDR1 (LSDR) and thus increase speed.

It is difficult to estimate the voltages at INT1 and INT2 based on Spice model because the subthreshold leakage model of NA1 and NA2 is usually not accurate for the logic process. Therefore, N3 and N4 can be added to provide further protection to N1 and N2 as shown in Fig. 6.



(A) NEW LEVEL-UP SHIFTER



(B) NEW LEVEL-DOWN SHIFTER

FIGURE 5. THE NEW PROPOSED LEVEL SHIFTERS, (A) THE LEVEL-UP SHIFTER, AND (B) THE LEVEL-DOWN SHIFTER.

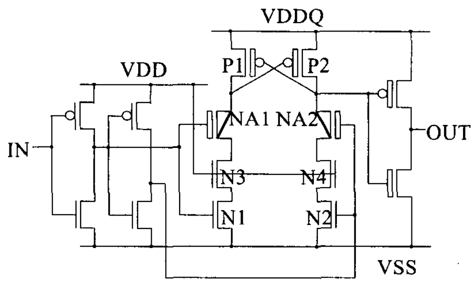


FIGURE 6. NEW LEVEL-UP SHIFTER TO PROVIDE MORE PROTECTION TO 1.0-V NMOS SWITCHES.

Transfer characteristics of proposed and conventional level-up shifters are simulated based on Figure 7 and the results are illustrated in Figure 8. One input pin of each level-up shifter is fixed to VDD and another input pin, IN, is swept from 0-V to VDD. If the level-up shifter can toggle, V(OUT) needs, at least, a voltage drop of Vt below VDDQ to turn on PMOSs at the opposite side. The hardest toggling condition is found at SF process, 0° C, VDDQ = 3.6-V, and VDD = 0.9-V. All MOSFET sizes are listed in Table 1. As shown in Figure 8, even with pull-down NMOSs to pull-up PMOSs ratio as high as 60:1, conventional level-up shifter cannot toggle because V(OUT) only drops to (VDDQ - 0.4-V) as V(IN) = VDD.

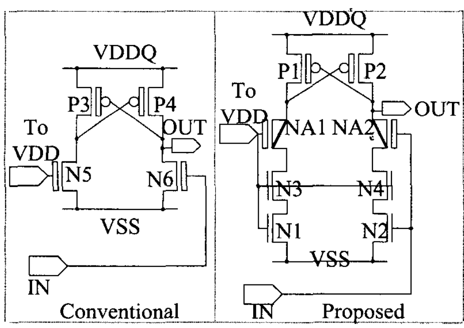


FIGURE 7. CIRCUIT CONFIGURATIONS TO GET TRANSFER CHARACTERISTICS OF LEVEL-UP SHIFTERS.

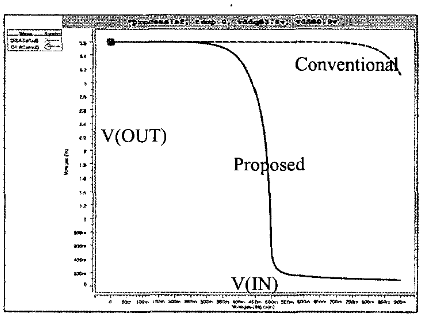


FIGURE 8. TRANSFER CHARACTERISTICS OF PROPOSED AND CONVENTIONAL LEVEL-UP SHIFTERS.

TABLE 1. MOSFET SIZES IN FIGURE 7.

P1	1/0.3	P3	1/0.3
P2	1/0.3	P4	1/0.3
NA1	20/1.2	N5	60/0.35
NA2	20/1.2	N6	60/0.35
N1	15/0.13		
N2	15/0.13		
N3	15/0.13	Unit: μm	
N4	15/0.13		

Fig. 9 shows the simulated waveforms in typical PVT condition (Typical process, 25°C, VDDQ = 3.3-V, and VDD = 1.0-V) using the level-up shifter circuitry shown in Figure 6. Simulations for other PVT conditions show that the maximum propagation delay from IN to OUT is 1-ns at FS process, 125°C, VDDQ = 3.0-V, and VDD = 0.9-V.

Optimized sizes of NA1 and NA2 for both speed and noise margin are 10-μm /1.2-μm, half of the current sizes. The reason to chose NA1 and NA2 twice of the optimized size is to reserve guard band before real silicon out. Figure 10 shows if NA1 and NA2 are taken as 10-μm /1.2-μm or 15-μm /1.2-μm, other than 20-μm /1.2-μm, the propagation delays will reduce to 0.75-ns and 0.9-ns, respectively, which is 25% and 10% faster.

Because NMOS switches are composed of core devices, the Vt of core devices will shrink proportionally to supply voltage, VDD. Therefore, by adjusting P1 and P2, this level-up shifter can operate even in sub 1-V process.

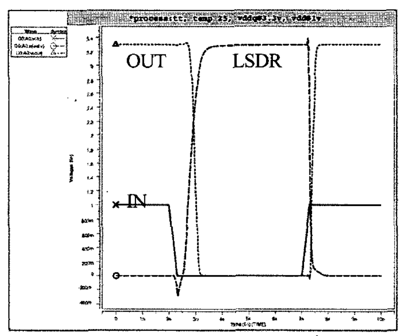


FIGURE 9. SIMULATED WAVEFORMS OF THE PROPOSED LEVEL-UP SHIFTER.

NEW LEVEL-DOWN SHIFTER

Figure 5 (b) is the level-down shifter. IN1 and IN2 are 3.3-V signals, and VDD is at 1-V that makes pull-up and pull-down devices, NUP and NDN, to have large gate-to-source voltages and thus low resistance. Because NUP and NDN always work in linear region, this circuit can work without any minimum limitation of the core voltage.

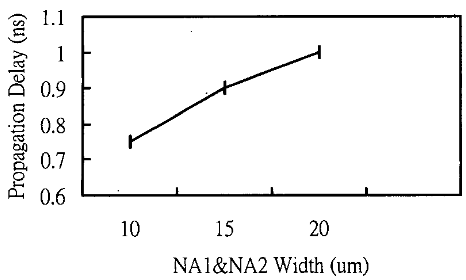


FIGURE 10. DIFFERENT SIZES OF NA1& NA2 VERSES PROPAGATION DELAYS.

NUP and NDN are optimized with sizes 3-µm /0.35-µm and 3-µm /0.35-µm, respectively. Conventional level-down shifter in Figure 2 has pull-up PMOS size of 30-µm /0.3-µm and pull-down NMOS size of 3-µm /0.35-µm. The worst PVT condition for the conventional one is at SS process, 0°C, and VDD = 0.9-V; VDDQ is not a key factor here. This is because (|Vgs| - |Vt|) of pull-up 3.3-V PMOS dominates the propagation delays. |Vt| increases at low temperature and |Vgs| decreases as VDD goes down to 0.9-V. Simulated waveforms of the worst PVT condition are shown in Figure 11. The conventional one has a propagation delay of 2.5-ns. Meanwhile, the proposed one has a propagation delay of 0.5-ns, which is five times faster.

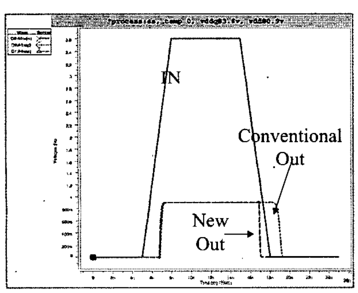


FIGURE 11. SIMULATED WAVEFORMS OF LEVEL-DOWN SHIFTER.

NOISE CONSIDERATIONS

As I/O frequency above 100MHz and output swing as high as 3.3-V, simultaneously switching noises (SSN) induced by current spike can be as high as 0.8-V which is almost the same amplitude as VDD of 1-V. Therefore, we have the following guidelines to help stable operations of the pre-driver and the core logic:

a) All NMOSs in Figure 5 (a) use the same ground, VSS, and layout closely;

b) All NMOSs in Figure 5 (b) use the same ground, VSS, and layout closely;

c) Use double guard rings to isolate I/O noises from the pre-driver and the core (Fig 12).

d) Put decoupling capacitors between VDD and VSS; Decoupling capacitors can be either PMOSs or NMOSs or other active or passive devices.

e) Put as many pick-ups as possible in the core.

Decoupling capacitors are normally used to share the noises at VDD and VSS to a half. Here they are used to make VDD and VSS to follow each other that keeps the voltage difference between VDD and VSS to a constant. Numerous pick-ups are used to help the substrate to follow the VSS fluctuations.

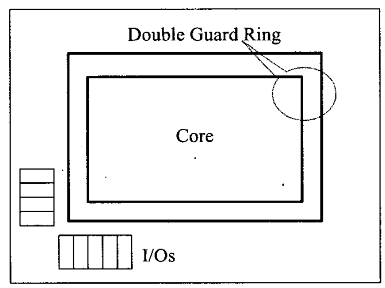


FIGURE 12. DOUBLE GUARD RING TO REDUCE I/O NOISES TO CORE.

CONCLUSION

Level shifters for 1.0-V to 3.3-V interfaces are developed in a 0.13-µm CMOS process. Level-up shifter uses zero-Vt 3.3-V NMOSs to protect 1.0-V NMOS switches and level-down shifter uses 3.3-V NMOSs as both pull-up and pull-down devices. No extra process step, no DC power and high-speed make these level shifters suitable for low power and high-speed applications. These techniques work even at VDD below 1.0-V in the future.

ACKNOWLEDGEMENTS

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