New Frequency-Locked Loop Based on CMOS Frequency-to-Voltage Converter: Design and Implementation

Abdelouahab Djemouai, Mohamad A. Sawan, *Senior Member, IEEE*, and Mustapha Slamani

***Abstract*—In this paper, we describe the architecture of a new CMOS fully integrated frequency-locked loop (FLL). The proposed FLL contains a frequency-to-voltage converter (FVC), an operational amplifier (opamp) and a differential voltage-controlled oscillator (VCO). The operation of the proposed circuit is based on frequency comparison of a reference and feedback signals. The architecture of the FVC is built upon capacitors charge redistribution principle, whereas the architecture of the VCO is based on differential delay cells in order to minimize the effect of the power supply and the substrate noise. Simulation carried out with Hspice using the CMOS 0.35-μm process shows that the FLL is very fast and operates over a wide frequency range. Two versions of the FLL are reported; the basic architecture could show a static offset due to the two employed FVCs. To alleviate this effect, a second version is proposed to completely eliminate the offset. The area of the proposed FLL is very small, and the design could be easily integrated in the same die together with other analog, digital and mixed-signal blocks. A functional test of five samples of a first version of this FLL proved that the proposed FLL works as expected from simulation results. Examples of the application of the proposed FLL are a high-precision VCO and a frequency synthesizer with true-fractional multiplication and division that does not require binary frequency dividers.**

***Index Terms*—Differential-delay cell, frequency-locked loop, frequency-to-voltage converter, phase-locked loop, voltage-controlled oscillator.**

I. Introduction

A PHASE-LOCKED loop (PLL) circuit is an interesting electronic building block widely used in many integrated applications. It is generally used in systems involving automatic control of frequency or phase, such as communications, frequency synthesis, radar, telemetry, and instrumentation systems. The PLL circuit generates an output signal that tracks an input reference signal. The output signal is synchronized with the input reference signal in frequency as well as in phase. Typically, a PLL is built around a phase detector or phase frequency detector (PFD), a charge pump, a low-pass filter, and a voltage-controlled oscillator (VCO) or current-controlled oscillator [1]. The PLL may also include frequency dividers and mixers when used in synthesizing frequency applications [2], [3]. The low-pass filter is required to ensure the stability and to determine the bandwidth of the PLL by filtering the PFD output signal. Usually, the low-pass filter is not integrated but implemented externally with discrete components in order to minimize the area of the integrated PLL. To overcome these design constraints and to allow the circuit to be fully integrated with an acceptable die area, we propose, in the present paper, a new frequency-locked loop (FLL) similar to a PLL in the way that it generates an output signal which tracks an input reference signal [4], [5]. However, in this case, the output signal is synchronized only in frequency with the input signal and not in phase, therefore, the locking time of this FLL would be very short. The proposed FLL is based on a new architecture that does not require the use of the phase detector, the charge pump nor the low-pass filter. The FLL principle operation is based on frequency comparison instead of phase comparison and where frequency comparison is completed by combining two frequency-to-voltage converters (FVCs) and an operational amplifier (opamp). Since the FLL is to be totally integrated with other analog and digital blocks in the same die, the FVCs are used to perform the frequency comparison. They should not be complex in order to keep the total area of the FLL short. In this direction, we propose a simple and fast FVC that requires a small integrated area [6]. The architecture of this FVC is built upon the charge redistribution principle based on switching capacitors, and requires control signals that are derived from its input signal.

The remainder of this paper covers the description and the operation of the proposed FLL and its different building blocks in Section II. In Sections III and IV, we outline the design steps of the FLL and the simulation and measurement results. In Section V, a second version of an offset-free FLL is discussed. This will be followed by Section VI, where we describe several applications of the FLL. Finally, we conclude in Section VII.

II. New Functions and Techniques

The proposed FLL is mainly a negative feedback circuit and is composed of two FVCs, a VCO, an opamp, and two frequency dividers per M and per N (Fig. 1). The feedback loop is composed of the divider per M, the FVC *FVC2*, the opamp and the VCO. The dividers per M and N are optional, but their use can improve the performance of the FLL as will be shown later. The

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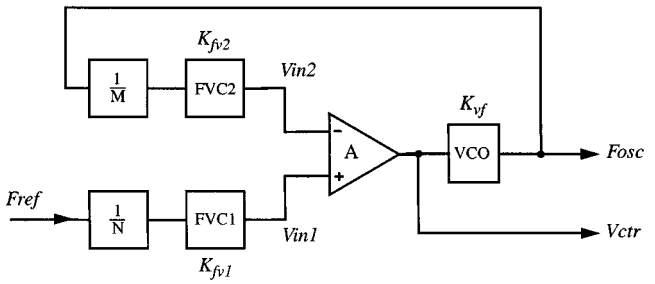

Fig. 1. Block diagram of the FLL circuit.

operation of the circuit is described as follows. First, the frequency of the input reference signal $(F_{\rm ref})$ is divided by N and converted to a voltage $(V_{\rm in1})$ by the *FVC1*. In the same way, the VCO oscillating frequency $(F_{\rm osc})$ is divided by M and converted to a voltage $(V_{\rm in2})$ by the *FVC2*. The difference between $V_{\rm in1}$ and $V_{\rm in2}$ is then amplified by the high-gain opamp and the resulting output voltage $(V_{\rm ctr})$ is employed to control the output frequency of the VCO. Since $V_{\rm in1}$ and $V_{\rm in2}$ correspond to $F_{\rm ref}$ and $F_{\rm osc}$ respectively, the *FVC1* and *FVC2* together with the opamp act as an analog frequency comparator. Depending on the voltage difference between $V_{\rm in1}$ and $V_{\rm in2}$, the opamp output voltage $V_{\rm ctr}$ will increase or decrease the VCO oscillating frequency $F_{\rm osc}$ until the voltage $V_{\rm in2}$ becomes equal to the voltage $V_{\rm in1}$. At the time when $V_{\rm in2}$ reaches $V_{\rm in1}$, the output voltage $V_{\rm ctr}$ ceases to vary and keeps the VCO oscillating at a constant frequency. Of course, as in any negative feedback system, the stability of the proposed design is carefully realized by the proper compensation of the opamp feedback loop in order for the design to work properly.

From Fig. 1, the opamp output voltage which represents the control voltage $(V_{\rm ctr})$ of the VCO can be expressed by

$$V_{\rm ctr} = \frac{A}{1 + K \cdot A} \cdot V_{\rm in1} \tag{1}$$

with

$$K = \frac{1}{M} \cdot K_{vf} \cdot K_{fv2} \tag{2}$$

where A, K_{vf}, and K_{fv2} are the gains of the opamp, the VCO, and the *FVC2*, respectively.

If the dc gain A of the opamp is very high, (1) can be simplified to lead to

$$V_{\rm ctr} = \frac{1}{K} \cdot V_{\rm in1} = \frac{M}{K_{vf} \cdot K_{fv2}} \cdot V_{\rm in1}. \tag{3}$$

From (2) and (3), we can derive the expression of the VCO oscillating frequency $F_{\rm osc}$

$$F_{\rm osc} = K_{vf} \cdot V_{\rm ctr} = \frac{M}{K_{fv2}} \cdot V_{\rm in1} \tag{4}$$

with $V_{\rm in1}$ equal to

$$V_{\rm in1} = \frac{1}{N} \cdot K_{fv1} \cdot F_{\rm ref}. \tag{5}$$

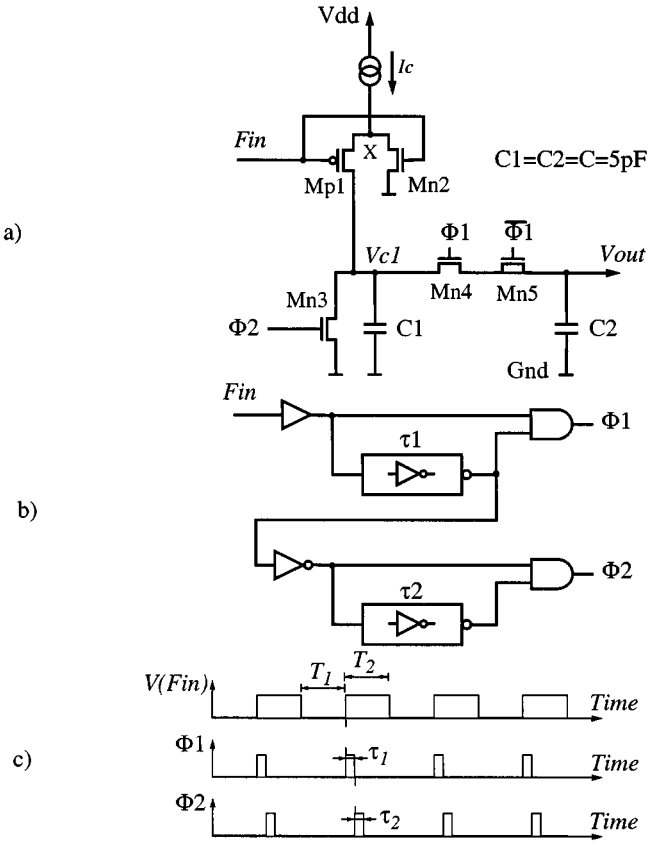

Fig. 2. FVC. (a) Basic architecture. (b) Logic controller block. (c) Control signals.

If $V_{\rm in1}$ of (4) is replaced by the expression given by (5), we obtain the expression of $F_{\rm osc}$ in term of the input reference frequency $F_{\rm ref}$, that is,

$$F_{\rm osc} = \frac{M}{N} \cdot \frac{K_{fv1}}{K_{fv2}} \cdot F_{\rm ref}. \tag{6}$$

If the converters *FVC1* and *FVC2* exhibit the same characteristics (if their components are matched: $K_{fv2} = K_{fv1}$), the VCO oscillating frequency $F_{\rm osc}$ will be related to the input reference frequency $F_{\rm ref}$ by

$$F_{\rm osc} = \frac{M}{N} \cdot F{\rm ref}. \tag{7}$$

In the case where M and N are equal, $F_{\rm osc}$ will be equal to $F_{\rm ref}$.

It is important to note that the FVC used here acts as an inverting amplifier (e.g., its output decreases when its input increases and vice versa), therefore, the right opamp connection should be carefully considered. It follows that, in the phase space, the action of the feedback branch composed by the VCO, the *FVC2* and the divider by M can be characterized by inverting amplifier. In these conditions, the transient behavior of the FLL feedback loop will be mainly predominated by the opamp characteristics. Therefore, the stability of the FLL circuit could be simply realized by Miller compensation of the opamp as verified by Hspice simulation. This is an interesting feature since in this case we do not use a low-pass filter as in the case of a conventional PLL.

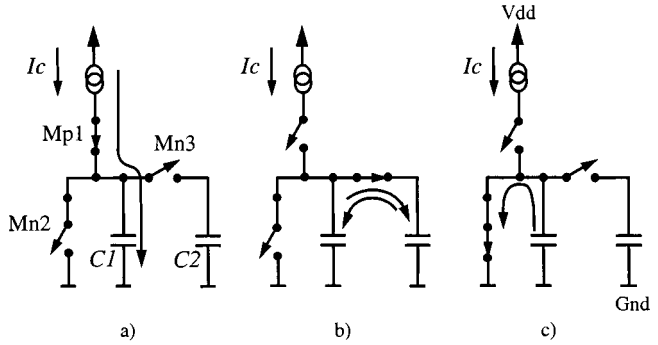

Fig. 3. Different operation steps of the proposed FVC. (a) Charging of capacitor $C1$. (b) Charge redistribution of $C1$ and $C2$. (c) Isolation of $C2$ and discharging of $C1$.

A. FVC

The FVC used in the FLL is presented in Fig. 2 [6]. It is composed of two equal capacitors $C1$ and $C2$ ($C1 = C2 = C$), a current source I_c, a set of transistors (*Mp1*, *Mn1*, *Mn2*, *Mn3*, and *Mn4*) that act as switches [Fig. 2(a)], and a logic controller block (LCB) which generates the signals $\Phi1$ and $\Phi2$ [Fig. 2(b) and (c)] that control transistors *Mn2*, *Mn3*, and *Mn4*. $\Phi1$ and $\Phi2$ have the same frequency $F_{\rm ref}$ as the input reference signal, but, with narrow pulsewidths that are equal, respectively, to the time required to discharge capacitor $C1$ and the time required to accomplish the charge redistribution operation between $C1$ and $C2$. The pulsewidth of $\Phi1$ could be evaluated using the time constant given by $(C1 + C2)$ times the ON resistor of transistor M4, whereas the pulsewidth of $\Phi2$ could be evaluated using the time constant given by $C1$ times the ON resistor of transistor *Mn2* [Fig. 2(a)]. In the presented design, the pulsewidths of $\Phi1$ and $\Phi2$ are approximately equal to 2 ns each.

Transistors *Mp1* and *Mn1* are controlled directly by the input signal, and are turned ON and OFF alternatively at the rate of the input signal frequency. The FVC uses, in a first step, the two signals ($\Phi1$ and $\Phi2$) together with the reference signal to charge the capacitor $C1$ by the constant current I_c during one-half period of the input waveform. Then, in a second step, the initial charge of $C2$ and the accumulated charge of $C1$ are equally redistributed in order to produce the output voltage that will be held by capacitor $C2$.

The detailed operation of this proposed FVC is presented in the following. During the half period $T1$ where the input signal $V(Fin)$ is at its low level, transistor *Mp1* is turned ON while *Mn1*, *Mn2*, and *Mn3* are OFF, therefore, capacitor $C1$ will be charged by the constant current Ic during the time $T1$ [Fig. 3(a)]. Transistor *Mn1* is included here to keep the voltage of the node X [Fig. 2(a)] at a low voltage level when the input signal is high, therefore when the input signal changes from the high level to the low level, capacitor $C1$ will begin charging from a very low voltage. This will eliminate the voltage error that could be introduced by the transient spikes that show up during the switching of transistor *Mp1* in the case where transistor *Mn1* is not used.

When the input signal switches to its high level, transistor *Mp1* is turned OFF and *Mn1* is turned ON, therefore, capacitor $C1$ ceases charging and is isolated from the rest of the circuit. Since accumulated charge of capacitor $C1$ is the charge integrated during the time $T1$ which is equal to half of the period of the input signal $(1/Fin)$, the total charge of $C1$ is then directly proportional to the half period of the input waveform. This charge should be then transferred to capacitor $C2$ to be stored as an indication of the input frequency which is accomplished in the following way: just after capacitor $C1$ is isolated from the rest of the circuit, signal $\Phi1$ goes to its high level for the short period τ_1 and turns ON transistor *Mn3*. Meanwhile, since *Mp1* and *Mn2* are OFF, the charge stored in capacitor $C1$ and the initial charge stored in capacitor $C2$ are then distributed equally between these two capacitors [Fig. 3(b)]. It is important to note that transistor *Mn4* with drain and source short connected acts as a dummy switch and its main purpose is to minimize the voltage errors associated with charge injection effect when the transistor *Mn3* is alternatively turned ON and OFF. Once the charge distribution of $C1$ and $C2$ is completed, transistor *Mn3* is turned OFF, therefore, capacitor $C2$ is isolated from the rest of the circuit and holds its charge safely during the second half period $T2$ of the input signal [Fig. 3(c)]. When the signal $\Phi1$ returns to zero, signal $\Phi2$ goes up for the short time period τ_2 and turns ON the transistor *Mn2* which discharges capacitor $C1$ [Fig. 3(c)].

If the input signal $V(Fin)$ to this circuit is a square waveform of a frequency Fin and with 50% of duty cycle, the FVC output voltage can be expressed in term of Fin by the following relation:

$$V_{\rm out} = \frac{I_{\rm c}}{C1}\left(\frac{T}{2}\right) = \frac{I_{\rm c}}{C}\left(\frac{1}{2F_{\rm in}}\right). \tag{8}$$

Equation (8) shows that the FVC output voltage is inversely proportional to the frequency Fin of the input waveform which could be understood as an inversion in the phase plan.

Referring to (8), the minimum and the maximum limits of the frequency operating range of the FVC can be fixed by the charging current I_c, the value of capacitor $C1$, and the minimum and the maximum values of the output voltage. These limits are given by

$$F_{\rm min} = \frac{I_{\rm c}}{2C}\left(\frac{1}{V_{\rm max}}\right) \tag{9}$$

$$F_{\rm max} = \frac{I_{\rm c}}{2{\rm C}}\left(\frac{1}{V_{\rm min}}\right). \tag{10}$$

Since $V_{\rm max}$ and $V_{\rm min}$ of the output voltage are limited by the negative and positive power supplies, $F_{\rm min}$ and $F_{\rm max}$ of the operating frequency range of this FVC could be fixed by the proper choice of I_c and C.

In order to determine the time response Tr of this FVC, we need to find the expression that relates the electrical charges of $C1$ and $C2$, which is similar to the expression that relates the output voltage $V_{\rm out}$ and the voltage Vc_1 of capacitor $C1$. If the frequency of the input signal is constant and capacitors $C1$ and $C2$ are equal, then the output voltage $V_{\rm out}$ will progress in time in the following way. After the first period, $V_{\rm out}$ is equal to the half of Vc_1 (this is the result of the charge redistribution between $C1$ and $C2$). Similarly, after the second period, $V_{\rm out}$ will be increased by the quarter of Vc_1 (the half of the difference between Vc_1 and $V_{\rm out}$), and after the third period $V_{\rm out}$ will be

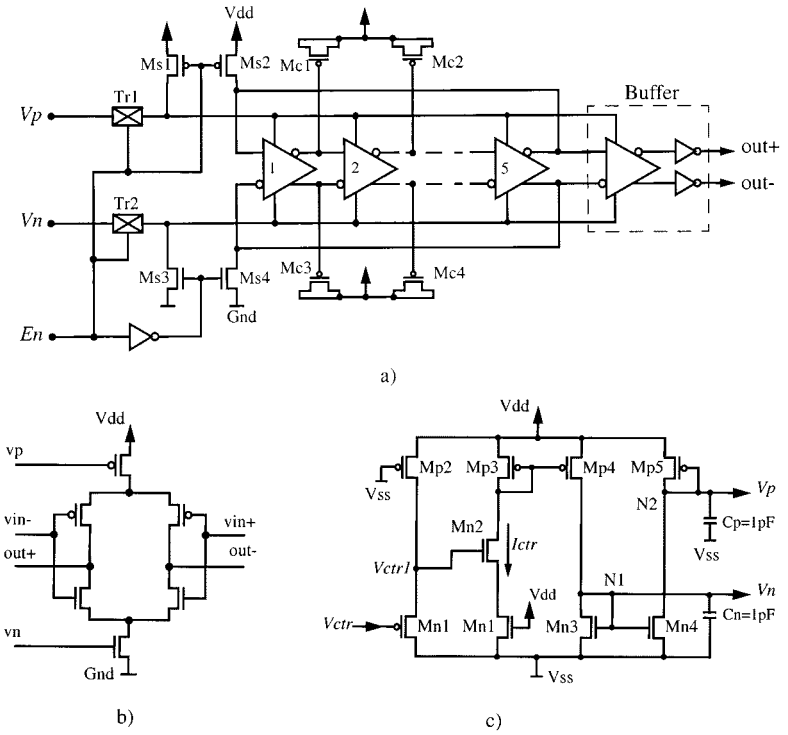

Fig. 4. Schematic of: (a) the VCO of the FLL of Fig. 1; (b) its basic differential cell; and (c) its bias circuit.

increased by the eighth of Vc_1 and so on. This progression can be expressed by the following equation:

$$V_{\text{out}} = \frac{1}{2^1}Vc_1 + \frac{1}{2^2}Vc_1 + \frac{1}{2^3}Vc_1 + \cdots + \frac{1}{2^N}Vc_1. \quad (11)$$

Here, N is an integer and is equal to the total number of cycles of the input signal corresponding to the time over which we would express the output voltage V_{out}. Equation (11) can be simplified and arranged to lead to

$$V_{\text{out}} = Vc_1\left(1 - \frac{1}{2^N}\right). \quad (12)$$

Using (12), the absolute error ΔV_{out} corresponding to the difference between Vc_1 and V_{out} can be expressed by

$$\Delta V_{\text{out}} = |V_{\text{out}} - Vc_1| = \frac{1}{2^N}Vc_1. \quad (13)$$

By examining the expression given by (13), it is obvious that to minimize the error ΔV_{out}, N should be very large, but, in fact, a small value of N leads to acceptable results. As an example, for $N = 7$, ΔV_{out} is less then 1% and for $N = 8$, ΔV_{out} is approximately equal to 0.4%. If we consider that $\Delta V_{\text{out}} = 0.4\%$ corresponding to $N = 8$ is acceptable, then the time response of the proposed converter could be approximated by

$$Tr \cong 8T \quad (14)$$

where $(1/T)$ is the frequency of the input signal.

Finally, in order for this circuit to operate properly, the maximum frequency $f_{\max}$ should be selected to respect the following relation:

$$F_{\max} \leq \frac{1}{2(\tau_1 + \tau_2)}. \quad (15)$$

If τ_1 and τ_2 are set, for example, to 2 ns each, then from (15), the maximum frequency limit of this FVC would be equal to 100 MHz. Here, τ_1 and τ_2 are determined respectively by the time required to discharge capacitor $C1$ and the time required to accomplish the charge redistribution operation between $C1$ and $C2$. One way to overcome this FVC maximum frequency limit and allow the circuit to operate at higher frequencies, is to insert a frequency divider at the input of the FVC. As an example, a division by 2 will push the maximum frequency limit to 200 MHz, a division by 4 will push it to 400 MHz, and so on. Following this, the presence of the dividers by M and by N in the FLL circuit of Fig. 1 is justified.

B. VCO

The schematic of the proposed VCO is presented in Fig. 4(a). It is a differential ring oscillator composed of five delay cells [Fig. 4(b)], an output buffer, and an enable circuit. The enable circuit is composed of two transmission gates *Tr1* and *Tr2*, four transistors *Ms1–Ms4*, and an inverter *I1*. This circuit is useful for testing purposes and for saving power when the FLL is not used (e.g., in the idle mode). The output buffer is necessary to isolate the VCO from the other sub-blocks that require the VCO outputs and to provide enough power to drive high-capacitive loads without disturbing the VCO operation. Since this buffer changes the load capacitance of the last delay cell of the VCO, the delay of this cell would be different from the other delay

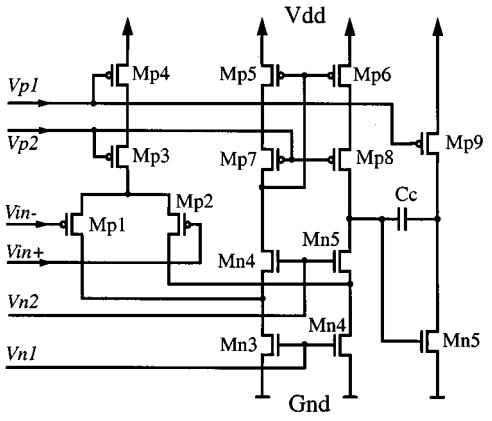

Fig. 5. Folded cascode operational amplifier used in the design of the FLL.

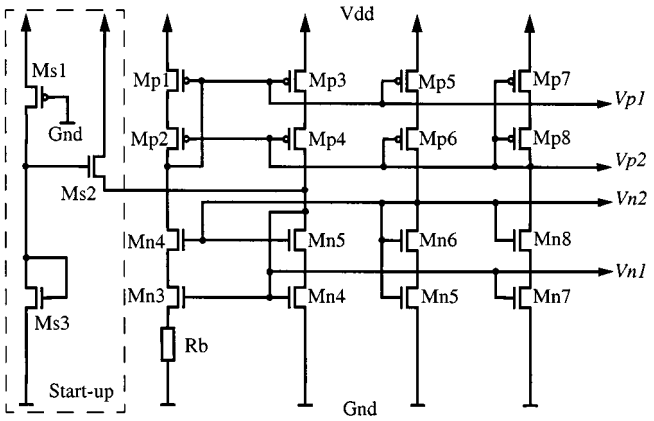

Fig. 6. Self-biasing voltage reference circuit used to generate the bias voltages of the folded cascode opamp of Fig. 5.

cells of the VCO which is not acceptable in some applications. To reduce this effect, all the load capacitors of all the delay cells of the VCO are equilibrated by inserting the capacitors formed by the gates of the transistors *Mc1–Mcn* [Fig. 4(a)]. Here, each transistor has the same size as the input transistors of the output buffer and with the drain and source tied together to the power supply.

The schematic of the basic differential delay cell of this VCO is presented in Fig. 4(b). It is composed of two starved cross-coupled CMOS inverters that are in the opposite states permanently and share the same source and sink currents that are used to control the delay of this stage. Since the capacitances of the output nodes of each delay cell are charged by equal currents (the sink and the source currents), the VCO based on this delay cell produces balanced output waveforms. Moreover, this architecture shows no static power loss, and the only losses are those attributed to the dynamic power consumption caused by the charge and the discharge of the parasitic capacitances associated with the output nodes. The sink and the source currents of each delay cell of the VCO are determined by the bias voltages $V_{\rm p}$ and $V_{\rm n}$ which are generated by the circuit of Fig. 4(c).

The operation of this circuit is described by the following: transistors *Mp1* and *Mp2* form a voltage follower with the *Mp2* acting as a load that limits the current flowing through these two transistors. The aim of this follower is to shift up the input voltage $(V_{\rm ctr})$ by a dc voltage equal to $V_{\rm tp}$ (the threshold of the transistor *Mp1*). This is necessary to allow the circuit to operate over a wide range of the control voltage $(V_{\rm ctr})$ especially when this voltage is very low. Transistors *Mn1* and *Mn2* operate in their linear region and act as resistors with the resistor of *Mn2* being controlled by the voltage $V_{\rm ctr1}$. Therefore, the current $(V_{\rm ctr})$ developed in this branch is determined or controlled by the voltage $V_{\rm ctr1}$ which is simply equal to the input voltage $I_{\rm ctr}$ plus $V_{\rm tp}$. The same current is mirrored and used to control the delay of the differential inverter stage.

In order to achieve this task, we need to generate the desired bias voltages $V_{\rm n}$ and $V_{\rm p}$ of this inverter. These bias voltages are simply generated by the current mirrors composed of the transistors *Mp3–Mp4* and *Mn3–Mn4*. To improve the high-frequency response of this biasing circuit, we added two capacitors ($C_{\rm n}$ and $C_{\rm p}$) of 1 pF each that stabilize the bias voltages $V_{\rm n}$ and $V_{\rm p}$.These two capacitors together with the impedances seen at

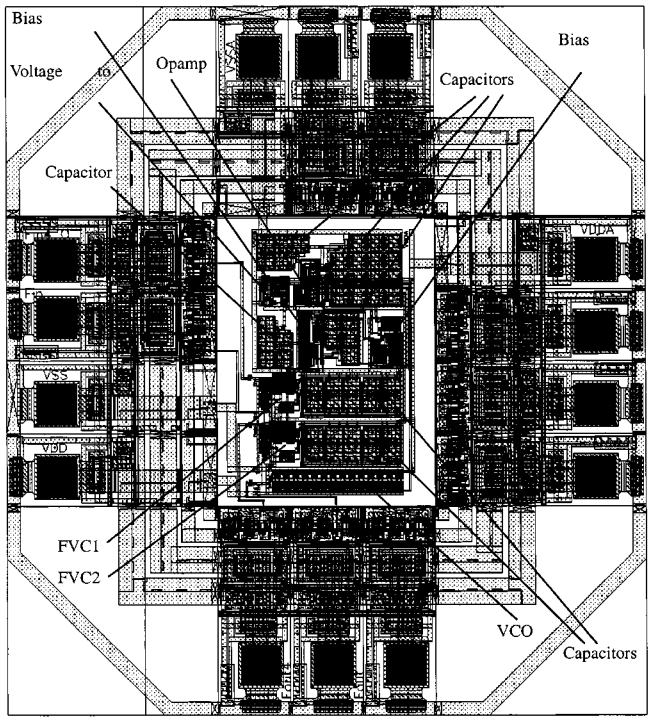

Fig. 7. Complete layout of the proposed FLL.

the nodes $N1$ and $N2$ act as low-pass filters, therefore, they eliminate or filter out the high-frequency transient components that could be coupled from the VCO.

C. Opamp

The opamp used in our application is reported in Fig. 5. It is a folded cascode CMOS opamp with an input stage made of p-channel MOS transistors. Its biasing current is fixed by the bias voltages $V_{\rm n1}$, $V_{\rm n2}$, $V_{\rm p1}$, and $V_{\rm p2}$. These bias voltages are generated by the bias circuit of Fig. 6. This opamp has a wide common mode range and presents the following characteristics: a dc gain of 109 dB, a phase margin of 90°, and a bandwidth of 2.2 MHz. The bias circuit of Fig. 6 is a self-biasing voltage reference constructed around high-swing cascode current mirror circuits and a resistor (*Rb*) that fixes the current source (15.3 μA) of the current mirrors. For this circuit to operate properly,

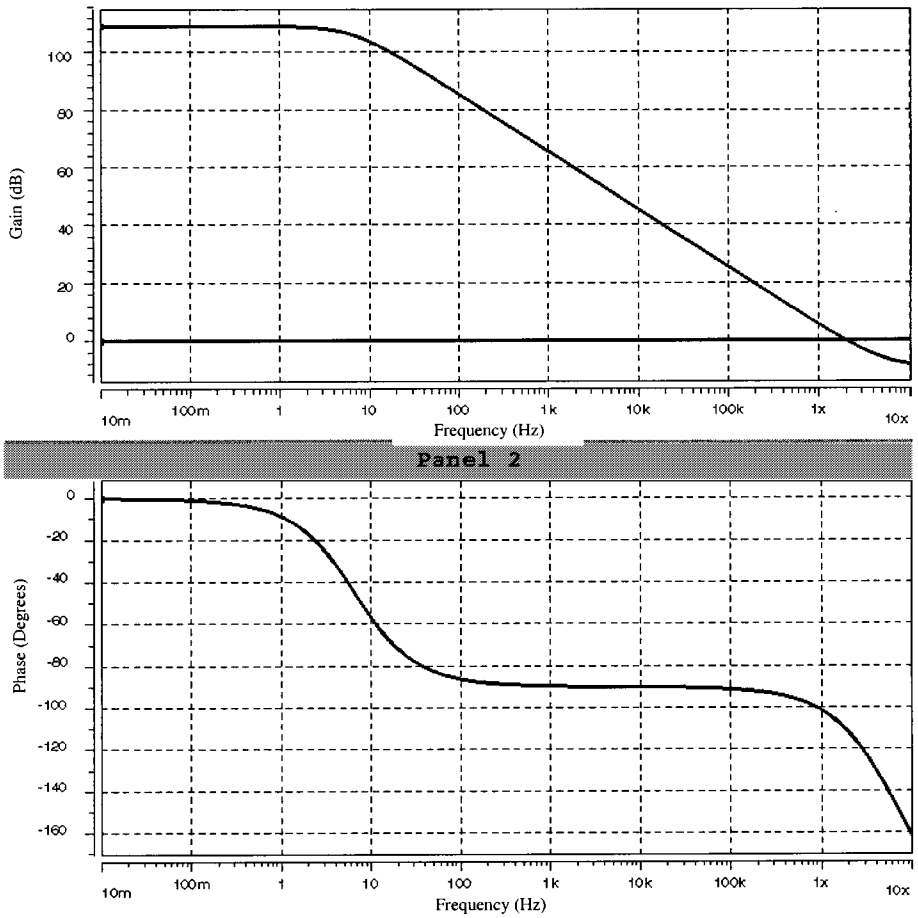

Fig. 8. Open-loop ac characteristics of the folded cascode opamp of Fig. 5.

it is important that the width of transistor *M3* should be K times greater than the width of the transistor *M4* where K is an integer and, in our application, is fixed to 4. Since this kind of bias circuit presents two stable operating points, one at the desired current (15.3 μA) and one at a current equal to zero, it requires a startup circuit that forces the circuit to move to the right operating point once it is powered up. This startup circuit is composed of the transistors *Ms1*, *Ms2*, and *Ms3* (Fig. 6).

III. Circuit Implementation of the FLL

To simulate the FLL, we fixed the capacitors $C1$ and $C2$ of the FVCs to 5 pF each and the charging current I_c is fixed to 430 μA [Fig. 2(a)]. The two dividers per M and N, where $M = N = 4$, are based on negative edge triggered D flip-flops and are dedicated to increase the maximum frequency limit of the FVC. Moreover, they also serve to transform the input and the output frequencies to balanced signals with 50% of duty cycle. The operating frequency range of the VCO scales from 161 to 256 MHz.

The complete FLL was implemented using the 0.35-μm CMOS double polysilicon and three metal process, and its layout is presented in Fig. 7. The total active area of the circuit is equal to 0.22 mm^2 (= 361 μm $\times$ 593 μm). Since this FLL design includes digital and analog parts, its layout was realized with special attention to minimize the noise injection from the digital parts to the analog parts. For this reason, the power and ground lines of the analog and digital parts were separated in the layout of the FLL; these lines would be connected together outside the chip containing the die of the FLL [7]. Also, for the accuracy of the analog parts, multiple matched transistors are used for the input stage of the amplifier and for all the current mirror circuits. This will beneficially reduce the channel length modulation and the process variation effects.

IV. Simulation and Experimental Results

In this section, we present the Hspice simulation results of the FLL and its various blocks implemented in a 0.35-μm CMOS. Fig. 8 illustrates the open-loop ac characteristics of the opamp of Fig. 5 used in this application. The dc gain, the phase margin, and the unity gain bandwidth of this opamp are equal to 109 dB, 90° and 2.2 MHz, respectively. In Fig. 9, we depict the FVC control signals $\Phi 1$ and $\Phi 2$ and the output voltage corresponding to an input square waveform with a period of 12 ns. From these results and as described previously, it is clear that the FVC output voltage reaches its final value after 8 cycles of the input waveform.

Simulation results of the complete FLL show that the circuit is stable and very fast. To highlight the large transient behavior of the FLL and to test its tracking ability, the FLL was simulated with an input reference frequency F_{ref} that changes from 171 to 230 MHz. The results of this simulation are depicted in Fig. 10, where we present the variation of the different control

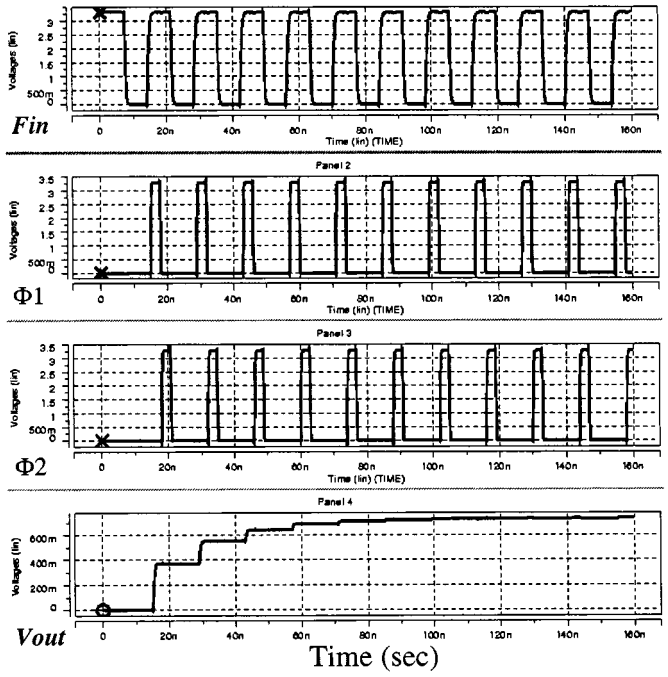

Fig. 9. Transient response of the FVC to a square-wave input.

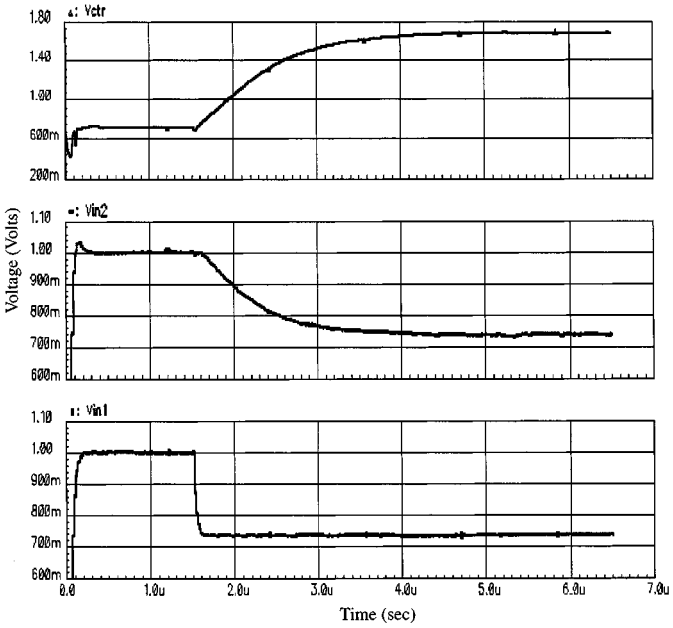

Fig. 10. Large transient response of the FLL.

voltages of the FLL. The frequency $F_{\rm ref}$ is equal to 171 MHz during the period of 0–1.5 μs and equal to 230 MHz in the period of 1.5–6.5 μs. The depicted voltages are the output of the *FVC1* $(V_{\rm in1})$ that corresponds to the reference frequency $F_{\rm ref}$, the output of the *FVC2* $(V_{\rm in2})$ that corresponds to the VCO oscillating frequency $F_{\rm osc}$, and the output of the opamp $(V_{\rm ctr})$ used to control the VCO frequency. These results prove the stability and the capacity of the FLL to correctly track the changes associated to the frequency of the input signal. From Fig. 10, the time required for the FLL to adjust the frequency of output signal to a change in the frequency of the input signal from 171 to 230 MHz is less than 2 μs. A functional test of five samples of a first version of this FLL shown in Fig. 7 proves that the proposed FLL operates correctly as expected. Experimental results of the tested chips show that the FLL has a frequency dynamic range (196–248 MHz) a little bit smaller than the frequency range obtained from Hspice simulation (161–256 MHz).

V. FLL Offset Cancellation

Since the proposed FLL uses two separate FVCs that could show some mismatches because of the bad tolerance of their integrated elements, the FLL performance will be deteriorated in such case. Indeed, any mismatch between the elements of both the FVCs will be directly reflected as a frequency offset in the FLL oscillating frequency. The major causes of this offset are mismatches between the charging currents of the FVCs, and the capacitors $C1$ of the *FVC1* and *FVC2*. Since the mismatch between integrated current sources could be kept very small by using wide-swing or cascoded current sources and current mirrors, the offset caused by the FVC charging currents is not too critical and it could be neglected. On the other hand, the offset caused by the mismatch of the FVCs capacitors is critical because the tolerance of integrated capacitors could be as high as 30%, therefore, this kind of mismatch could not be neglected.

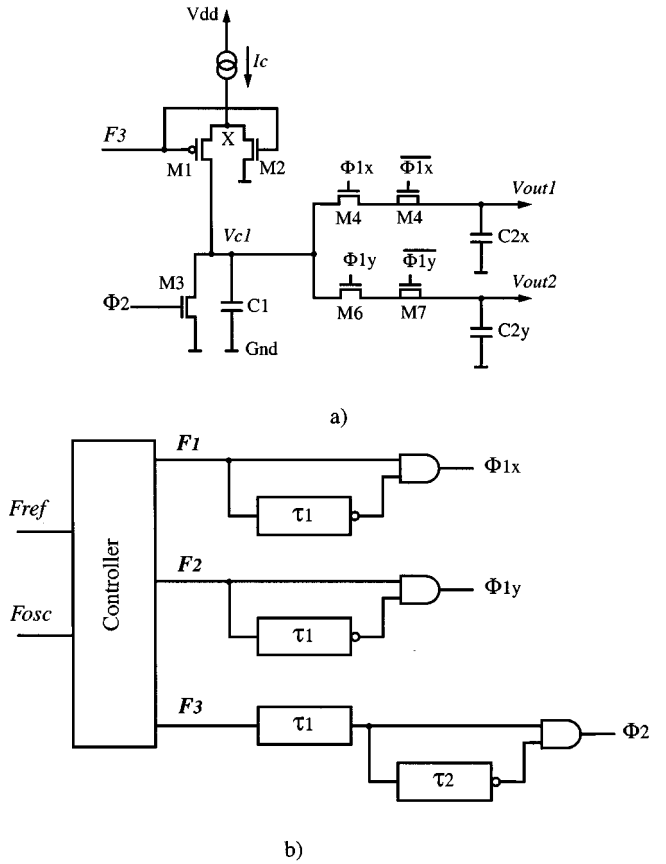

Fig. 11. Frequency-to-voltage converter with offset cancellation. (a) Basic architecture. (b) Circuit used to generate the control signals; the controller content is the object of Fig. 12.

Fortunately, it is possible to completely eliminate the offset resulted from any mismatch between the two FVCs by using the proposed circuit of Fig. 11(a). The new circuit is intended to replace the two FVCs used in the FLL of Fig. 1 and is controlled by

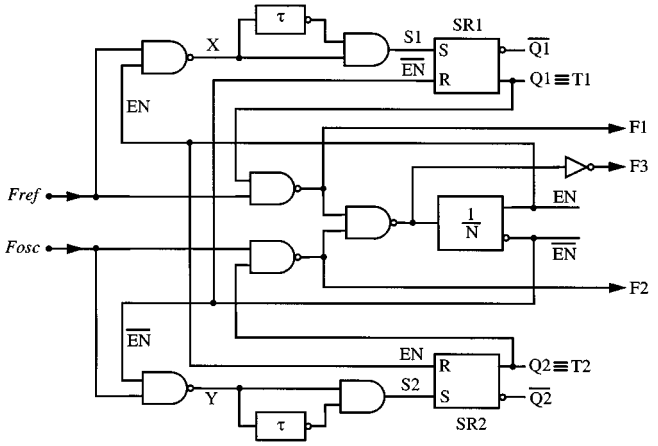

Fig. 12. Block diagram of the controller of the circuit of Fig. 11.

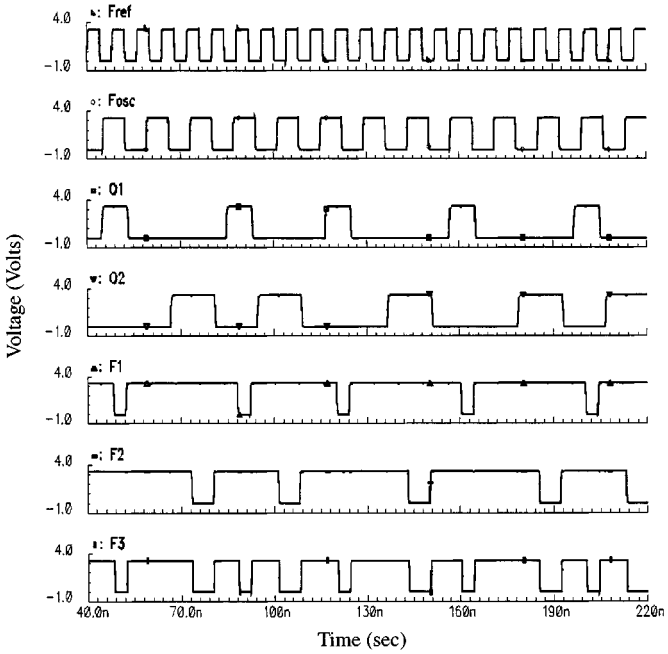

Fig. 13. Control signals of the circuit of Fig. 12 for the case where $F_{\rm ref}$ and $F_{\rm osc}$ are different.

the signals generated by the circuit of Fig. 11(b). In this configuration, both FVCs share the same charging current source and the same integrating capacitor $C1$, therefore, this circuit can be considered as offset free. Capacitors $C2x$ and $C2y$ serve only as storage elements and are used to hold the converted voltages corresponding to the reference frequency and oscillating frequencies of the FLL, therefore, their mismatch does not induce any offset.

The mismatch-free FVC circuit converts, alternatively, during one period of time $(T1)$ the reference frequency $F_{\rm ref}$ and during another period of time $(T2)$ the FLL oscillating frequency $F_{\rm osc}$. During the period of time $T1$ the holding capacitor $C2y$ is isolated and the circuit converts a fixed number of cycles of the reference frequency $F_{\rm ref}$ and stores the result in capacitor $C2x$. In the period of time $T2$ the holding capacitor $C2x$ is isolated and the circuit converts a number of cycles of the oscillating frequency $F_{\rm osc}$ and stores the result in capacitor $C2y$. Therefore, it is obvious that the two capacitors $C2x$ and $C2y$ are continually isolated from each other and store adequately the voltages resulting from the conversion of $F_{\rm ref}$ and $F_{\rm osc}$. The circuit that generates all the needed control signals (the controller) to properly operate this new FVC is shown in Fig. 12. It is an asynchronous circuit composed mainly of logic gates, two set/reset (SR) latches, a frequency divider $(1/N)$, and two delay lines ($\sim$1 ns each). The frequency divider is necessary to determine the two conversion periods $T1$ and $T2$. These two periods are not fixed, but track the FLL reference and oscillating frequencies variation in such a way that $T1$ contains $N/2$ periods of $F_{\rm ref}$ and $T2$ contains $N/2$ periods of $F_{\rm osc}$.

The operation of the controller is described here with the help of Figs. 12 and 13. When the divider output (EN) changes from 0 to 1, the latch *SR2* is reset and its output is forced to stay at 0 the whole time where the EN signal is equal to 1. Just after this moment, the circuit generates a pulse (the set signal $S1$) which is synchronized with the $F_{\rm ref}$ to set the output $Q1$ of the latch *SR1* to 1. During this period of time where both EN and $Q1$ are equal to 1, the input of the divider per N is equal to $F_{\rm ref}$ and the divider output (EN) will return to 0 after $N/2$ cycles of $F3$. In this case, the EN signal is equal to 1 during at least $N/2$ cycles of $F_{\rm ref}$. When the EN signal returns to 0, the latch *SR1* is reset $(Q1 = 0)$ and stays at this state as long as $EN = 0$. The pulsewidth of $Q1$ defines the conversion period $T1$ mentioned previously and is used to generate the signal $F1$ which contains exactly $N/2$ pulses of $F_{\rm ref}$. At the same time (when the EN signal returns to 0) and where the latch SR1 is reset, the circuit operation process is reversed and *SR2* latches *Q2* that defines the time conversion period $T2$. Since, in this case EN is equal to 0, the input of the divider by N is equal to $F_{\rm osc}$ and, consequently, its output will return to 1 after $N/2$ cycles of $F3$. In this case, the EN signal is equal to 0 during atleast $N/2$ cycles of $F_{\rm osc}$. It follows that the signal $F2$ generated during the conversion period $T2$ will contain exactly $N/2$ pulses of $F_{\rm osc}$. The switch control signals $\phi 1x$, $\phi 1y$, and $\phi 2$ of the FVC are then derived from the signals *F1*, *F2*, and *F3* where *F3* is generated from *F1* and *F2* using an AND gate. In Fig. 13, an Hspice simulation illustrates the control signals *F1*, *F2*, and *F3* generated by this controller when $F_{\rm ref}$ and $F_{\rm osc}$ are different.

VI. FLL Applications

One of the numerous interesting applications of the proposed design is a high-precision VCO. This can be achieved by removing the divider $1/N$ and the frequency-to-voltage *FVC1* (Fig. 1) and applying an input control voltage directly at the node $V_{\rm in1}$ instead of an input reference frequency. In this case, the VCO will be less sensitive to the power supply noise, since its oscillating frequency will be stabilized by the feedback action in such a way that $V_{\rm in2}$ is equal to $V_{\rm in1}$. Moreover, the transfer characteristics of this VCO are determined by the FVC *FVC2*, whereas its frequency dynamic range is fixed by that of the internal VCO. In these conditions, the output frequency can be determined using the transfer function of the *FVC2*.

Another interesting application of the FLL is its use as a continuous-frequency synthesizer by keeping the charging current $(I_{\rm cref})$ of the FVC that converts $F{\rm ref}$ constant and replacing

the charging current (I_{cosc}) of the FVC that converts F_{osc} by a programmable current source. To get a clear insight of this, we suppose that the two dividers of the FLL are equal $(M = N)$ and the capacitors $C1$ of the two FVCs are also equal. In such case, it follows from (6) and (8) that the FLL oscillating frequency F_{osc} can be expressed by

$$F_{\text{osc}} = \frac{I_{C\text{osc}}}{I_{C\text{ref}}} \cdot F_{\text{ref}}. \tag{16}$$

Therefore, it is now clear that by programming $I_{C\text{osc}}$ we can achieve frequency division and multiplication with fractional capabilities and without the use of binary dividers.

VII. Conclusion

In this paper, we have presented a new architecture of a CMOS fully integrated FLL design. The new approach is based on frequency comparison instead of phase comparison, such as in the case of conventional PLLs. This design is mainly composed of a new FVC, a VCO, and an operational amplifier. The presented FLL does not comprise a low-pass filter employed in the case of a PLL to guarantee its stability, but it is stabilized by the Miller compensation of the opamp. In this application, a capacitor of 12 pF is used to compensate the opamp and is sufficient to stabilize the whole system. Large transient simulation results show that the system is very fast and works over a wide frequency range which is determined (or fixed) by the VCO total delay cells. A version of this circuit was simulated using a 0.35-μm CMOS, and the results were reported. In addition, a functional test of five samples of a first version of this FLL proved that the proposed FLL works, as expected from Hspice simulation. The active area of the realized FLL occupies a space of 0.22 mm^2, which is very small compared to the area of an equivalent PLL. It follows that the present circuit could be integrated in the same die together with many other mixed-signal subsystems.

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