Architecture for frequency-to-current conversion

T.Y. Lin, E.M. Drakakis and A.J. Payne

A frequency-to-current converter based on a novel operational technique is considered. A circuit realisation using elementary translinear building blocks is proposed to implement both of the linear and nonlinear dynamics of the system.

Introduction: Frequency-to-voltage or frequency-to-current conversion is an important function and its use may be found in a variety of applications, such as speed control, flow measurement, tachometry, over/under speed sensing, touch or sound switches and many other applications in the field of instrumentation and power system control. A frequency-to-current converter (FCC) generates an output current proportional to the frequency of an input signal (the output current being readily convertible to voltage). The conversion from frequency-domain to current or voltage-domain, in principle, involves counting the number of zero-crossings on the time-axis in one form or another. It may be based on explicitly counting the number of narrow pulses over a fixed period of time or, by simple lowpass filtering which implicitly takes the average of fixed duration pulses [1]. Nevertheless, the overall performance does ultimately depend on the type of architecture employed. The existing types of approach, however, generally require complex circuitry for explicit pulse counting and averaging processes and are unsuitable for low frequency applications. A different architecture was introduced in [2], based on an analogue computational approach, in which the input frequency information is extracted via differentiation and integration performed in parallel, where clearly implicit pulse counting is involved. Though elegant, this architecture demands extremely precise differentiators and integrators. Slight phase mismatches between these two blocks would introduce large spikes at the output. In this Letter, we introduce a different architecture for frequency-to-current conversion. It takes the analogue computational approach, in which the counting on the time-axis remains implicit, and the matching between sub-systems is noncritical. This architecture is inherently fast, functionally dense and suitable for monolithic integrated implementation.

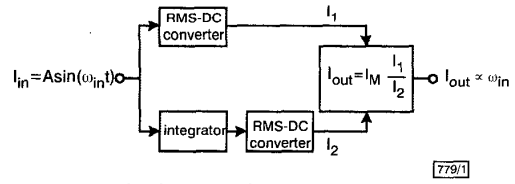

Fig. 1 *Basic principle of proposed frequency-to-current converter*

Principle of operation: The generic conceptualisation of the proposed FCC system is shown in Fig. 1. The system comprises four sub-blocks of three kinds: an integrator, two RMS-DC converters and a divider. The RMS-DC function gives an output current I_{out} that is equal to the mean value or the low-pass filtered version of I_{in}^2/I_{out}:

$$I_{out} = \left\langle \frac{I_{in}^2(t)}{I_{out}} \right\rangle \tag{1}$$

Assuming that the input signal I_{in} is a pure sinusoid with a peak amplitude A and input frequency ω_{in}

$$I_{in}(t) = A\sin(\omega_{in}t) \tag{2}$$

Taking the square of the input current and applying the double-angle identity gives

$$I_{in}^2(t) = A^2\left[\frac{1}{2} - \frac{1}{2}\cos(2\omega_{in}t)\right] \tag{3}$$

Thus the output of the RMS-DC converter becomes

$$I_1 = \left\langle \frac{I_{in}^2(t)}{I_1} \right\rangle = \frac{A^2}{2I_1} \tag{4}$$

resulting in the quasi-DC value [6]

$$I_1 = \frac{A}{\sqrt{2}} \tag{5}$$

On the parallel branch, the input current is first integrated, giving

$$I'_{in}(t) = -\frac{A}{\omega_{in}\tau_i}\cos(\omega_{in}t) \tag{6}$$

where τ_i is the time constant of the integrator. Subsequently $I'_{in}(t)$ is processed by a second RMS-DC converter, resulting in

$$I_2 = \left\langle \frac{I_{in}'^2(t)}{I_2} \right\rangle = \frac{A^2}{2I_2\omega_{in}^2\tau_i^2} \tag{7}$$

Thus,

$$I_2 = \frac{A}{\omega_{in}\tau_i\sqrt{2}} \tag{8}$$

Finally, I_1 and I_2 are fed into the divider, leading to

$$I_{out} = I_M\frac{I_1}{I_2} = I_M\tau_i\omega_{in} \tag{9}$$

Eqn. 9 shows that the output current is linearly proportional to the input signal frequency, confirming the operation of the FCC. Note that both sides of the equation are dimensionally consistent.

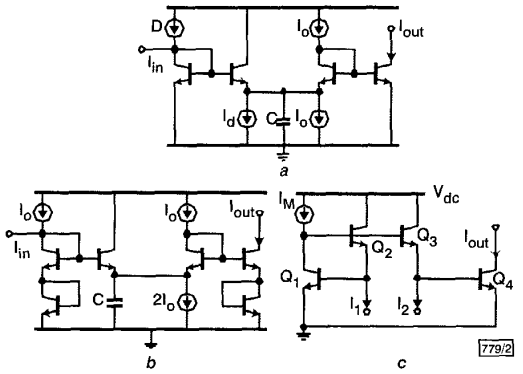

Fig. 2 *Circuit implementations*

a Log-domain integrator
b Translinear RMS-DC converter
c Translinear divider

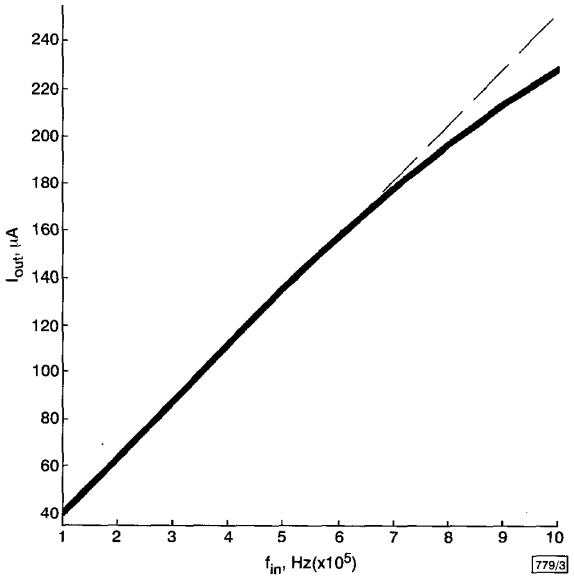

Fig. 3 *Simulated and expected transfer characteristics of proposed frequency-to-current converter*

——— simulated
– – – – expected

Circuit realisation: It is clear from the preceding Section that the principle of the proposed conversion system involves inherently nonlinear, dynamic processes. Thus we have adopted the translin-

ear principle based circuits because of their ease in implementing linear and nonlinear, static or dynamic functions [4, 5] and their high functional density.

(i) *Integrator:* A log-domain lossy integrator [5] shown in Fig. 2*a* is employed. The time-domain characteristics of the structure are described by the following differential equations:

$$CV_T\dot{F}(t) + I_dF(t) = I_{in}(t) \quad (10)$$

and

$$I_{out}(t) = I_OF(t) \quad (11)$$

(ii) *RMS-DC converter:* eqn. 1 shows that the RMS-DC function involves two separate functions: (1) square-divide and (2) lowpass filtering. The translinear first-order lowpass function is given by

$$CV_T\dot{I}_{out}(t) + I_OI_{out}(t) = I_OI_{in}(t)' \quad (12)$$

By suitably pre-processing the current $I_{in}(t)'$, i.e. $I_{in}(t)' = I_{in}^2(t)/I_{out}(t)$, the two distinct functions can be conveniently merged into a single nonlinear function described by the following nonlinear differential equation [3]:

$$CV_T\dot{I}_{out}(t)I_{out}(t) + I_OI_{out}^2(t) = I_OI_{in}^2(t) \quad (13)$$

The circuit that implements eqn. 13 is shown in Fig. 2*b*.

(iii) *Divider:* Consider the translinear circuit in Fig. 2*c*. Applying TLP gives

$$I_{out}I_2 = I_MI_1 \quad (14)$$

and thus,

$$I_{out} = I_M\frac{I_1}{I_2} \quad (15)$$

The output current is therefore linearly proportional to the ratio I_1/I_2, realising the division function.

Simulation of the complete system by interconnecting the above sub-circuits as shown in Fig. 1, with SpectreRF, using commercial bipolar transistor models confirm the basic principle of the proposed FCC, in that it produces a linear output current in response to the input frequency information, as seen from Fig. 3. Note that the same circuits can be designed using the MOS transistor operating in the sub-threshold regime.

Conclusion: A new frequency-to-current conversion principle has been proposed. Essentially, the proposed principle of frequency-to-current conversion is achieved by extracting the frequency information via a combination of integration (implicit pulse counting and averaging), and nonlinear dynamic processing (RMS-DC conversion and division). It is also shown that translinear circuits efficiently implement the necessary linear and nonlinear processing building-blocks of the proposed FCC.

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Compact low voltage four quadrant CMOS current multiplier

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A new compact low voltage four quadrant current mode CMOS multiplier is presented. Post layout simulation in a CMOS 0.5 μm technology shows a linearity error lower than 0.9% for signal swings up to ±50 μA. The circuit operates at a supply of ±1.5 V, has a static power dissipation of 0.6 mW and a 1 dB bandwidth of 33 MHz.

Introduction: Analogue multipliers are useful building blocks in the realisation of functions such as automatic gain control, modulation, filtering, etc. Various CMOS current multiplier circuits have been published in the literature [1 – 3] with transistors operating in either the weak or strong inversion region. In this Letter we present a new four quadrant current mode CMOS multiplier based on the quadratic current generator reported in [4]. The resulting multiplier has a high dynamic range, a high bandwidth and operates at a ±1.5 V supply. The circuit has a low input impedance and a high output impedance which ensure that the circuit can be directly used as a part of a larger current mode design. An analysis of the effect of device mismatch is also presented.

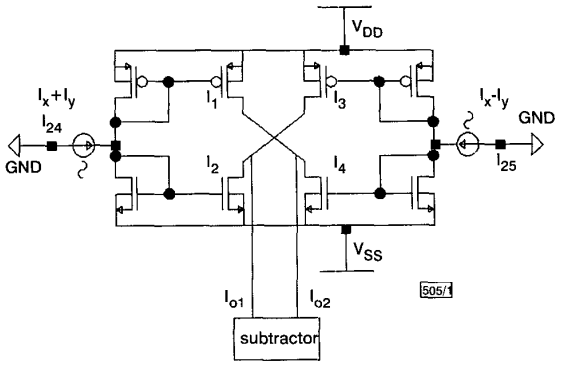

Fig. 1 *Multiplier circuit realised using core cell*

Circuit description: The proposed multiplier is based on the cell presented in [4] consisting of a back-to-back connection of two current mirrors with all transistors working in their saturation region. Two such cells with their outputs cross-coupled are shown in Fig. 1. Assuming that the MOS transistors are operating in the saturation region, it can be shown [4] that

$$I_1 = \frac{K}{2}\left(\frac{V_{DD} - |V_{tp}| - V_{tn}}{2} + \frac{I_x + I_y}{K(V_{DD} - |V_{tp}| - V_{tn})}\right)^2 \quad (1)$$

$$I_2 = \frac{K}{2}\left(\frac{V_{DD} - |V_{tp}| - V_{tn}}{2} - \frac{I_x + I_y}{K(V_{DD} - |V_{tp}| - V_{tn})}\right)^2 \quad (2)$$

$$I_3 = \frac{K}{2}\left(\frac{V_{DD} - |V_{tp}| - V_{tn}}{2} + \frac{I_x - I_y}{K(V_{DD} - |V_{tp}| - V_{tn})}\right)^2 \quad (3)$$

$$I_4 = \frac{K}{2}\left(\frac{V_{DD} - |V_{tp}| - V_{tn}}{2} - \frac{I_x - I_y}{K(V_{DD} - |V_{tp}| - V_{tn})}\right)^2 \quad (4)$$

where it has been assumed that $V_{SS} = 0$ V, $K_n = \mu_nC_{ox}W/L = K_p = \mu_pC_{ox}W/L = K$, and μ_n, μ_p, C_{ox}, W/L, V_{tn}, V_{tp} have their usual meanings.

The saturation condition can be ensured if we have

$$|I_x + I_y|, |I_x - I_y| \leq \frac{K(V_{DD} - |V_{tp}| - V_{tn})^2}{2} \quad (5)$$

The multiplier is based on obtaining the product of two currents, from the subtraction of the squares of their addition and difference. Then, from eqns. 1 – 4, I_{01} and I_{02} are derived as

$$I_{01} = I_1 - I_4 = I_x + \frac{2I_xI_y}{K(V_{DD} - |V_{tp}| - V_{tn})^2} \quad (6)$$