A Precision CMOS Bandgap Reference

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Abstract — **This paper describes the design of a precision on-chip bandgap voltage reference for applications with CMOS analog circuits. The circuit uses naturally occurring vertical n-p-n bipolar transistors as reference diodes. P-tub diffusions are used as temperature-dependent resistors to provide current bias, and an op-amp is used for voltage gain. The circuit is simple. Only two reference diodes, three p-tub resistors, and one op-amp are necessary to produce a reference with fixed voltage of −1.3 V. An additional op-amp with two p-tub resistors will adjust the output to any desired value.**

The criteria for temperature compensation are presented and show that the properly compensated circuit can *in principle* produce thermal drift which is less than 10 ppm/°C. Process sensitivity analysis shows that in practical applications it is possible to control the output to better than 2 percent, while keeping thermal drift below 40 ppm/°C. Test circuits have been designed and fabricated. The output voltage produced was −1.30± 0.025 V with thermal drift less than 7 mV from 0°C to 125°C. Significant improvements in performance, at modest cost in circuit complexity, can be achieved if the op-amp offset contribution to the output voltage is reduced or eliminated.

I. Introduction

In a large and complex LSI-CMOS analog circuit, the voltage reference is often a potentially most troublesome component since it must produce a temperature stable, process invariant, and precisely controlled output. In the past, most of efforts in voltage reference design have emphasized temperature compensation at the expense of output precision. The commonly used references based on the difference between gate/source voltages of enhancement and depletion mode MOS transistors realize low thermal drift; however, the absolute magnitude of output is poorly controlled because it depends on the accuracy of depletion and enhancement implants [1]. In the bandgap references, where the output is derived from the voltage difference of two diodes forward biased by ratioed currents, both the thermal drift and the absolute value of the output can be controlled with precision [2]–[4].

A CMOS bandgap voltage reference which uses bipolar-like source-to-drain transfer characteristics of MOS transistor in weak inversion was reported [5], [6]. The output voltage exhibited relatively low thermal drift and tight voltage spread from sample to sample. Another approach [7] used precision curvature-compensated switched capacitor CMOS bandgap reference. It required trimming and used a complex circuitry for generation of bias currents, thus consuming a large area.

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This paper describes the design of another simple bandgap circuit that can be conveniently implemented in CMOS technology. The output of this circuit is both temperature stable and precise. The circuit configuration which follows that given by Kuijk [8] uses temperature dependent p-tub resistors to provide bias currents to the reference diodes, which are the emitter–base junctions of the bipolar transistors formed by the n^+ diffusion inside the p-tub. First, the basic circuit and the criteria for temperature compensation are presented, followed by discussion of the characteristics of the reference diodes and biasing resistors. The sensitivity of the output voltage to the most common process variation, and the power supply fluctuations will then be discussed in detail. Finally, the experimental results to verify circuit performance will be presented to illustrate the precision and the stability of the circuit.

II. The Bandgap Circuit

In the bandgap circuit the output voltage is derived from the voltage difference across two identical diodes forward-biased by two unequal, precisely ratioed currents. The positive temperature coefficient of this difference is then cancelled by the negative temperature coefficient of voltage across one of the diodes. If the voltage across diode 1 is $V_1(T)$ and across diode 2 is $V_2(T)$, then the output can be expressed as

$$\begin{aligned} V_{\text{out}} &= A\big(V_1(T)-V_2(T)\big)+B\big(V_2(T)\big) \\ &= aV_1(T)-bV_2(T) \end{aligned} \tag{1}$$

where constants a and b are chosen to obtain a voltage V_{out} that has a minimum variation over the temperature range of interest.

The principles of bandgap references and the criteria for derivation of constants a and b are given in detail in [4]. These are derived for devices biased by either temperature independent constant current I, or currents which vary with temperature as T^{α}, where α is a constant. Neither one of these temperature variations of currents can be easily implemented in a CMOS analog circuit.

The bandgap circuit configuration used to derive the function in (1) is illustrated in Fig. 1. The first op-amp with transistors $Q1$ and $Q2$, and resistors $R1$, $R2$, and $R3$ is the bandgap circuit which produces a fixed voltage $V_{\text{out}} = -1.3$ V. The second op-amp with resistors $R4$ and $R5$ is a gain stage to adjust the output V_{ref} to a desired value. The discrete version of this bandgap circuit was first

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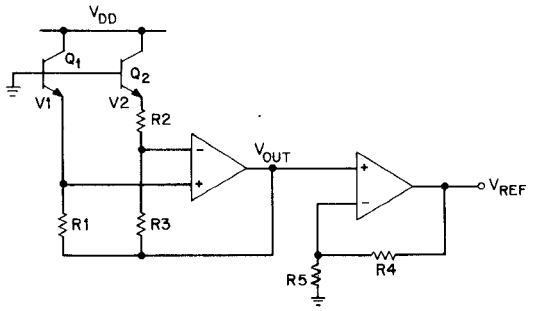

Fig. 1. Schematic of the CMOS bandgap circuit to produce negative output voltage. A bandgap source developing positive output with respect to ground is illustrated in [9].

proposed by Kuijk [8], who used integrated diode pairs and thin film resistors. More recently, Ye and Tsividis [9] have demonstrated this configuration, and a configuration producing a positive output voltage, using vertical n-p-n bipolar transistors and discrete external resistors. They also suggested using diffusion or polysilicon resistors in a fully integrated version of this circuit.

The gain constants a and b of circuit in Fig. 1 are given by

$$a = R_3/R_2 + 1 \tag{2}$$

$$b = R_3/R_2. \tag{3}$$

In addition to the gain of the circuit, which is determined by the ratio of resistors R_3 and R_2, the magnitude and the ratio of the bias currents is determined by the ratio of resistors R_1 and R_3:

$$I_1(T) = \frac{V_{\text{out}} - V_1(T)}{R_1} \tag{4}$$

$$I_2(T) = \frac{V_{\text{out}} - V_1(T)}{R_3} = \frac{V_{\text{out}} - V_2(T)}{R_3 + R_2}. \tag{5}$$

In this implementation, however, the biasing currents $I_1(T)$ and $I_2(T)$ are temperature dependent because of the variation of $V_1(T)$ and $V_2(T)$, and to a lesser extent because of the variation of V_{out} with respect to temperature. The conditions for the temperature compensation of this circuit with temperature independent R_1, R_2, and R_3 are given in [8].

In CMOS technology the situation is even further complicated because the only on-chip conductors that have large enough resistance values for proper biasing of the reference diodes are also temperature-dependent. The p-tub resistors approximately double their resistance for a temperature increase from 0 to 100°C.

The detailed derivation of the temperature compensation for the circuit illustrated in Fig. 1 is algebraically tedius and is briefly summarized in this section.

For a reference diode whose current I is given by Shockley's equation, for $qV \gg nkT$,

$$I = I_0 e^{qV/nkT}. \tag{6}$$

The voltage drop at temperature T is given by

$$V(T) = n\left[V_G(T) + \left(\frac{kT}{q}\right)\ln\left(\frac{I}{AT^{\beta}}\right)\right] \tag{7}$$

where n is the nonideality factor, $V_G(T)$ is the bandgap voltage at temperature T, k is the Boltzmann constant, q is the electron charge, A is a normalizing constant related to the geometry of the device, and β is a constant related to the fabrication process.

$V_G(T)$ is itself a function of temperature. Reference [10] gives the empirical expression for the bandgap value extrapolated from physical measurement over temperature range from 300 to 400 K.

$$V_G(T) = V_{G0} + \frac{dV_G}{dT}T \tag{8}$$

where $V_{G0} = 1.20595$ V, and $dV_G/dT = -2.7325 \times 10^{-4}$ V/K.

For a circuit whose function is given by (1), subject to the condition that the temperature coefficient at temperature $T = T_0$ is zero,

$$\left.\frac{dV_{\text{out}}}{dT}\right|_{T=T_0} = 0. \tag{9}$$

The value of the output voltage $V_{\text{out}}(T_0)$ is unique and given by

$$V_{\text{out}}(T_0) = n\left[V_{G0} + \left(\frac{kT_0}{q}\right) \cdot \left(\beta - 1 + T_0\left(\frac{1}{R(T_0)}\right)\left(\left.\frac{dR}{dT}\right|_{T=T_0}\right)\right)\right] \tag{10}$$

where $dR/dT|_{T=T_0}$ is the derivative of resistance of biasing resistors with respect to temperature at T_0.

The temperature response to the bandgap equation can be described by the following differential equation:

$$T\frac{dV_{\text{out}}}{dT} - V_{\text{out}} + \frac{nkT^2}{q}\left(\frac{1}{R}\right)\left(\frac{dR}{dT}\right) + \frac{nkT}{q}(\beta - 1) + nV_{g0} = 0. \tag{11}$$

It is important to notice that the value of $V_{\text{out}}(T_0)$ as given in (10), and the bandgap temperature response as given in (11) depends only on physical diode parameters n and β, and resistor temperature coefficient $(1/R)(dR/dT)$.

III. The Reference Diode in a CMOS Bandgap Circuit

It is well known that nearly ideal diode characteristics can be obtained from the base–emitter voltage V_{be} of a bipolar transistor. In the twin tub CMOS technology the vertical n-p-n bipolar devices are readily available with n^- substrate collector, p-tub base, and n^+ emitter.

In the layout of the bipolar devices five unit transistors are connected in parallel to make one reference diode. In this approach, similar to the one given in [6], the reference device can operate at larger biasing current, and in addition better matching of references can be achieved.

These devices, each unit transistor with 20 μm$\times$20 μm emitter, manufactured in the 3.5 μm linear twin tub CMOS process, were characterized to obtain the value of parameters n and β necessary to predict the voltage drop across the reference device as given in (7).

The value of n was determined by measuring I–V characteristics of the reference devices at room temperature between currents of 0.5 and 500 μA, and then fitting the measured voltage using (7), with n being the adjustable parameter. The voltage drop of the diode in the fit was normalized to the value at the lowest current. The best fit was obtained for $n=1.01$ over a range of currents from 0.5 to 25 μA. At currents above 25 μA, the differences between measured voltage and the fit were greater than 0.5 mV.

To measure the β parameter directly, the precise I–V characteristics of reference devices over a wide range of temperatures are needed. Such a measurement is tedious and difficult to do precisely, because a minor inaccuracy (as little as 0.5°C) in temperature measurement of the references, can lead to large errors in estimate of β. When these measurements are made on devices placed on a wafer prober, an uncertainty in temperature between the thermocouple in the wafer chuck, and the wafer itself can also cause significant errors in the value of β.

A new indirect method of measurement was used in determining the value β. A precision op-amp with low input offset and high open-loop gain, and a set of precision discrete resistors whose values were individually measured, were externally connected to the bipolar devices on the wafer. The connections were identical to those of the bandgap circuit, and the values of discrete resistors were selected to minimize the output variations with temperature. The voltage produced by the circuit was measured as a function of temperature of the reference diodes. A fit to the data as a function of β was made using the computer simulation of the bandgap circuit. Fig. 2 illustrates the measured and predicted responses of the circuit. The best overall agreement is for $\beta=1.775$.

The simulator used to obtain the best fit was written in Fortran. The program contains appropriate diode models given in (7), and (8), to generate the I–V–T characteristics of the reference diodes. Given diode characteristics, and the resistance values R_1, R_2, and R_3, the program solves iteratively for bias points V_1 and V_2, and output voltage V_{out} until,

$$\frac{V_{out}-V_1(R_1(T),T)}{R_1(T)}=\frac{V_{out}-V_2(R_3(T),T)}{R_2(T)+R_3(T)}\cdot\frac{R_3(T)}{R_1(T)}. \tag{12}$$

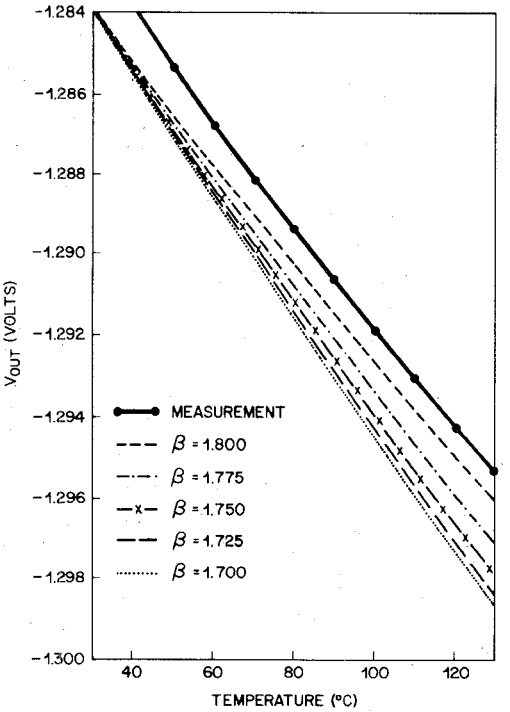

Fig. 2. Comparison of temperature response between simulated and measured fixed resistor bandgap circuit to determine the value of β.

This method of measurement is much less sensitive to vagaries in temperature measurement since the discrete resistors are chosen to minimize temperature dependence of the output voltage. This decreased output voltage sensitivity to temperature enables easier, and more precise determination of β.

IV. Biasing Resistors in the CMOS Bandgap Circuit

The results of the diode characterizations described in the previous section illustrate that the proper operation of reference devices requires small biasing currents in the microampere range. To provide these small currents, resistance values of the order of 10^5 Ω or higher are needed. The only on-chip conductor available in CMOS technology that has sufficiently high sheet resistance to render these resistors practical is the p-tub diffusion. The sheet resistance of the p-tub diffusion in the 3.5 μm twin tub CMOS technology is ~ 3 kΩ/□. Thus, resistor values up to 0.5 MΩ can be readily realized.

P-tub resistors exhibit temperature dependent behavior due to mobility changes over the temperature range of interest. The measurements of temperature effect on mobility variation of p-type silicon samples [11] yielded mobility dependence of $T^{-2.2}$. The measurements of temperature dependence of p-tub resistance, illustrated in Fig. 3, yielded essentially the same result.

Therefore, for a p-tub resistor,

$$R(T)=R_0T^{2.2} \tag{13}$$

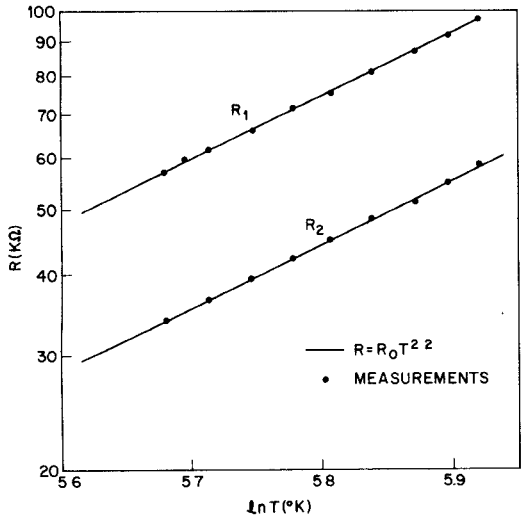

Fig. 3. Temperature characteristic of the p-tub resistors.

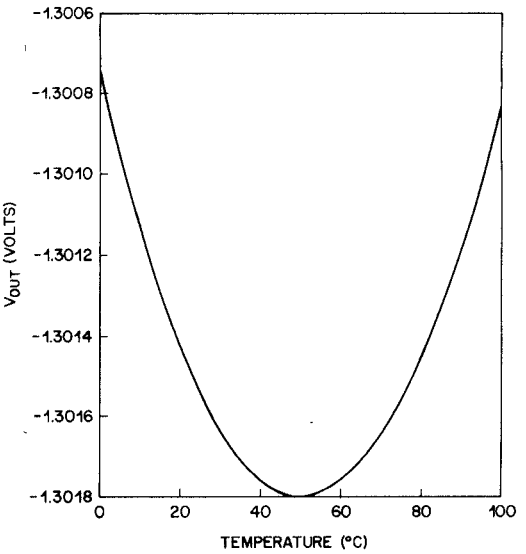

Fig. 4. Predicted temperature response of the bandgap circuit.

where R_0 is the normalizing constant. Therefore,

$$\left(\frac{1}{R}\right)\left(\frac{dR}{dT}\right)=\frac{2.2}{T} \tag{14}$$

and the proper compensation, according to formula (10), occurs when V_{out} at T_0 is

$$V_{\text{out}}(T_0)=n\left[V_{G0}+\left(\frac{kT_0}{q}\right)(\beta+1.2)\right]. \tag{15}$$

Fig. 4 illustrates the predicted temperature response of the bandgap circuit from 0 to 100°C, where the resistance of biasing resistors varies as $T^{2.2}$, the value of $\beta=1.775$, and the value of T_0 is 50°C. The value of $V_{\text{out}}(T_0)$ is -1.3018 V, and the temperature variation of V_{out} over 100°C is approximately 1 mV. The temperature coefficient that can be obtained using this approach is less than 8 ppm/°C.

V. Process Sensitivity of the Output Voltage

One of the advantages of the bandgap references over the threshold differencing scheme is that both magnitude and temperature compensation of the output voltage are relatively tolerant of processing variations. In this section an approximate analysis of the sensitivity of the output voltage to the processing variants will be presented. The current density ratio between reference diodes is 25:1 yielding voltage difference $(V_1-V_2)\sim 80$ mV at 25°C. The value of constants a and b in (1) is 10 and 9, respectively.

The main processing parameters that affect the output of the bandgap circuit are: p-tub doping, resistor mismatch, reference diode mismatch, and the threshold mismatch of the op-amp input devices. The threshold mismatch, which results in the op-amp offset error, mainly affects the magnitude of the output voltage if the offset itself is not a function of temperature. All other processing variations affect magnitude, as well as the temperature compensation of the output.

The doping of the p-tub affects the resistance of the biasing resistors and the V_{be} drop across the reference diodes. Both the value of the biasing resistors, and the V_{be} drop across the reference devices affect the voltages V_1 and V_2 of the circuit.

The resistance of the p-tub resistor uniformly doped by ion implantation is inversely proportional to the implant dose of boron N_s.

$$R\sim\frac{1}{N_s}. \tag{16}$$

Therefore, for a fractional error in implant dose dN_s/N_s, the fractional error on the p-tub resistance dR/R is;

$$\frac{dR}{R}\sim\frac{-dN_s}{N_s}. \tag{17}$$

For the n-p-n bipolar device biased with fixed V_{be}, the collector current is proportional to the number of impurities/unit area in the base [12] (also known as Gummel number). For the device with ion implanted p-tub base, this number is equal to the ion implant dose N_s. Therefore,

$$I\sim\frac{1}{N_s}e^{qV_{be}/kT} \tag{18}$$

and the V_{be} drop across the reference device is

$$V_{be}\sim\frac{kT}{q}\ln(IN_s). \tag{19}$$

The change in V_{be} of the reference device due to the p-tub ion implant error is

$$dV_{be}\approx\frac{kT}{q}\frac{dN_s}{N_s}. \tag{20}$$

The doping of the p-tub in the twin tub CMOS process can be controlled to ± 10 percent. This variation in the ion

implant dose should result in a $\pm 0.1\ kT$, or $\pm$ 2.5 mV error in V_{be} at room temperature.

From (19) the variation of the voltage across the reference device biased by the p-tub resistor resulting from the changes in V_{be} and the bias current is

$$dV_1 \approx dV_2 \approx \frac{kT}{q}\left[\frac{dN_s}{N_s} + \frac{dI}{I}\right]. \tag{21}$$

For bias current I in the circuit,

$$I = \frac{V_{\text{out}} - V_{be}}{R}, \tag{22}$$

the change in current dI is

$$dI = \frac{dV_{\text{out}} - dV_{be}}{R} - \frac{(V_{\text{out}} - V_{be})\,dR}{R^2} \tag{23}$$

for 10% resistance variation, the first term in (23) is small. Therefore,

$$\frac{dI}{I} \approx -\frac{dR}{R} \tag{24}$$

and using (17), (21), and (24)

$$dV_1 \approx dV_2 \approx \frac{2kT}{q}\left(\frac{dN_s}{N_s}\right). \tag{25}$$

The bandgap output voltage change is then

$$dV_{\text{out1}} = adV_1 - bdV_2 \approx (a-b)\,dV_1 \approx dV_1. \tag{26}$$

The total variation of the output voltage due to variation in the p-tub doping is

$$dV_{\text{out1}} \approx \frac{2kT}{q}\left(\frac{dN_s}{N_s}\right). \tag{27}$$

The ± 10 percent error in the p-tub implant will result in ± 5 mV error in the output voltage at room temperature. This is significantly better than the accuracy of the output voltage produced by the threshold differencing circuit due to the ion implant variation.

The V_{be} voltage produced by the reference devices is very uniform, and the mismatch of the voltage across different devices of the same size on the same chip is small. The measurements of the reference devices biased with constant current on the different chip sites of the same wafer yielded the maximum mismatch of less than 0.2 mV. Such a mismatch would result in a output voltage change of

$$dV_{\text{out2}} \approx adV_1 \approx bdV_2 \approx 2 \text{ mV} \tag{28}$$

where the value of $a = 10$ is used.

The mismatch of the resistor ratio R_3 and R_2 affects the gain of the circuit. The mismatch of the ratio R_1 and R_3 influences the current ratio supplied to the references, and thus the difference between V_1 and V_2.

The resistances R_1 and R_3 can be matched accurately because they can be ratioed by an exact integer factor, and also because R_1 and R_3 have an identical voltage across them thus eliminating problems due to any nonlinearities of p-tub resistance. The mismatch of R_2 and R_3 is more likely to occur since these resistors are ratioed by a noninteger number, and because R_2 is biased at a different potential from the substrate than R_1 and R_2. Therefore, only R_3/R_2 mismatch will be considered here.

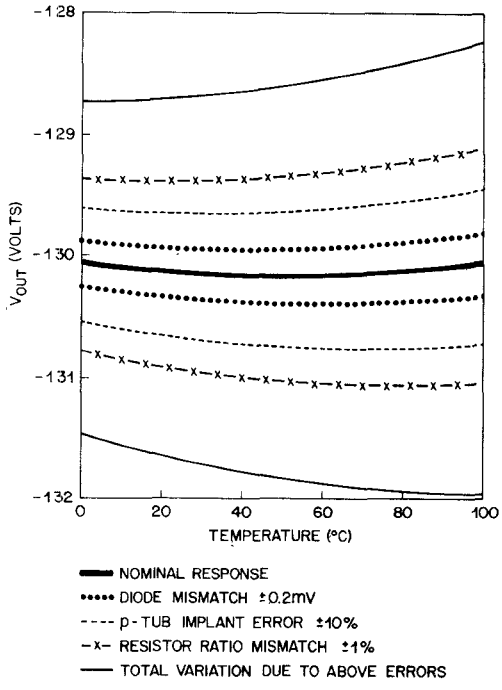

Fig. 5. Sensitivity of output voltage to processing variations.

The variation of the output voltage of the bandgap circuit due to mismatch of R_3, and R_2 is

$$dV_{\text{out3}} = d\left(\frac{R_3}{R_2}+1\right)V_1 - d\left(\frac{R_3}{R_2}\right)V_2 = d\left(\frac{R_3}{R_2}\right)(V_1 - V_2). \tag{29}$$

In a careful layout the resistance values of the p-tub resistors can be matched better than 1 percent. Therefore, for 1 percent resistance mismatching and 80 mV difference between V_1 and V_2, with $R_3/R_2 = 10$ the output voltage error is

$$dV_{\text{out3}} = 0.01\left(\frac{R_3}{R_2}\right)(V_1 - V_2) \approx 8 \text{ mV}. \tag{30}$$

The above discussion illustrated that excluding the offset error of the op-amp the various processing variations can affect the output voltage of the bandgap circuit by about ± 15 mV at room temperature in the worst-case analysis. This is only about 1.2 percent of the total voltage produced by the bandgap circuit. The estimate of the effect of these parameters on temperature compensation is considerably more difficult and was done using the numerical bandgap simulator discussed in Section III. Fig. 5 illustrates the predicted worst-case behavior of the bandgap circuit and how each processing variation contributes to errors in the output voltage temperature compensation.

In this simulation the output of each reference diode voltage was varied by ± 2.5 mV, reference device mismatch was varied by ± 0.2 mV, the sheet resistivity of biasing resistors was varied by ± 10 percent and the ratio of resistors was mismatched by ± 1 percent. The worst-case analysis yields the temperature compensation of the output voltage of about 5 mV over the temperature range from 0 to 100°C.

The input offset error of the summing op-amp can have significant and detrimental effect on the control of the magnitude of the output voltage. An analysis of the bandgap circuit shown in Fig. 1, which includes the offset error of the op-amp, gives the following relation for V_{out}.

$$V_{\text{out}} = aV_1 - bV_2 + cV_{os} \tag{31}$$

where a and b are given in (2) and (3), V_{os} is the offset, and

$$c = -\left(1 + \frac{R_3}{R_2}\right) = -a. \tag{32}$$

The offset of the op-amp is therefore multiplied by the factor c. In a typical bandgap circuit, $c \approx 10$; thus, small offset value of the op-amp can contribute a large error to the output voltage.

VI. Sensitivity of Output Voltage to Power Supply Variations

The primary effect of the power supply variation on the output voltage of the bandgap circuit comes from change of the reverse bias on the biasing p-tub resistors R_1, R_2, and R_3. This, in turn changes their resistance values resulting in modified gain factors and bias currents to reference diodes.

In the circuit, resistors R_1 and R_2 are identically biased with respect to the substrate, although they operate at different current densities. R_2 is biased approximately 80 mV more positive than the other two. Therefore, neglecting the influence of bias current, the voltage coefficients of R_1 and R_3 should be identical

$$\frac{1}{R_1}\frac{dR_1}{dV_{\text{sup}}} = \frac{1}{R_3}\frac{dR_3}{dV_{\text{sup}}}. \tag{33}$$

After tedious algebra, using (1), (2), (3), (4), (5), (7), and (33) one can compute the total variation of the output voltage to be

$$\frac{dV_{\text{out}}}{dV_{\text{sup}}} = \frac{R_3}{R_2}\left[\frac{1}{R_3}\frac{dR_3}{dV_{\text{sup}}} - \frac{1}{R_2}\frac{dR_2}{dV_{\text{sup}}}\right](V_1 - V_2) \frac{-nkT}{q}\left[\frac{1}{1 + \frac{nkT}{q}\left(\frac{1}{V_{\text{out}} - V_1}\right)}\right]\left(\frac{1}{R_1}\right)\left(\frac{dR_1}{dV_{\text{sup}}}\right). \tag{34}$$

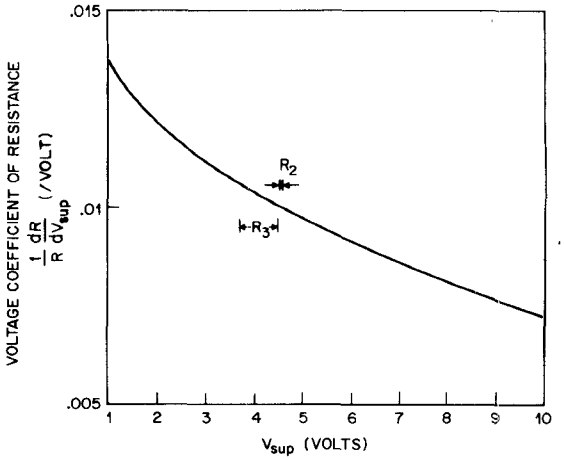

Fig. 6. Voltage coefficient of p-tub resistance as a function of substrate bias (V_{sup}).

The first term in brackets depends on differences between voltage coefficients of resistance between R_1 (or R_3) and R_2 due to different reverse biasing conditions. Fig. 6 illustrates the normalized voltage coefficient of the p-tub resistor as a function of reverse bias. (This curve is shown for an arbitrary current approximating operating point of R_3 resistor. The shape of the curve varies slightly at different currents.) On this curve the bias voltages are marked for resistors R_3 and R_2. Since the difference between the two coefficients of those points is small ($< 10^{-3}$), the first term in (34) is less than 0.8 mV/V.

The second term in (34) results from modified current through reference diodes. Again, a quick computation shows this value to be ~ 0.2 mV/V. The total expected variation of the output is therefore expected to be about 0.6 mV/V.

VII. Preliminary Results

Fig. 7 shows the photomicrograph of the circuit designed to test the performance of the resistor bandgap circuit. The operational amplifiers used in the circuit are described in [13]. The tester uses a second op-amp with p-tub resistors R_4 and R_5 to adjust the output voltage to a desired value. Because the gain of this stage is determined only by resistance ratio and not by resistance values themselves, it is reasonably precise and independent of temperature. The total circuit size, including the second op-amp and resistors R_4 and R_5, is 0.4 mm^2. The power consumption is 2 mW. In this paper only the results relating to the output of the first op-amp will be discussed. The data are based on measurements obtained from three device lots fabricated in the 3.5 μm linear twin tub CMOS process.

Fig. 8 shows the measured temperature response of one sample circuit along with the predicted response obtained from computer simulation. The output voltage shown has been compensated for the input offset error of the op-amp by measuring the offset contribution and subtracting it from the measured output of the circuit. The amplified

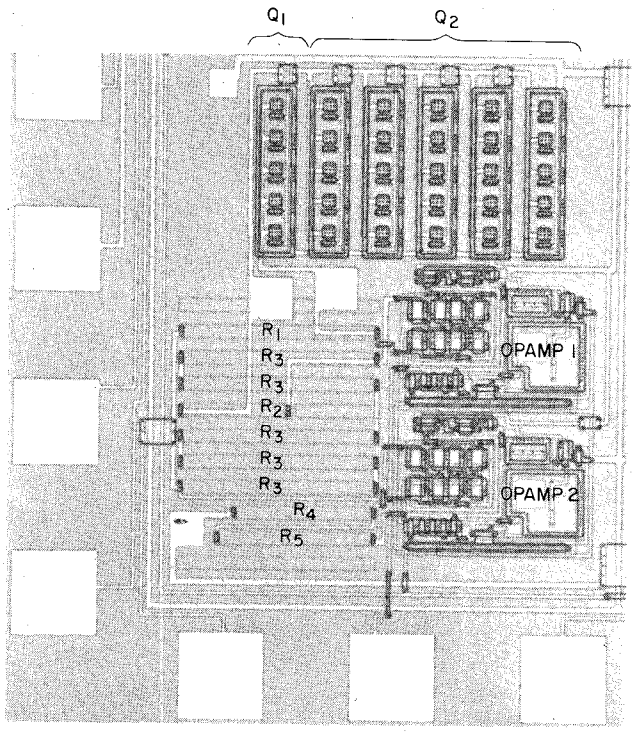

Fig. 7. Photomicrograph of the bandgap test circuit.

offset contribution was measured by grounding emitters of Q_1 and Q_2 through internal pads and measuring the output. The predicted temperature response and the value of the output voltage agree well with the compensated measured values. The temperature stability of the output is better than 2 mV from 0 to 125°C.

More complete measurements of circuits on different chip sites of a single wafer show that the offset compensated output voltage variation is 3 mV at room temperature. The wafer to wafer variation of the offset compensated output is 7 mV while the temperature stability of the output of most the circuits is better than 5 mV from 25 to 125°C.

As expected, the largest contribution to the output error comes from the input offset of the CMOS summing op-amp. Fig. 9 shows the typical temperature responses of three randomly selected circuits from three separate wafer slices from three wafer lots. For comparison, the output of these circuits with op-amp offset subtracted are also shown. The bulk of the output voltage variation in these samples is due to the offset of the op-amp. More extensive measurements indicate that the output voltage of individual circuits may vary by ± 15 mV due to the offset error alone. In the extreme cases of large offset errors, the offset itself may be temperature-dependent, and may add 2 mV to the temperature instability of the bandgap circuit.

The sensitivity of the output to power supply variations was measured at room temperature with power supply voltage varied from 4.75 to 5.25 V. The output of most of the circuits changed by less than 0.3 mV, the mean was 0.4 mV. The maximum variation, observed on small percentage of samples, was 1.1 mV. The output variation is larger than predicted in Section VI. The differences are

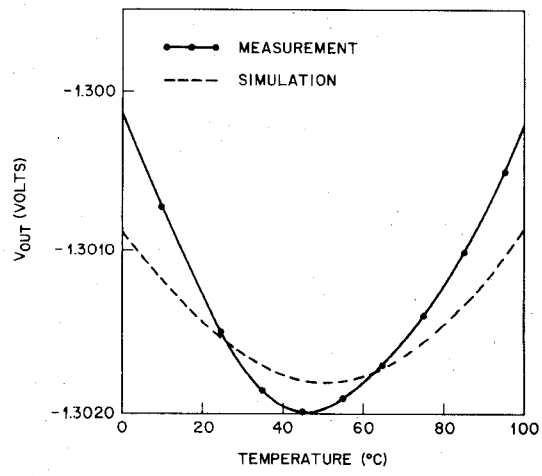

Fig. 8. Measured and predicted temperature responses of the bandgap circuit after compensation for the op-amp offset.

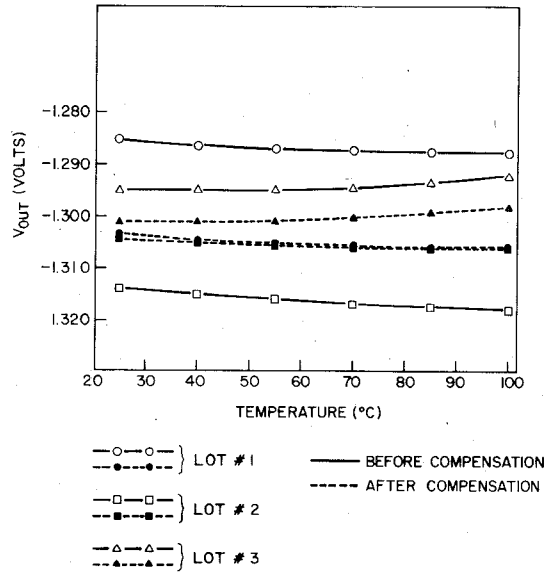

Fig. 9. Measured temperature response of three randomly selected bandgap circuits from three separate wafer lots.

likely due to omission in analysis of the influence of bias current on the voltage coefficient of resistance of R_1 and R_3.

The preliminary data suggest that without any offset cancelling technique, the output voltage of the bandgap circuit is $1.30 \pm .025$ V, while the worst-case temperature drift is 7 mV from 0 to 125°C. Dramatic improvement in performance at modest cost in circuit complexity can be achieved if input error contribution is reduced either by cascading reference devices, or by offset cancelling techniques [14].

VIII. Conclusions

The design of a simple and practical precision CMOS bandgap reference circuit which uses p-tub temperature dependent resistors and naturally occurring n-p-n bi-polar transistors is described. The criteria for the proper temperature compensation of the output voltage are derived and

are shown to be independent of the design parameters such as current values and their ratios, resistor values, or diode bias points. The diodes manufactured in the 3.5 μm twin tub linear CMOS process are shown to be acceptable for the references in the bandgap circuit. The magnitude and temperature stability of the output voltage is shown to be tolerant to the most common variations of the CMOS process. The performance of the test circuits matches well the predictions of the bandgap response made by the bandgap computer simulations. The output voltage of the circuit is $-1.30 \pm .025$ V with temperature stability better than 7 mV from 0 to 125°C. A version of this circuit, which produces positive output is shown in [9]. A dramatic improvement in the performance can be achieved if op-amp offset error contribution is reduced by using offset correcting techniques.

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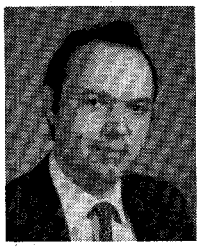

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