A New Level-Up Shifter for High Speed and Wide Range Interface in Ultra Deep Sub-Micron

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***Abstract*— A New level-up shifter aimed at ultra low core voltage and wide range I/O voltage is designed using a 90nm CMOS process. Proposed level shifter uses analog circuit techniques and standard zero-Vt NMOS transistor without adding extra mask or process step. No static power consumption and stable duty ratio make this level shifter suitable for wide I/O interface voltage applications in ultra deep sub-micron. These techniques work even 0.6V core voltage, 1.65~3.6V I/O voltage, within 45:55 duty ratio up to 200MHz.**

I. INTRODUCTION

To achieve high performance and high integration density, the transistor dimensions are aggressively scaled down in ultra deep submicron process while low power dissipation is achieved by scaling down the supply voltage even under 1.0V. But, Still 3.3V I/O voltage is the main stream of I/O interface. Level shifter circuits are widely used as the bridges that connect low core voltage to high I/O interface voltage for interfacing logic and functional devices or circuits. A level shifter using bootstrapping technique has been reported[1]. This paper describes level-up shift aims at ultra low core voltage and wide range I/O voltage in high speed application.

II. PRIOR ARTS

A. Conventional Level Shifter Type-I

The conventional level shifter using cross-coupled PMOS load is shown in Fig.1. Thick gate oxide transistor was used for MN11, MN12, MP11 and MP12 to overcome high voltage stress. The gate source voltage(Vgs) of MN11 and MN12 supply latching seed voltage on node T1 and T2. This voltage is used for cross-coupled MP11,and MP12 to positive feedback action which result in fully VDD2 voltage in node T1. Current driving capability for MN11 and MN11 are decided core voltage(vdd1) but those of MP11 and MP12 are controlled by the I/O voltage(vdd2). When V_A is low, MN11 and MP12 are turn on and MN12 and MP11 are turn off. At that time if V_A switches to high, following procedure is take place. MN11 off, MN12 on → MP11 on→ T1 switch low to high→ MP12 off. Finally the transition time from low voltage to high voltage is decided by the current driving capability of MP11. Pull-down nmos has to overcome the PMOS latch action before the output change state, so the size of MN11 and MN12 are much larger than MP11, MP12.

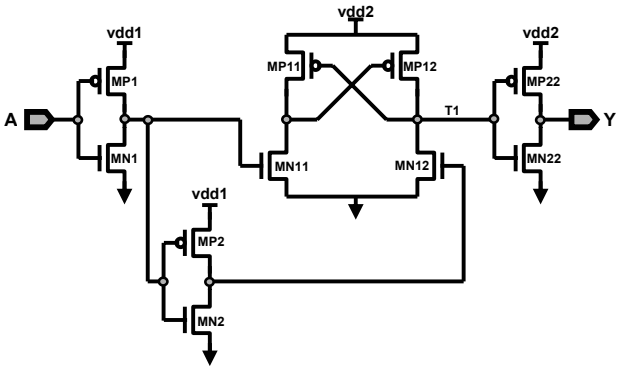

Figure 1. Conventional level-up shifter(Type-I).

However, conventional level shifter do not operate any more as the core voltage decrease under 1V because of the thick gate oxide transistor's (MN11, MN12) high threshold voltage. The current driving ability of MP11 and MP12 is affected by source voltage(VDD2). When I/O voltage(VDD2) changes which makes different current driving capability result in delay variation in level-shifter, so above feature is not adequate for wide range voltage application in a given core voltage.

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B. Conventional Level Shifter Type-II

Another conventional low to high level-shifter is depicted in Fig. 2. Unlike cross-coupled level-shifter[2], the current driving capability for MP11 and MP12 is decided gate-source voltage(Vgs,MP11) regardless of VDD2 voltage level, and the saturation current of MN11 determines Vgs,MP11. The current driving ability of MP11 and MP12 is not affected by I/O voltage(VDD2) but MP11 and MP12 threshold voltage, it shows stable current driving capability.

Compare to cross-coupled level-shifter this shows better performance in operating speed within same size. Due to gate oxide transistor of MN11 and MN12, it has weak point in low core voltage, specially under 1V. To operate at ultra low core voltage, the low to high level shifting block MN11 and MN12 need to be changed to thin gate-oxide transistor.

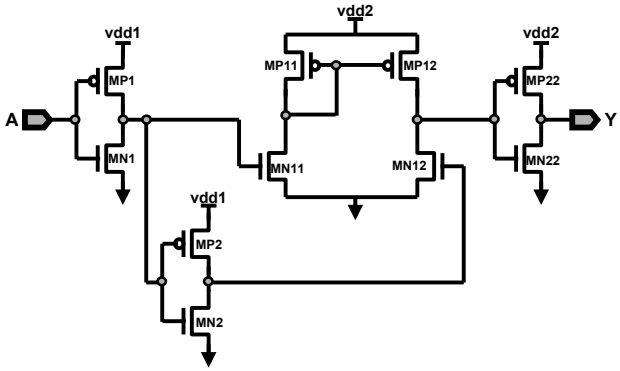

Figure 2. Conventional level-up shifter (Type-II).

The current driving ability of MP11 and MP12 is not affected by I/O voltage(VDD2) but MP11 and MP12 threshold voltage, it shows stable current driving capability. This circuit is suitable to wire range I/O voltage application, also it has a leakage current path when MN11 and MP11 on at the same time.

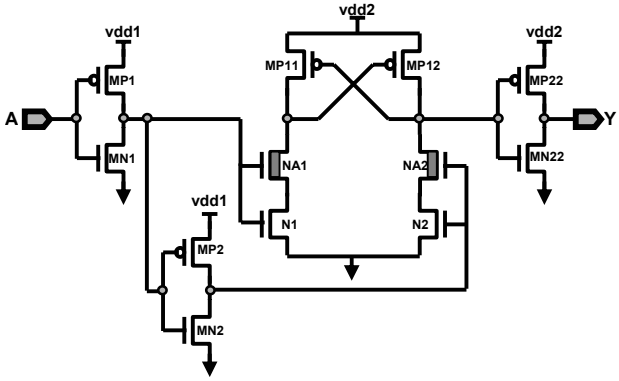

Figure 3. Conventional level-up shifter (Type-III)

C. Conventional Level Shifter Type-II1

Fig. 3. shows modified cross-coupled 1V to 3.3V level-shifter[3]. The drawback of conventional level-shifter, operation in low core voltage(VDD1), was solved using thin gate-oxide transistor in nmos switch N1, N2. zero-Vt 3.3V nmos NA1 and NA2 are used to protect 1.0V nmos N1 and N2 from high voltage stress. But, this circuit is not applicable for ultra low core voltage and wide range I/O voltages such as 0.6V core voltage and I/O voltage is from 1.65V to 3.6V.

III. PROPOSED LEVEL-UP SHIFTER

Fig.4. shows a novel low to high level-shifter which operate in ultra low core voltage(0.6V) and wide I/O voltage ranges(1.65V~3.6V) with small duty ratio variation under process, voltage and temperature corners. Thin gate-oxide input stage of level shifting block is used to operate under ultra low core voltage. To avoid source-drain over stress voltage for MN11 and MN12, Thick gate-oxide zero-Vt. Transistor MN31 and MN32 is used. In case of input signal, A, changes high to low, when A is high MN11 is 'off' and MN12 is 'on' at that time the MP11 and MP12 is 'off' due to gate voltage MP11 and MP is below those transistor's threshold voltage. Even MN31 is 'on' during this event leakage current does not exist due to MN11 and MP11 is 'off'.

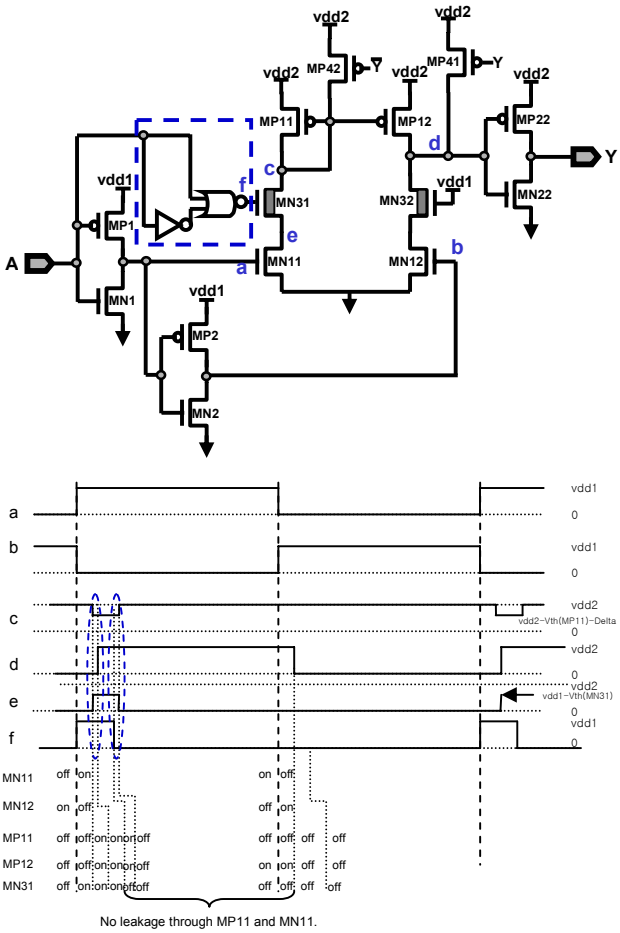

Figure 4. Proposed level-up shifter

When A switches to low, MN11 is turn ‘on’ which makes MP12 ‘on’ and MN12 ‘off’. MP12 makes the final level-shifter output voltage to low. Switch element turns on MN31 only A transfer low to high. After finishing logic transition, MN31 is ‘off’ and cuts the leakage path without feedback path which was used conventional Type-II level shifter. At that time the gate voltage of MP11 and MP12 is discharged through the MP11 which makes MP11 and MP12 is ‘off’. In this case both MN12 and MP12 is ‘off’ temporary. If those transistors are off at the same time input node-d is floating. To prevent this event MP41 and MP42 are added.

IV. Simulation Results

Transition characteristics of conventional and proposed level-up shifters are simulated under following conditions. The operating voltage for core logic and I/O is 0.6V to 1.0V and 1.65V to 3.6V, respectively. -55°C and 125°C junction temperature and 5 corners of spice parameters of 90nm CMOS process were considered. 200MHz signal frequency and 0.05pF output load is selected. The conventional Type-I level shifter does not operate under 0.9V core voltage. Low voltage operation characteristics is improved to 0.7V core voltage in Type-III, but this type of level shifter is not suitable to wide range I/O operating voltage(1.65V~3.6V) because of the degradation of duty ratio. The 45:55 duty ratio for 3.0V~3.6V is increased up to 25:75 under 1.8V I/O voltage ranges. Otherwise, the proposed level-up shifter works even 0.6V core voltage without duty ratio degradation. Fig.5. shows simulated waveforms at 200MHz signal frequency in all PVT corners. The duty ratio characteristic of proposed level shifter is shown in Fig.6. The x-axis represents overall simulation cases and y-axis shows duty ratio. Due to the stable duty ratio, proposed level shifter is suitable to wide range I/O voltage application without circuit modifications.

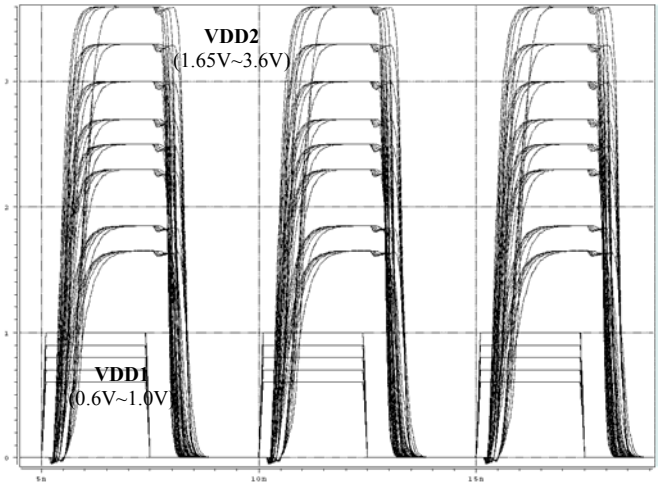

Figure 5. Simulation results with 200MHz Signal

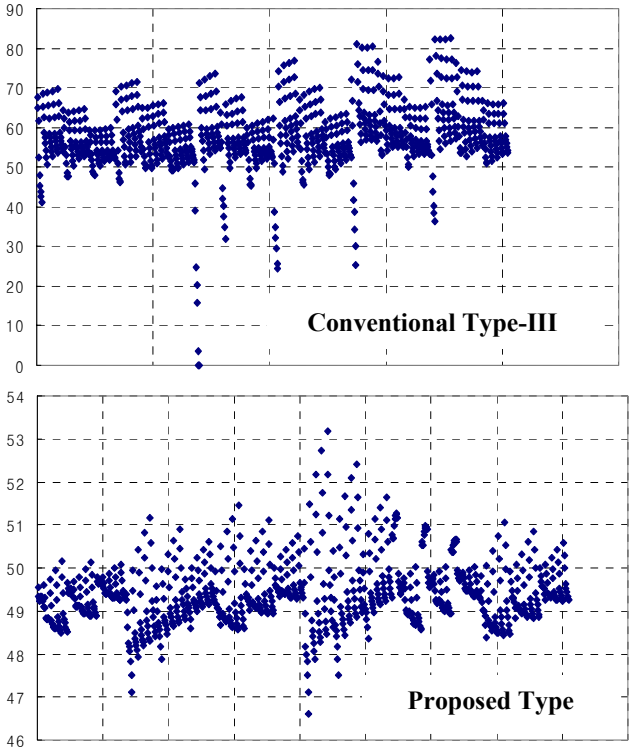

Figure 6. Duty Ratio Comparison
(X-axis: simulation cases / Y-axis: duty ratio)

V. Conclusions

A level shifter aimed at ultra low core voltage and wide range I/O voltage is designed using a 90nm CMOS process. Proposed level shifter uses analog circuit techniques and zero-Vt transistor with no extra process step. No static power and stable duty ratio make this level shifter suitable for ultra low core voltage and wide range I/O voltage applications. These techniques work even 0.6V core voltage, 1.65~3.6V I/O voltage within 45:55 duty ratio up to 200MHz.

References

[1] T.F Knight and A. Krymm, “A self-terminating low-voltage swing CMOS output driver,” IEEE J. Solid-State Circuits, vol. 23, no.2, pp.457-464, Apr. 1988.

[2] Harold Pilo and Steve Lamphier., “A 300MHz, 3.3V 1Mb SRAM fabricated in a 0.5um CMOS process,” ISSCC. Digest of Technical Papers, vol. 31, no. 12, pp. 148-149, Feb. 1993.

[3] Wen-Tai Wang, et al., “Level Shifters for high-Speed 1V to 3.3V Interfaces in a 0.13um Cu-Interconnection/Low-k CMOS Technology,” Proc. Of Symp. On VLSI Circuits, pp. 307-310, June 2001.