A 1-V CMOS Current Reference With Temperature and Process Compensation

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***Abstract*—A 1-V current reference fabricated in a standard CMOS process is described. Temperature compensation is achieved from a bandgap reference core using a transimpedance amplifier in order to generate an intermediate voltage reference, $V_{\rm REF}$. This voltage applied to the gate of a carefully sized nMOS output transistor provides a reference drain current, $I_{\rm REF}$, nearly independent of temperature by mutual compensation of mobility and threshold voltage variations. The circuit topology allows for compensation of threshold voltage variation due to process parameters as well. The current reference has been fabricated in a standard 0.18-μm CMOS process. Results from nineteen samples measured over a temperature range of 0 °C to 100 °C, showed values of $I_{\rm REF}$ of 144.3 μA $\pm$ 7% and $V_{\rm REF}$ of 610.9 mV $\pm$ 2% due to the combined effect of temperature and process variations.**

***Index Terms*—CMOS, current reference, low voltage, process and temperature compensation, transimpedance amplifier.**

I. Introduction

CURRENT references play an important role in analog and mixed-signal systems. They are a key component in analog to digital and digital to analog converters and they are also found in numerous analog circuits such as operational amplifiers (OAs), filters and monolithic sensors. As more of these systems are used remotely, the demand for low power, low voltage references increases while conventional bandgap architectures require a supply voltage higher than 1.25 V [1]. Meanwhile, the cost per function offered by sub-micron CMOS processes continues to decrease which challenges designers to conceive circuits using those technologies while matching the performances of more mature processes.

Recent works demonstrated the difficulty to obtain current references fabricated in CMOS processes having an output current independent of process variations. In [2], from a circuit using native MOS transistor and a trimmable n-well resistor chain, a temperature variation coefficient (TC) of 368 ppm/°C was obtained. Circuits employing p-i-n diodes [3] and MOSFETs operating in week and moderate inversions [4] showed an output current variation of $\pm$5% and $\pm$10%, respectively, due to temperature and process parameter drifts. In [5], a current reference showing a TC of 50 ppm/°C was measured, however, no result on process variation was reported. Since the reference current was a function of the absolute value of a resistor and of the base-emitter voltage of a p-n-p transistor, minimum chip to chip variation of the output current could be in the vicinity of $\pm$10%. Finally, [6] reported on a current reference having a combined temperature and process variations of $\pm$5% obtained on a circuit fabricated in a 0.15-μm CMOS process.

This paper describes a CMOS current reference based on a low supply bandgap voltage reference (BGR) in order to provide a temperature compensated voltage. The temperature compensated current is obtained by applying the BGR's output voltage to an nMOS output transistor. Proper sizing of the output transistor allows the device to operate in the vicinity of the zero TC (ZTC) point [7]. At this point, mutual compensation of threshold voltage and mobility variations, due to temperature, is producing an output current reference nearly independent of temperature. In addition, good matching of the output transistor with key transistors of the BGR provides a process compensation scheme for the current reference. This paper is organized as follows: in Section II, the basic principle of the process parameter compensation scheme is described and the theory of the ZTC bias point is reviewed. Since the architecture of BGR is intertwined with the temperature compensation scheme, Section III presents the theory of operation of the BGR and its circuit architecture. In Section IV, measurements of the voltage and current reference performed on nineteen samples under three different temperatures are compared with measured ZTC operating points of the output transistor. Finally, Section V summarizes the main contributions of this paper.

II. Process Parameter Compensation and ZTC Bias Point

A. Process Parameter Compensation

Since current references require high output impedances, the output current is inevitably generated at the drain of a transistor as shown in the simple scenario in Fig. 1. In this case, the inter-die variation of the output current, $I_{\rm REF}$, depends mainly on the accuracy of its gate–source voltage, equals to $V_{\rm REF}$, and the reproducibility of the threshold voltage, $V_{\rm TH4}$, of transistor M_4, according to the equation of the drain current in the saturation region

$$I_{\rm REF} = \frac{\mu_n C_{\rm ox}}{2}\frac{W_4}{L_4}(V_{\rm REF} - V_{\rm TH4})^2. \quad (1)$$

Assuming an hypothetical case were $V_{\rm REF}$ is identical on every die, $I_{\rm REF}$ would still experience a large variation due to the $V_{\rm TH4}$ voltage shift that could reach $\pm$100 mV according to the

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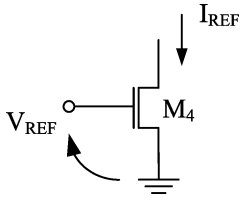

Fig. 1. Simple circuit to generate a current reference.

SPICE model file of the 0.18-μm CMOS process used to design this circuit. From the total derivative of expression (1)

$$\frac{dI_{\rm REF}}{I_{\rm REF}} = \frac{d(\mu_n C_{\rm ox} W_4/L_4)}{\mu_n C_{\rm ox} W_4/L_4} + 2\frac{(dV_{\rm REF} - dV_{\rm TH4})}{(V_{\rm REF} - V_{\rm TH4})} \qquad (2)$$

the second term of relation (2) indicates that $dI_{\rm REF}/I_{\rm REF}$ is dependent on the difference in variations $dV_{\rm REF}$ and $dV_{\rm TH4}$. Hence, the influence of threshold voltage variations on $I_{\rm REF}$ could be largely reduced by applying a process sensitive voltage $V_{\rm REF}$, where its variation is positively correlated to the one of $V_{\rm TH4}$ in order to keep the term $(dV_{\rm REF} - dV_{\rm TH4})$ of (2) as small as possible. In these conditions, for a transistor M_4 conceived with a width W_4 and a length L_4 several times larger than the minimum size allowed by the technology $I_{\rm REF}$ would remain dependent only on shifts of the oxide capacitance $C_{\rm ox}$, and the mobility μ_n from their nominal values.

B. ZTC Bias Point

A temperature-independent $I_{\rm REF}$ is obtained by operating the output transistor M_4 at the ZTC bias point. The threshold voltage $V_{\rm TH4}$ and the mobility μ_n of M_4 are dependent on the temperature and can be approximated with the following relations [7]:

$$V_{\rm TH4}(T) = V_{\rm TH4}(T_0) + \alpha_{VT}(T - T_0) \qquad (3)$$

where α_{VT} is a negative constant and T_0 is the reference temperature, and

$$\mu_n(T) = \mu_n(T_0)\left[\frac{T}{T_0}\right]^{\alpha_\mu} \qquad (4)$$

where α_μ is also a negative constant. By inserting (3) and (4) in (1), the temperature dependence of $I_{\rm REF}$ becomes

$$I_{\rm REF} = \frac{C_{\rm ox}}{2}\frac{W_4}{L_4}\mu_n(T_0)\left[\frac{T}{T_0}\right]^{\alpha_\mu} \times (V_{\rm REF} - [V_{\rm TH4}(T_0) + \alpha_{VT}(T - T_0)])^2. \qquad (5)$$

For carefully sized nMOS transistors with channel doping concentration in the vicinity of 10^{15} to 10^{16} cm^{-3}, the constant α_μ is close or equal to -2 [7]. In this condition, there is a gate–source voltage $V_{\rm REF}$ equals to

$$V_{\rm REF} = V_{\rm ZTC} = V_{\rm TH4}(T_0) - \alpha_{VT}T_0 \qquad (6)$$

where the output current $I_{\rm REF}$ becomes independent of the temperature

$$I_{\rm REF} = I_{\rm ZTC} = \frac{\mu_n(T_0)}{2}C_{\rm ox}\left(\frac{W_4}{L_4}\right)(\alpha_{VT}T_0)^2. \qquad (7)$$

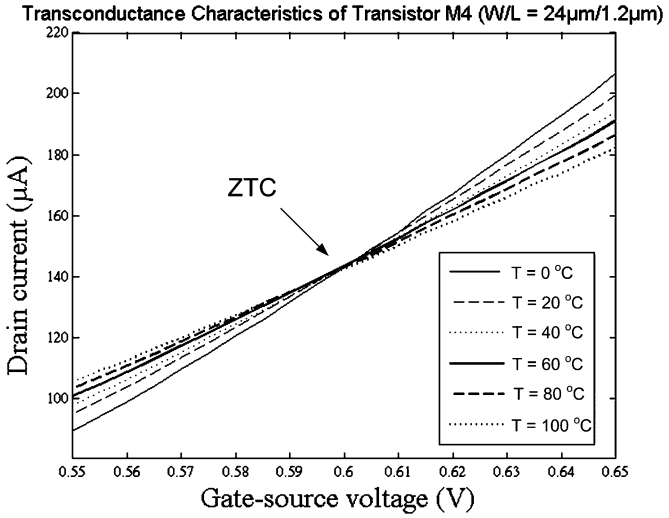

Fig. 2. Measured transconductance characteristics of output transistor M_4 showing the ZTC operating region.

The transistor M_4 biased at $(I_{\rm ZTC}, V_{\rm ZTC})$, then presents a transconductance characteristic independent of the temperature. Fig. 2 shows the transconductance characteristics measured for five temperatures for the nMOS transistor M_4 fabricated in a 0.18-μm CMOS process. The result indicates a ZTC point at $V_{\rm ZTC}$ of 595 mV and a $I_{\rm ZTC}$ of 139 μA.

The proposed circuit has been designed to generate a process sensitive reference voltage, $V_{\rm REF}$, in order to cancel inter-die shifts of $V_{\rm TH4}$ of the output transistor M_4. In addition, by having a temperature compensated $V_{\rm REF}$, such that transistor M_4 is biased at the ZTC operating point ($V_{\rm REF} = V_{\rm ZTC}$), a temperature-independent $I_{\rm REF}$ is produced. In the next section, the circuit employed to generate $V_{\rm REF}$ is presented.

III. Proposed Current Reference Circuit

A. Temperature Compensated Voltage Reference Circuit

The basic principle of temperature compensation used for this circuit relies on the sum of two currents, one proportional to the absolute temperature $(I_{\rm PTAT})$ and one conversely proportional to the absolute temperature $(I_{\rm CTAT})$. This principle is similar to the one previously employed in other circuits [1], [5], [8], [9], except that here, a different way to generate the current $I_{\rm CTAT}$ has been implemented. The circuit in Fig. 3 depicts this temperature compensation principle. Using basic calculations, the proper resistor ratio, R_1/R_2, is calculated in order to obtain the drain current of transistors M_1 and M_2, $I_{D1} = I_{D2} = I_{\rm PTAT} + I_{\rm CTAT}$, independent of the temperature. To produce the current $I_{\rm PTAT}$, the circuit requires that node A and B stay at the same voltage. In conventional voltage reference circuits, this requirement is fulfilled with an OA having its input directly connected to nodes A and B. However, in sub-1 V architecture, a problem arises as the input common-mode range of the amplifier must reach 850 mV—the forward biased base-emitter voltage of a bipolar transistor at -40°C [2]. Two solutions have been proposed which do not require native MOS transistors. One of them

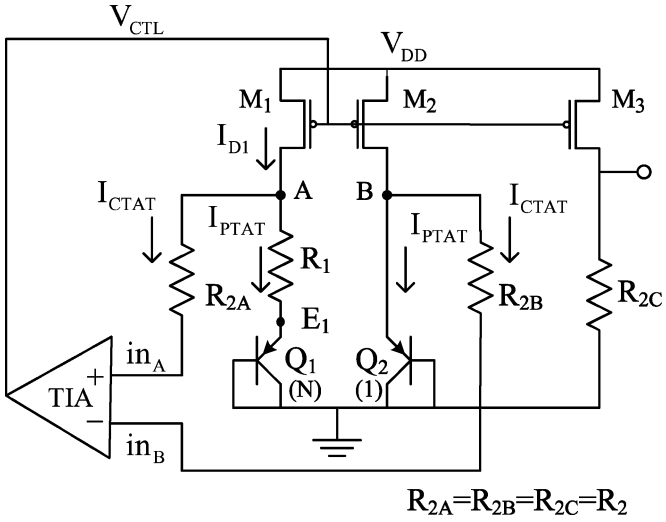

Fig. 3. Schematic diagram of proposed voltage reference generator.

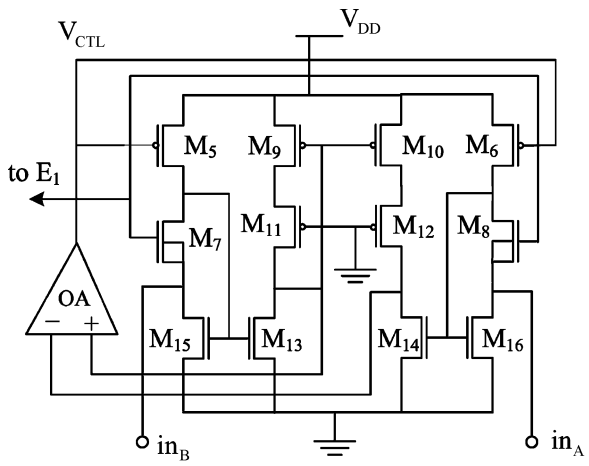

Fig. 4. Schematic diagram of the TIA.

uses a resistor divider on the I_{CTAT} branch [8]. This solution, however, requires that dc level shifts be provided by bipolar transistors in order to increase the amplifier common-mode input range. The other solution that has inspired the circuit topology of this work is detailed in Fig. 3. It consists of a transimpedance differential amplifier (TIA) that forces the same current in the two I_{CTAT} branches, thus keeping nodes A and B at the same voltage. This scheme is inevitably strongly dependent on the temperature variation of the biasing voltages $V_{\mathrm{in}A}$ and $V_{\mathrm{in}B}$ at the input nodes in_A and in_B of the TIA. In [9] the authors present a way to eliminate the effect of $V_{\mathrm{in}A}$ and $V_{\mathrm{in}B}$ on the temperature compensated output voltage. However, in the proposed circuit, two major modifications have been made so that voltages $V_{\mathrm{in}A}$ and $V_{\mathrm{in}B}$ become part of the temperature compensation scheme. First, gates of the TIA's input transistors M_7 and M_8 (Fig. 4) are connected to the emitter node E_1 of the bipolar transistor Q_1. The current I_{CTAT} flowing from the drain of M_2 to the source of M_7 is then equal to

$$I_{\mathrm{CTAT}} = \frac{V_{EB2} - V_{\mathrm{in}B}}{R_2} = \frac{V_{EB2} - (V_{SG7} + V_{EB1})}{R_2}. \quad (8)$$

The circuit of the TIA employs wide-swing current mirrors in order to ensure sub-1 V operating voltages, as shown in Fig. 4. The second modification consists of connecting the TIA's output voltage V_{CTL} to the gate of transistors M_5 and M_6 of the TIA. In this case, since V_{CTL} controls the temperature compensated drain currents of M_1, M_2 and M_3, biasing currents of the input branches of the TIA, set by M_5 and M_6, are also temperature compensated. Transistors M_7 and M_8 have their bulk connected to the source in order to eliminate the body effect and are composed of four transistors M_4 in parallel. In these conditions, M_7 and M_8 have their threshold voltages $V_{\mathrm{TH7}}(T)$ and $V_{\mathrm{TH8}}(T)$ equal to $V_{\mathrm{TH4}}(T)$.

The temperature-dependent relationship of V_{GS7} can be determined by inserting (3) and (4) in (1) and replacing $V_{\mathrm{TH4}}(T)$, V_{REF}, I_{REF}, and $W_4 \backslash L_4$ by $V_{\mathrm{TH7}}(T)$, V_{GS7}, I_{D7} and $W_7 \backslash L_7$, respectively

$$V_{GS7}(T) = V_{\mathrm{TH7}}(T_0) - \alpha_{VT}T_0 + \alpha_{VT}T + \left(\frac{2I_{D7}}{\mu_n(T_0)[T/T_0]^{\alpha_\mu}C_{\mathrm{ox}}(W_7/L_7)}\right)^{1/2}. \quad (9)$$

Since the same temperature-independent current flows through M_5 and M_7, the current I_{D7} remains constant regardless of the temperature. By expressing V_{EB1} and V_{EB2} in terms of current and replacing V_{SG7} by (9), (8) becomes

$$I_{\mathrm{CTAT}} = \frac{1}{R_2}\left[\frac{kT}{q}\ln(N) + T \times \left(\alpha_{VT} + \left[\frac{2I_{D7}}{\mu_n(T_0)T_0^2C_{\mathrm{ox}}(W_7/L_7)}\right]^{1/2}\right)\right] + \frac{(V_{\mathrm{TH7}}(T_0) - \alpha_{VT}T_0)}{R_2} \quad (10)$$

where q is the charge of the electron, k the Boltzmann constant, N the ratio of Q_1 and Q_2 emitter areas, and α_μ is equal to -2. It appears from (10) that a current conversely proportional to temperature can be obtained by selecting I_{D7} low enough so that the negative constant, α_{VT}, becomes the dominant term. Obviously, the same condition applies on I_{D8} of transistor M_8 of the other I_{CTAT} branch. Since nodes A and B are kept to the same voltage, the current I_{PTAT} is given by

$$I_{\mathrm{PTAT}} = \frac{V_{EB2} - V_{EB1}}{R_1} = \frac{kT}{qR_1}\ln(N). \quad (11)$$

As seen in Fig. 3, both current I_{CTAT} and I_{PTAT} flow out from the drain of M_1. The current I_{D1} is in turn mirrored to the drain of M_3 and flows through R_{2C} to generate the voltage reference, V_{REF}. From the addition of (10) and (11), V_{REF} can be expressed as

$$V_{\mathrm{REF}} = \left(\frac{R_2}{R_1} + 1\right)\frac{kT}{q}\ln(N) + T\left(\alpha_{VT} + \left[\frac{2I_{D7}}{\mu_n(T_0)T_0^2C_{\mathrm{ox}}(W_7/L_7)}\right]^{1/2}\right) + V_{\mathrm{TH7}}(T_0) - \alpha_{VT}T_0. \quad (12)$$

TABLE I
DEVICE SIZES AND VALUES OF THE PROPOSED CURRENT REFERENCE

Device Type W/L(μm /μm)	M_1, M_2, M_3 PMOS (140/4)	M_5, M_6 PMOS (140/4)	M_7, M_8 NMOS (4x24/1.2)	M_9, M_{10} PMOS (12/10)	M_{11}, M_{12} PMOS (12/8)	M_{13}, M_{14} NMOS (8/8)	M_{15}, M_{16} NMOS (144/16)
Device Type W/L(μm /μm)	M_{17}, M_{18} PMOS (6/4)	M_{19},M_{20} PMOS (24/4)	M_{21},M_{22} NMOS (8/4)	M_{23}, M_{24} PMOS (48/8)	M_{25}, M_{26} PMOS (24/8)	M_{27}, M_{28} NMOS (24/8)	M_{29} PMOS (60/16)
Device Type (Size\Value)	M_4 NMOS (24/1.2)	Q_1, Q_2 PNP [10x (5μm x 5μm), (5μm x 5μm)]			R_1, R_2, R_3, R_4 N-diffused resistors [(20K), (70K), (70K), (20K)]		

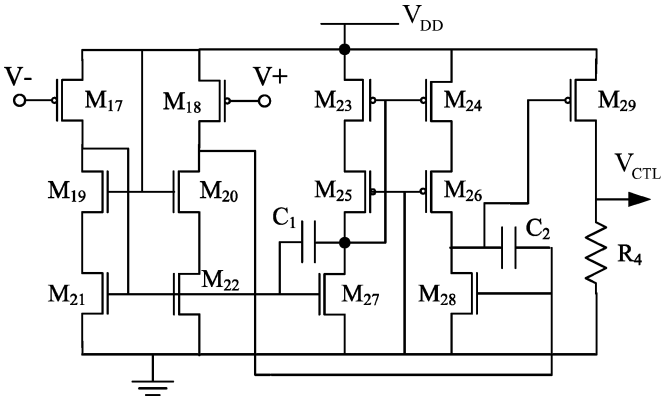

Fig. 5. Schematic diagram of the OA.

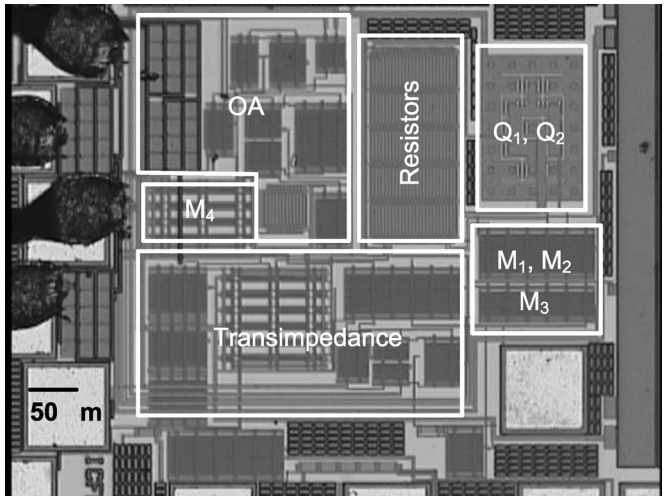

Fig. 6. Micrograph of the current reference.

Thus, for a ratio R_2/R_1 of

$$\frac{R_2}{R_1} = -\frac{q}{k\ln(N)}\left(\alpha_{VT} + \left[\frac{2I_{D7}}{\mu_n(T_0)T_0^2 C_{\rm ox}(W_7/L_7)}\right]^{1/2}\right) - 1 \tag{13}$$

the temperature dependence of $V_{\rm REF}$ is removed

$$V_{\rm REF} = V_{\rm ZTC} = V_{\rm TH7}(T_0) - \alpha_{VT}T_0. \tag{14}$$

The result of (14) corresponds to the $V_{\rm ZTC}$ voltage of transistor M_4 (6) since $V_{\rm TH7}(T_0)$ is equal to $V_{\rm TH4}(T_0)$. Therefore, by applying $V_{\rm REF}$ to the gate of transistor M_4 of Fig. 1, a temperature compensated current source is obtained. Well matched transistor layouts of M_4, M_7 and M_8 will produce correlated variations of $V_{\rm TH7}(T_0)$, $V_{\rm TH8}(T_0)$ and $V_{\rm TH4}(T_0)$ which will minimize shifts in $I_{\rm REF}$ due to process variations, as explained in Section II-A. Moreover, good matching of M_7 and M_8 reduces the input offset current of the TIA. Table I gives the sizes and values of the components used for the fabrication of the current reference.

B. Circuit Layout

The circuit of the OA of Fig. 4 is shown in Fig. 5. It provides an additional voltage gain to increase the overall transimpedance gain of the TIA. The circuit topology is similar to the one employed in [9] as an intermediate voltage amplifier. Capacitors C_1 and C_2 were adjusted externally in order to introduce a pole for eliminating the closed loop instability.

A micrograph of the circuit is shown in Fig. 6. A test pad was provided to access the gate of the output transistor M_4 in order to measure the variation of $V_{\rm REF}$ as a function of the temperature and to evaluate accurately the operating point $(I_{\rm ZTC}, V_{\rm ZTC})$ of M_4 by performing dc voltage sweeps on its gate at different temperatures. The chip has been fabricated in a 0.18-μm standard CMOS process and consumes approximately 83 μA, excluding the reference current sunk by transistor M_4.

IV. EXPERIMENTAL RESULTS

A. $I_{\rm ZTC}$ and $V_{\rm ZTC}$ Measurements

The ZTC operating point of transistor M_4 was measured for twenty samples. A sweep of the gate–source voltage was done for three temperatures namely 25°C, 50°C, and 100 °C from which the common intersection point $(I_{\rm ZTC}, V_{\rm ZTC})$, as shown in Fig. 2, was extracted. Measurements of the threshold voltage of M_4 were also performed for each sample according to the method described in [10]. Plots of correlation were used to compare the parameters. In Fig. 7(a), the plot of $V_{\rm TH}$ versus $I_{\rm ZTC}$ shows no correlation between these parameters, as it is expected for a transistor operating at the ZTC operating point according to (7). However, in Fig. 7(b), a positive correlation is obtained from the plot of $V_{\rm TH}$ versus $V_{\rm ZTC}$. This result is in agreement with the process compensation scheme presented in Section II-A where correlated shifts of $V_{\rm REF} = V_{\rm ZTC}$ and $V_{\rm TH}$ are needed to reduce

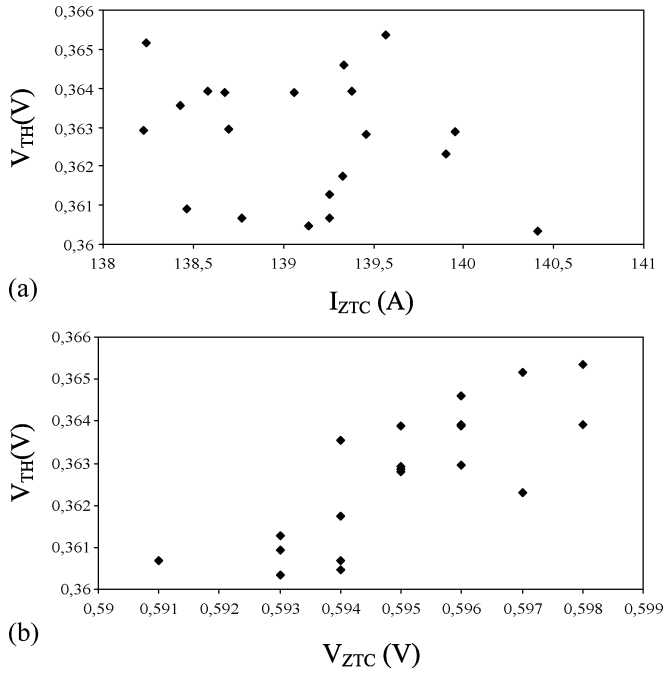

Fig. 7. Correlation plots obtained from measurements on transistor M_4 of the ZTC operating point and threshold voltage, $V_{\rm TH}$, from twenty samples. (a) $V_{\rm TH}$ versus $I_{\rm ZTC}$. (b) $V_{\rm TH}$ versus $V_{\rm ZTC}$.

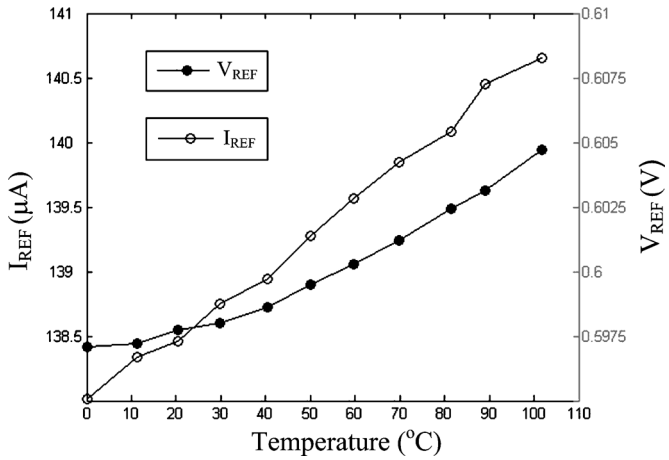

Fig. 8. Measured temperature dependence of $V_{\rm REF}$ and $I_{\rm REF}$.

the sensitivity of $I_{\rm REF}$ to process parameter variations. Therefore, it appears that the ZTC operating point is a good candidate for process compensated current references. From these measurements, an average current $I_{\rm ZTC}$ of 139.1 μA and an average voltage $V_{\rm ZTC}$ of 595 mV were obtained with variations of 1.6% and 1.2%, respectively.

B. $I_{\rm REF}$ and $V_{\rm REF}$ Variations

TC measurements were performed by sweeping each sample from 0 to 100 °C. Values of $I_{\rm REF}$ and $V_{\rm REF}$ were recorded every 10 °C. A total of nineteen samples were measured. A typical temperature plot is shown in Fig. 8. From these results, temperature variation coefficients of 185 $\rm ppm/°C$ for $I_{\rm REF}$ and 125$\rm ppm/°C$ for $V_{\rm REF}$ were calculated.

Histograms of the distribution of $I_{\rm REF}$ and $V_{\rm REF}$ obtained from the nineteen samples at three temperatures: 0, 50 and 100 °C were realized in order to evaluate the combined effect of process and temperature variations. Fig. 9(a) shows the maximum dispersion of $I_{\rm REF}$, being $\pm$7%, which leads to a maximum variation of $\pm$10.1 μA for an average value of 144.3 μA. At the same time, Fig. 9(b) indicates a maximum dispersion on $V_{\rm REF}$ of $\pm$2%, which represents a maximum variation of $\pm$12.2 mV for an average value of 610.9 mV. Comparing the measured ranges of $V_{\rm ZTC}$ [595 mV $\pm$ 3 mV] and $V_{\rm REF}$ [610.9 mV $\pm$ 12.2 mV] it is clear that for the nineteen samples the output current transistor M_4 is not biased exactly at the ZTC operating point. The larger variation observed on $I_{\rm REF}$ [144.3 μA $\pm$ 10.1 μA] compared to the one of $I_{\rm ZTC}$ [139.1 μA $\pm$ 2.2 μA] is partly due to the voltage $V_{\rm REF}$ not being close enough to the corresponding $V_{\rm ZTC}$ value of M_4. As stated in Section II, the proposed process compensation scheme relies on good matching of transistors M_7, M_8 and M_4 to insure that $V_{\rm REF}$ approaches $V_{\rm ZTC}$. Layouts of M_7, M_8 were done in that respect; with the limitation that M_4 was not interdigitated with M_7, M_8 for purpose of noise immunity. The measured power-supply rejection ratio (PSRR) at the $V_{\rm REF}$ node is $-$27.5 dB at 10 kHz and $-$22.8 dB at 10 MHz. Table II compares the TC and the combined effect of TC and process variation coefficient (PC) for the circuit proposed in this work with other current references recently published.

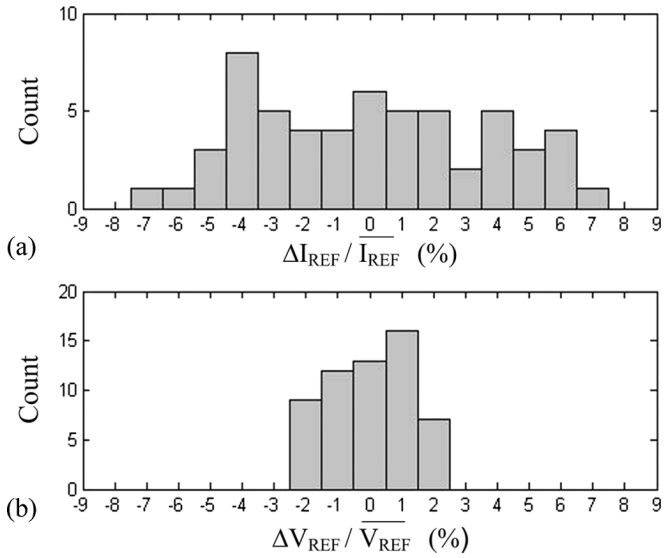

Fig. 9. Distributions obtained from the measurement of nineteen samples at three temperatures (0, 50 and 100 °C) for (a) $I_{\rm REF}$ and (b) $V_{\rm REF}$.

V. Conclusion

A simple process compensation scheme for current references was described. It takes advantage of the reduced variation of the drain current, due to process parameter changes, of a MOS transistor operating at the ZTC point $(I_{\rm ZTC}, V_{\rm ZTC})$. A circuit was proposed to generate a reference voltage equals to $V_{\rm ZTC}$ as the gate biasing voltage of the output transistor employed as the current generator. This circuit uses a transimpedance amplifier in the feedback loop in order to operate at a supply voltage of 1 V or below. The circuit has been fabricated in a CMOS 0.18-μm standard process. Experimental results showed a variation of $\pm$7% on the output current caused

TABLE II
COMPARISON OF CMOS CURRENT REFERENCES

Ref. Year	Technology	V_{DD} (V)	I_{REF} (A)	Temperature range (°C)	TC (ppm)	TC & PC (%)	Number of measured samples
[2] 2002	CMOS 0.25 µm using native transistors	1.5	5 µ	-40 to 150	368	N/A	N/A
[5] 2003	CMOS 0.18 µm	1	528 µ	0 to 110	50	N/A	N/A
[3] 2003	CMOS 2µm SIMOX using p-i-n diode	10	19 µ	-15 to 90	12	± 5	30 from 2 wafers
[6] 2003	CMOS 0.15 µm	1	90 µ	40 to 110	257	± 5	148 from 2 wafers
[4] 2005	CMOS 1.5 µm	1.1	410 p	-20 to 70	3 700	± 10	10
This work	CMOS 0.18 µm	1	144 µ	0 to 100	185	± 7	19

by the combined effect of temperature and process, while the ZTC current was measured separately and presented a variation of $\pm 1.6\%$ due to process only. The discrepancy between those results reflects the difficulty to generate a voltage reference that precisely equals to the V_{ZTC} of the output transistor. Better matching of key transistors M_7, M_8, and M_4 could reduce the variation observed on I_{REF}. It is our belief that trimming might be required to adjust the ratio of R_2/R_1 such that V_{REF} could attain precisely the ZTC operating point of the output transistor. In the past, advantages of trimming techniques have already been exploited in bandgap voltage references [8].

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