A Precision Low-TC Wide-Range CMOS Current Reference

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***Abstract*—This paper describes a programmable temperature-compensated CMOS current reference. The proposed circuit achieves a first-order temperature compensation by canceling the negative temperature coefficient (TC) of an on-chip poly resistor with the positive TC of a MOS transistor operating in the ohmic region. Programmability of the current reference is enabled with the use of floating-gate transistors, thus allowing arbitrary current values to be set accurately. The temperature compensation is independent of the reference value; a low TC reference is possible for a wide range of currents. Prototypes from a 0.5 μm CMOS process exhibited a maximum temperature coefficient of 132 ppm/°C for a temperature range of 0 °C to 80 °C. Experimental results showed a current precision of 0.02% along with a line regulation of 1%/V for a supply voltage of 2.3 V to 3.3 V. These results were obtained for current references of 16 μA to 53 μA for five different prototypes.**

***Index Terms*—Charge, current reference, floating gate, programmable, temperature coefficient.**

I. Introduction

A CURRENT reference is an essential circuit on any analog and mixed-signal system, as is used to establish the quiescent condition for many different circuits such as oscillators, amplifiers, and phase-locked loops (PLLs), among others. Many circuit topologies have been proposed to reduce the temperature coefficient (TC) [1], [2], improve the line regulation [3], and increase the precision [4], [5] of current references. Most of the published work has focused on minimizing their temperature dependence.

Temperature compensation of a current reference is a difficult task; typical approaches rely on specific device parameters values for proper performance. Optimal compensation is difficult to obtain since parameter values cannot be predicted accurately due to random variation across process, dies, and runs. Also, the current reference value is typically dictated by the compensation method; temperature compensation is only obtained for a single, non-arbitrary current value.

Some of the proposed architectures [1], [3] use a variation of the bandgap voltage reference circuit to obtain a low-TC current reference. These approaches take advantage of the opposite TC and the linear temperature dependence of $\Delta V_{\rm be}$ and $V_{\rm be}$. Others [4], [6], [7] exploit the temperature dependence of the MOS transistor parameters $V_{\rm th}$ and μ. A temperature coefficient of 4 ppm/°C was obtained in [8] with the use of a bipolar process. All CMOS current [1], [5] have reported experimental results in the range of 50 ppm/°C–400 ppm/°C for first-order temperature compensation. With use of the second-order compensation techniques, temperature coefficients in the 10's ppm/°C are possible; no experimental data have been reported.

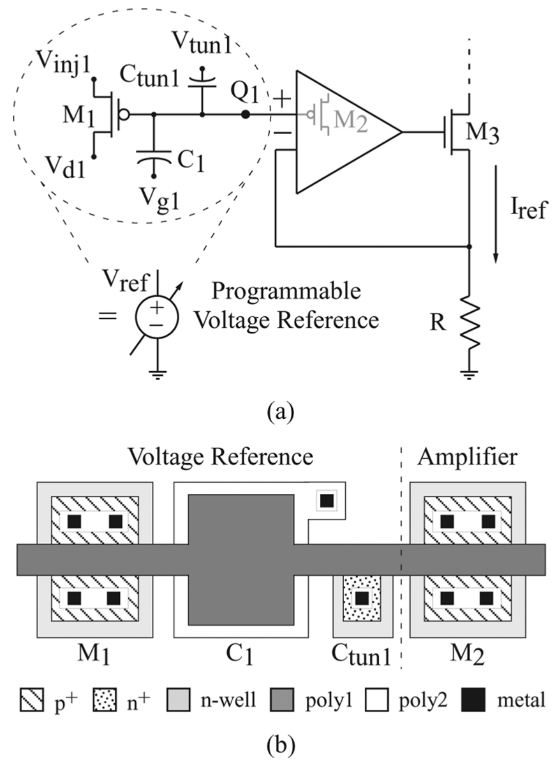

Fig. 1. Proposed programmable current reference. (a) Schematic diagram of the proposed current reference. (b) Layout diagram of the programmable voltage reference composed of M_1, M_2, C_1, and $C_{\rm tun_1}$.

The use of programmable transistors, when building a current source, has been shown only in [9] and [10]. In [9], temperature compensation is achieved by programming currents with opposite TCs; experimental results showed a 2% variation over a limited range of 45 °C to 75 °C. In [10], a programmable current source is introduced briefly without any temperature compensation.

This paper describes a programmable temperature-compensated current reference. The proposed circuit achieves a first-order temperature compensation by canceling the negative TC of an on-chip poly resistor with the positive TC of a MOS transistor operating in the ohmic region. Flexibility and immunity to device parameters is enabled through the use of floating-gate

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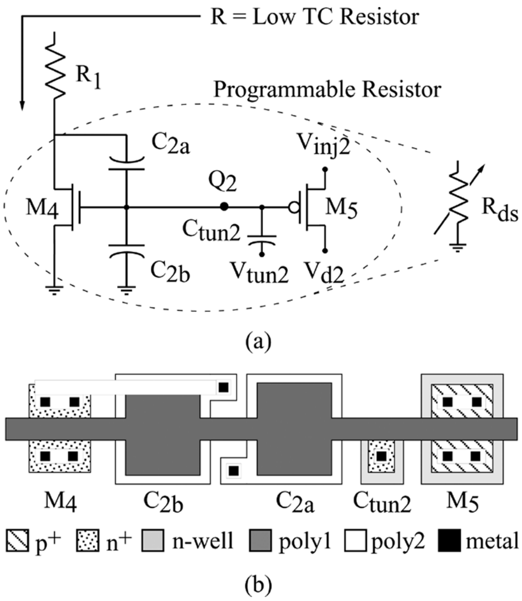


Fig. 2. Proposed temperature-compensated resistor. (a) Circuit schematic of the proposed resistor. (b) Layout diagram of the ohmic resistor composed of M_4, M_5, C_{tun_2}, C_{2_a}, and C_{2_b}.

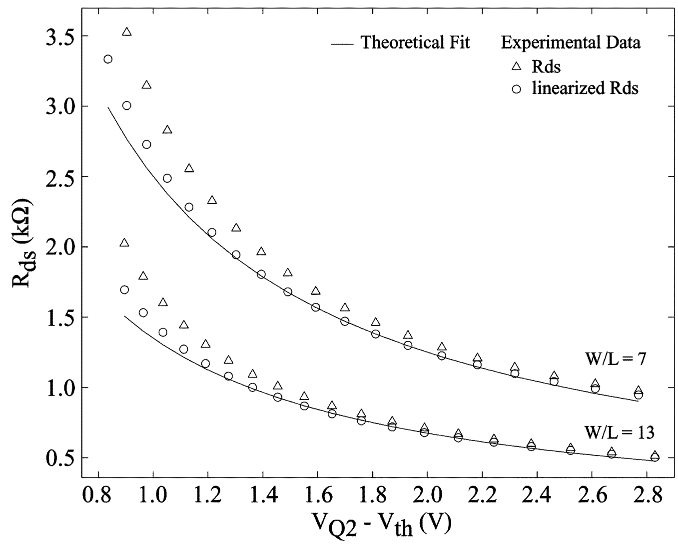


Fig. 3. Plot of the ohmic resistance for different $V_{Q_2} - V_{\mathrm{th}_n}$ values.

transistors. Programmability of the ohmic resistor allows compensation of parameter variations, while programmability of the reference voltage allows for an accurate current reference for a wide range of values.

II. Programmable Current Reference

A voltage reference circuit, composed of $M_1, M_2, C_{\mathrm{tun}_1}$, and C_1, is encircled in Fig. 1(a). Assuming M_1 is off (all terminals grounded), and $C_1 \gg C_{\mathrm{tun}_1}, C_{\mathrm{par}}$, where C_{par} is the parasitic capacitance, the voltage reference will be given by

$$V_{\mathrm{ref}} = \frac{Q_1}{C_1} \tag{1}$$

where Q_1 is the charge stored on C_1, a poly–poly capacitor.

Fig. 1(b) shows the layout diagram of the programmable voltage reference. The reference voltage is connected to the input transistor of the amplifier with a poly line; transistors M_1 and M_2 share the gate terminal. Inputs to this terminal are capacitively coupled through C_1 and C_{tun_1}, thus creating a floating node [see Fig. 1(a)]. The voltage V_{ref} can be set arbitrarily by modifying Q_1 with M_1 [11] as seen in (1). Modification of the charge on a floating node is discussed in Section V.

Fig. 1(a) shows the circuit diagram of the proposed programmable current reference. The current reference consists of a programmable voltage reference (discussed above), a resistor, and an amplifier. Assuming the amplifier has infinite gain, the voltage across the resistor R will be forced to V_{ref}, resulting in

$$I_{\mathrm{ref}} = \frac{Q_1}{C_1}\frac{1}{R}. \tag{2}$$

An arbitrary I_{ref} value can be obtained after fabrication by modifying Q_1 as seen in (2).

The temperature coefficient of I_{ref}, $\mathrm{TC}_{I_{\mathrm{ref}}} = (1/I_{\mathrm{ref}})\cdot(\delta I_{\mathrm{ref}}/\delta T)$, is given by

$$\mathrm{TC}_{I_{\mathrm{ref}}} = -\frac{1}{R}\frac{\delta R}{\delta T} - \frac{1}{C_1}\frac{\delta C_1}{\delta T} \tag{3}$$

$$\approx -\frac{1}{R}\frac{\delta R}{\delta T} \tag{4}$$

where $(1/R)(\delta R/\delta T)$ and $(1/C_1)(\delta C_1/\delta T)$ are the temperature coefficients of R and C_1, respectively. The temperature dependence of I_{ref} will be dictated by R; temperature coefficients for poly–poly capacitors range from 20 ppm/°C–50 ppm/°C, thus are assumed to be negligible. The floating-gate charge Q_1 does not exhibit any temperature variations. A low-TC current reference can be obtained with a low-TC resistor as seen in (4).

III. Temperature Compensated Resistor

A low-TC resistor is obtained by canceling the negative TC of an on-chip poly resistor with the positive TC of a MOS resistor. Resistance characteristics and temperature behavior of the ohmic resistor are examined next, followed by a detailed discussion of the proposed low-TC resistor.

A. Programmable Resistor

The ohmic resistor circuit is composed of M_4, M_5, C_{tun_2}, C_{2_a}, and C_{2_b}, as shown encircled in Fig. 2(a). Transistor M_4, along with capacitors C_{2_a} and C_{2_b}, form a linearized resistor [12]. Fig. 2(b) shows the layout diagram of the ohmic resistor. The gate terminals of M_4 and M_5 share a poly1 connection; inputs to this terminal are capacitively coupled through C_{2a}, C_{2b}, and C_{tun_2}, thus creating a floating node [see Fig. 2(a)]. Charge on this floating node can be set arbitrarily by modifying Q_2 via M_5 [11]. Modification of the charge on a floating node is discussed in Section V. Assuming there is a charge Q_2 stored in the floating node, M_4 operates in the ohmic region,[1] and M_5

[1]The equations derived in this section assume that M_4 operates in the strong inversion region; a similar analysis can be done for M_4 operating in the weak inversion region.

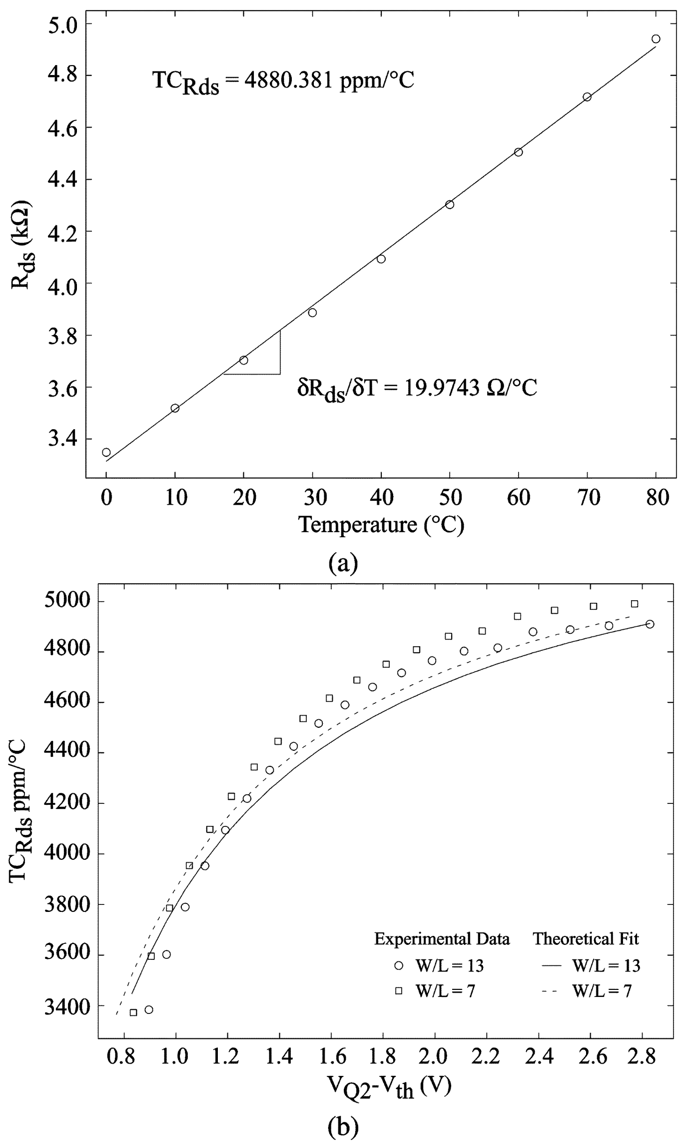


Fig. 4. $R_{\rm ds}$ Temperature behavior. (a) Plot of the ohmic resistance for a temperature range of $-60\,^{\circ}$C to $140\,^{\circ}$C. (b) Plot of $R_{\rm ds}$ temperature coefficient for different $V_{Q_2} - V_{{\rm th}_n}$ values.

is off (all terminals grounded), the ohmic resistance $R_{\rm ds}$ can be approximated as

$$R_{\rm ds} \approx \frac{1}{\frac{W}{L}\mu_n C_{\rm ox}\left(V_{Q_2} - V_{{\rm th}_n}\right)} \approx \frac{1}{K_n\left(V_{Q_2} - V_{{\rm th}_n}\right)} \tag{5}$$

where μ_n is the mobility of charge carriers, $C_{\rm ox}$ is the oxide capacitance, W and L are M_4 dimensions, $V_{Q_2} = Q_2/C_2$ is the voltage due to Q_2, $V_{{\rm th}_n}$ is the threshold voltage, and $K_n = (W/L)\mu_n C_{\rm ox}$. It can be seen from (5) that $R_{\rm ds}$ can be modified with V_{Q_2} to any arbitrary value, after fabrication.

The temperature sensitivity, $\delta R_{\rm ds}/\delta T$, and first-order temperature coefficient, ${\rm TC}_{R_{\rm ds}} = (1/R_{\rm ds})(\delta R_{\rm ds}/\delta T)$, of $R_{\rm ds}$ can be shown to be

$$\frac{\delta R_{\rm ds}}{\delta T} = \left[-\frac{1}{\mu_n}\frac{\delta \mu_n}{\delta T} + \frac{1}{V_{Q_2} - V_{{\rm th}_n}}\frac{\delta V_{{\rm th}_n}}{\delta T}\right] \cdot \left[\frac{1}{K_n\left(V_{Q_2} - V_{{\rm th}_n}\right)}\right] \tag{6}$$

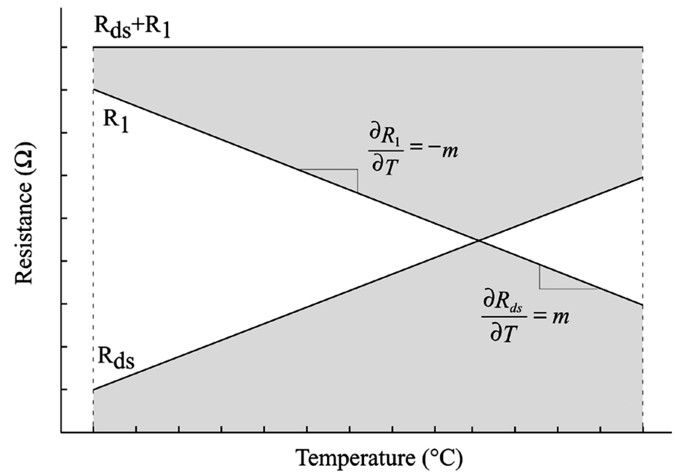


Fig. 5. Graphical representation of the linear cancellation of the resistor temperature sensitivity.

and

$$\begin{aligned}{\rm TC}_{R_{\rm ds}} &= -\frac{1}{\mu_n}\frac{\delta \mu_n}{\delta T} + \frac{1}{V_{Q_2} - V_{{\rm th}_n}}\frac{\delta V_{{\rm th}_n}}{\delta T} && (7)\\ &= \frac{n}{T} - \frac{\alpha}{V_{Q_2} - V_{{\rm th}_n}} && (8)\end{aligned}$$

respectively, where T is the temperature, n is the mobility temperature coefficient, and α is the threshold voltage temperature sensitivity. The temperature behavior of $R_{\rm ds}$ can be modified with V_{Q_2} as seen in (6) and (8). For large enough V_{Q_2} values ($V_{Q_2} > (T\cdot\alpha/n) + V_{{\rm th}_n}$), a positive ${\rm TC}_{R_{\rm ds}}$ is obtained.

Fig. 3 shows experimental data, along with theoretical fit, of $R_{\rm ds}$ for different $V_{Q_2} - V_{{\rm th}_n}$ values. As expected, the linearized version [12] of $R_{\rm ds}$ follows closely the behavior predicted by (5). Fig. 4(a) shows the temperature behavior of $R_{\rm ds}$ over a temperature range of $-60\,^{\circ}$C to $140\,^{\circ}$C. The ohmic resistor exhibits a strong linear dependence with temperature; higher order temperature effects are due to mobility. A temperature coefficient of $+4880$ ppm/$^{\circ}$C was obtained for a $V_{Q_2} - V_{{\rm th}_n}$ value of 1.8 V. Values of -1.65 and -1.6 mV/$^{\circ}$C were extracted for device parameters n and α, respectively. The temperature coefficient of $R_{\rm ds}$ for different $V_{Q_2} - V_{{\rm th}_n}$ values is shown in Fig. 4(b). The experimental data follows closely the theoretical behavior predicted by (8). A small difference between the temperature coefficient behavior of different sized $R_{\rm ds}$ arises from device parameter mismatch. Arbitrary ${\rm TC}_{R_{\rm ds}}$ values are possible by modifying V_{Q_2} as seen in Fig. 4(b).

B. Low-TC Resistor

Fig. 2(a) shows the schematic diagram of the proposed resistor R. The resistor is a series combination of R_1, a high poly resistor, and $R_{\rm ds}$, a MOS transistor (M_4) operating in the ohmic region (see Section III-A).

Using (5), R can be written as

$$\begin{aligned}R &= R_1 + R_{\rm ds} && (9)\\ &= R_1 + \frac{1}{K_n\left(V_{Q_2} - V_{{\rm th}_n}\right)} && (10)\end{aligned}$$

where all the variables have their usual meaning.

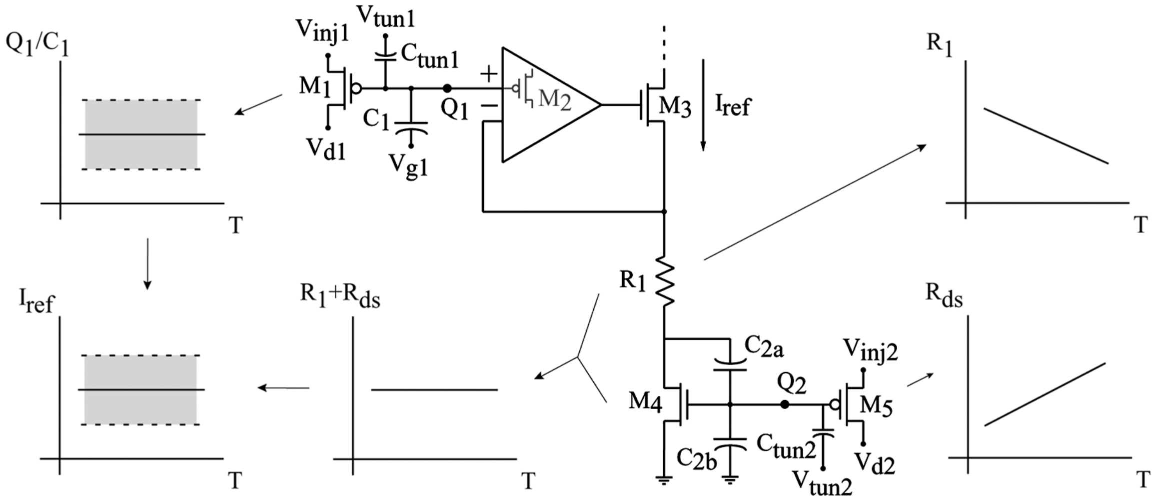


Fig. 6. Simplified schematic diagram of the proposed current reference, with a graphical representation of the temperature behavior of the different components.

A first-order temperature variation of R, obtained by differentiating (10) against temperature, is given by

$$\frac{\delta R}{\delta T} = \frac{\delta R_1}{\delta T} + \frac{\delta R_{\rm ds}}{\delta T} \tag{11}$$

$$= R_1 \cdot {\rm TC}_{R_1} + R_{\rm ds} \cdot {\rm TC}_{R_{\rm ds}} \tag{12}$$

where ${\rm TC}_{R_1} = (1/R_1)(\delta R_1/\delta T)$ is the temperature coefficient of R_1. Temperature sensitivity cancellation ($\delta R/\delta T = 0$) can be achieved by satisfying

$$\frac{\delta R_1}{\delta T} = -\frac{\delta R_{\rm ds}}{\delta T} \tag{13}$$

or

$$\frac{R_1}{R_{\rm ds}} = -\frac{{\rm TC}_{R_{\rm ds}}}{{\rm TC}_{R_1}}. \tag{14}$$

Temperature sensitivity cancellation is possible for resistors with opposite temperature behavior as seen in (13). Fig. 5 shows a graphical representation of the proposed approach. Linear cancellation of the positive temperature sensitivity of $R_{\rm ds}$ is possible with a resistor with negative temperature sensitivity.

Substituting (5) and (8) into (14), the TC cancellation can be achieved by properly sizing R_1 and M_4 according to

$$R_1 K_n (V_{Q_2} - V_{{\rm th}_n}) = \left[\frac{n}{T} - \frac{\alpha}{V_{Q_2} - V_{{\rm th}_n}}\right] \cdot \left[\frac{1}{{\rm TC}_{R_1}}\right]. \tag{15}$$

Optimal TC cancellation can be obtained by modifying V_{Q_2} as seen in (15). Immunity to device parameters R_1, K_n, and $V_{{\rm th}_n}$ can be obtained by programming V_{Q_2} to satisfy (15) for nominal values of n, α, and ${\rm TC}_{R_1}$. This is done by monitoring the voltage across $R_{\rm ds}$ during the temperature compensation process. For batch fabrication, the optimal TC cancellation will be degraded due to variations of n, α, and ${\rm TC}_{R_1}$. Variations of these parameters exhibit a lower spread compared to variations of R_1, K_n, and $V_{{\rm th}_n}$.

IV. Proposed Current Reference

Fig. 6 shows the simplified circuit diagram of the proposed current reference. A temperature-insensitive programmable current reference is obtained by combining the programmable current reference circuit presented in Section II with the temperature-compensated resistor circuit presented in Section III.

The analytical expression for $I_{\rm ref}$, obtained by substituting (10) in (2), is given as

$$I_{\rm ref} = \frac{Q_1}{C_1} \cdot \left[\frac{K_n(V_{Q_2} - V_{{\rm th}_n})}{R_1 K_n (V_{Q_2} - V_{{\rm th}_n}) + 1}\right]. \tag{16}$$

The temperature dependence of $I_{\rm ref}$ will depend directly on R as shown in (4). Modification of V_{Q_2} allows for optimal TC cancellation of R in (16), as discussed in Section III-B, while modification of V_{Q_1} allows for precise programming of $I_{\rm ref}$ to any arbitrary value, as discussed in Section II. In contrast to other approaches [1]–[8], the proposed TC cancellation method is independent of $I_{\rm ref}$ due to $I_{\rm ref}$'s direct proportionality to V_{Q_1}. A pictorial representation of the temperature behavior of the different components is also shown in Fig. 6.

V. Charge Modification

Performance of the proposed current reference relies on the ability to modify the charge on a floating node. It has been shown in [13] that the charge on a floating node can be precisely programmed for target currents with 0.05% accuracy, and exhibits long-term charge retention. A charge loss of 0.001% in 10 years at 25 °C has been reported in [14].

Charge on a floating node can be removed through Fowler–Nordheim tunneling [15] and added through impact-ionized hot-electron injection [13], [16]. For a 0.5 μm CMOS process, electron tunneling is enabled by applying a high voltage (15 V) to the tunneling capacitor, while hot-electron injection occurs for high enough drain–source voltages (> 5 V). Electron tunneling is used primarily as a global erase and precision programming is achieved through hot-electron injection. This work employs on-chip charge modification with the use of a high-voltage charge pump for tunneling and a negative-voltage charge pump for injection.

Fig. 7 shows the circuit used to program the charge Q_1 of the proposed reference (refer to Fig. 6). Transistors M_1 and M_2 and capacitors C_1 and $C_{\rm tun1}$ represent the same devices

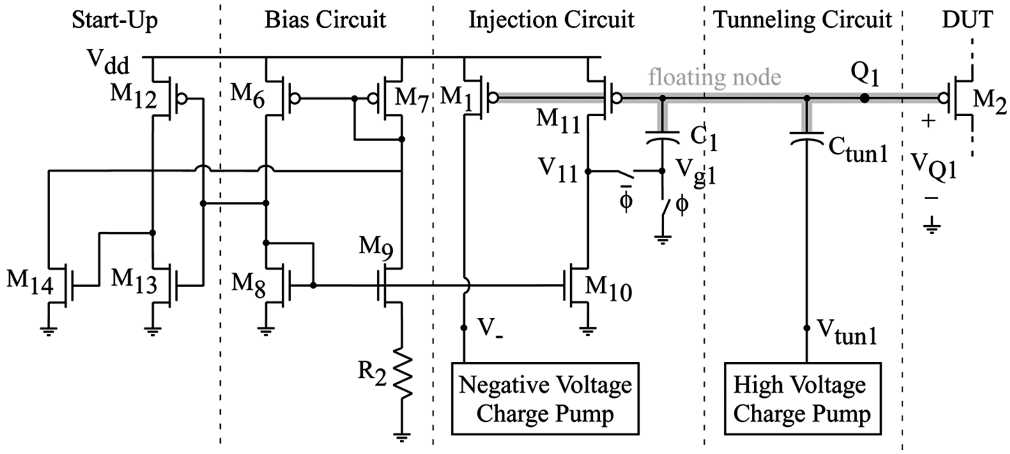


Fig. 7. Schematic diagram of the circuit used to modify the charge Q_1 (see Fig. 6) of the proposed current reference. An identical approach is used to modify Q_2.

shown in Fig. 6. The additional transistor (M_{11}), connected to the floating node, is used for constant charge injection. Transistors M_6–M_{10}, along with resistor R_2, form a bootstrap current source that bias M_{11}. Proper operation of the circuit is ensured with the start-up circuit composed by M_{12}–M_{14}. A bias current of 1 μA was used in this design, thus burning only an additional 3 μA of current. An identical approach is used to program the charge Q_2 of the proposed resistor (refer to Fig. 6) for temperature compensation.

During normal operation, $\phi = V_{\rm dd}$, charge pumps are turned off, and $V_{\rm tun_1}$ and V_- are set to gnd and $V_{\rm dd}$, respectively. This ensures there is no coupling though $C_{\rm tun_1}$ and M_1 is turned off. Transistor M_{11} will be on; its region of operation will depend on the charge Q_1 available on the floating node. The value of the floating-node voltage will be given by (1).

During programming, $\phi = gnd$, a feedback loop is established by the diode-connected transistor M_{11}. The voltage V_{11} will ensure that the current set by M_{10} flows through M_{11}, independently of Q_1. This results in a constant current through M_1 as it will mirror the current of M_{11} (see Fig. 7). For injection, a negative-voltage pulse is applied to the drain terminal of M_1 with the use of a negative charge pump. A constant charge modification will occur when injecting due to the fixed current through M_1. The change in charge will be a function of the bias current of M_1, the drain–source voltage applied to M_1, and the duration of the pulse. For tunneling, a high-voltage pulse is applied to $C_{\rm tun_1}$ with the use of a high-voltage charge pump.

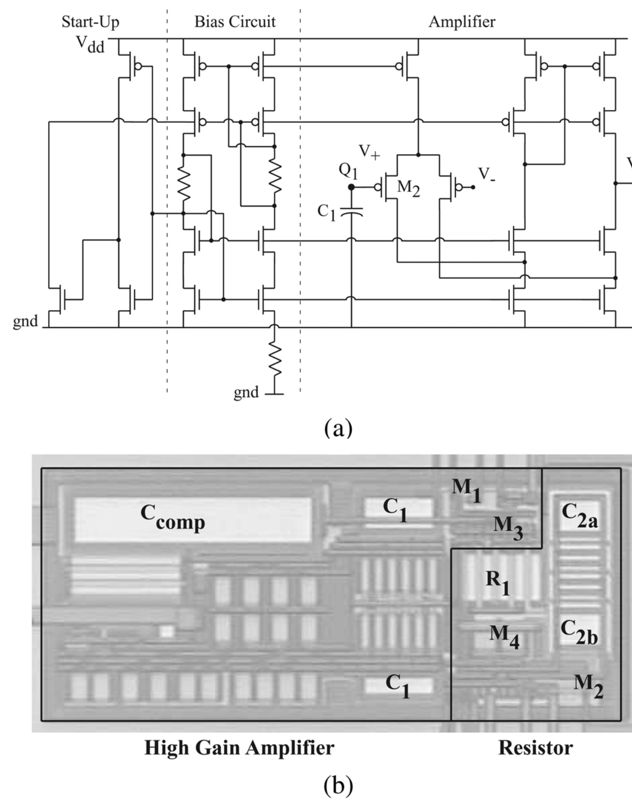


Fig. 8. Prototype. (a) Schematic diagram of the folded cascode amplifier used for the proposed current reference presented in Fig. 6. (b) Chip micrograph of the prototype current reference in a 0.5 μm CMOS process.

VI. Experimental Results

A prototype chip was fabricated in 0.5 μm CMOS process. A folded cascode topology was used to implement the high-gain amplifier. Fig. 8(a) shows the schematic diagram of the amplifier along with the start-up and the bias circuitry. The power consumption of the amplifier along with the bias circuitry was just 21 μW at a $V_{\rm dd}$ of 3.3 V. Also, the amplifier exhibits a minimum gain 65 dB for a $V_{\rm dd}$ range of 2.1 V to 3.3 V and a temperature range of 0 °C to 80 °C. Fig. 8(b) shows the die micrograph of the prototype integrated circuit (charge pumps not included); the total area of the current reference is just 200 μm × 75 μm. The charge pumps and the programming circuit occupy an additional area of 132 μm × 342 μm.

Measurements were conducted to characterize run-specific device parameters. Experimental results showed R_1 and TC_{R_1} to be 12.1 kΩ and -1750 ppm/°C respectively, which results in $\delta R_1/\delta T = -21.2\ \Omega/°\mathrm{C}$. Optimal TC compensation was carried out by measuring the temperature sensitivity of the ohmic resistor $R_{\rm ds}$ for different programmed values of V_{Q_2} as shown in Fig. 9(a). The temperature sensitivity, $\delta R_{\rm ds}/\delta T$, was found to decrease with increasing $V_{Q_2} - V_{\mathrm{th}_n}$, as expected from (6). An

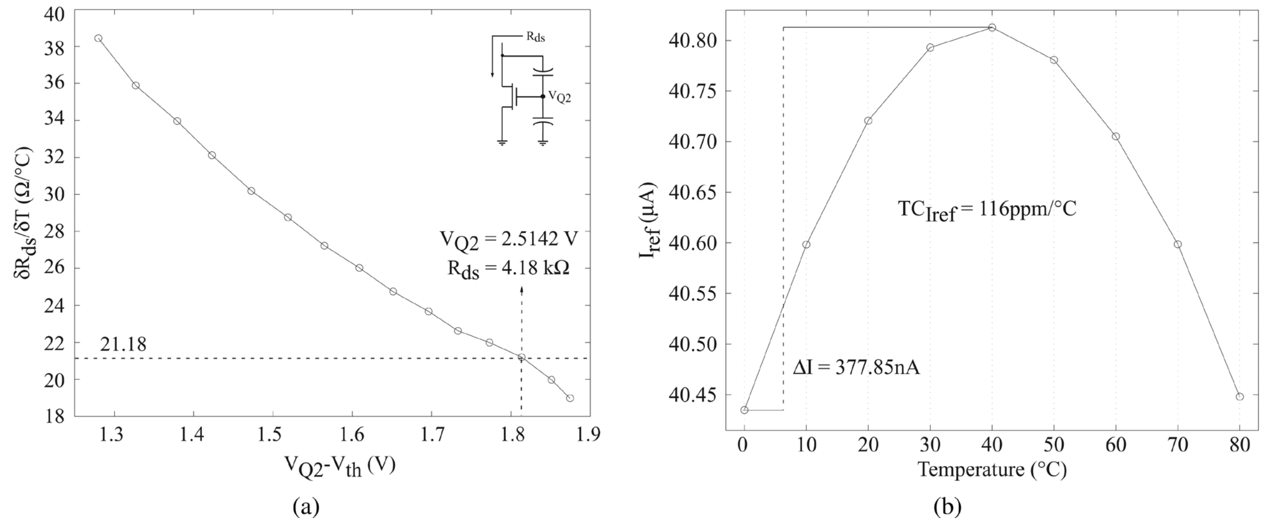


Fig. 9. Optimal TC cancellation. (a) Temperature sensitivity of the ohmic resistor as a function of the programmed voltage on the floating node. (b) Plot of the current reference against temperature for a programmed current of 40.8 μA.

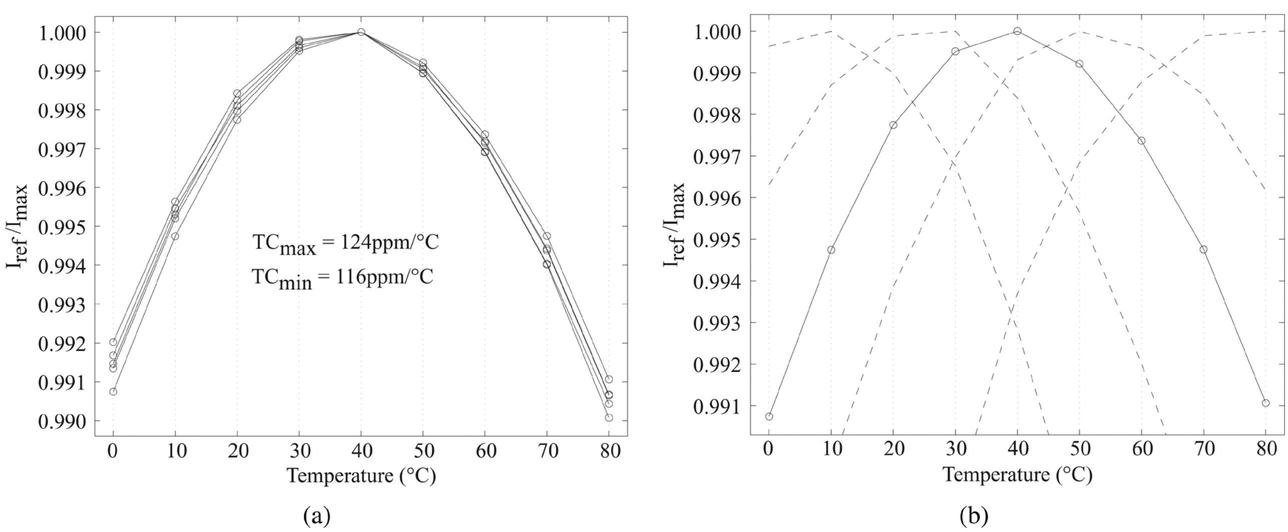


Fig. 10. Temperature sensitivity: (a) Plot of the normalized current reference, $I_{\rm ref}/I_{\rm max}$, against temperature for five different prototypes. (b) Plot of the normalized current reference against temperature for different programmed resistor values.

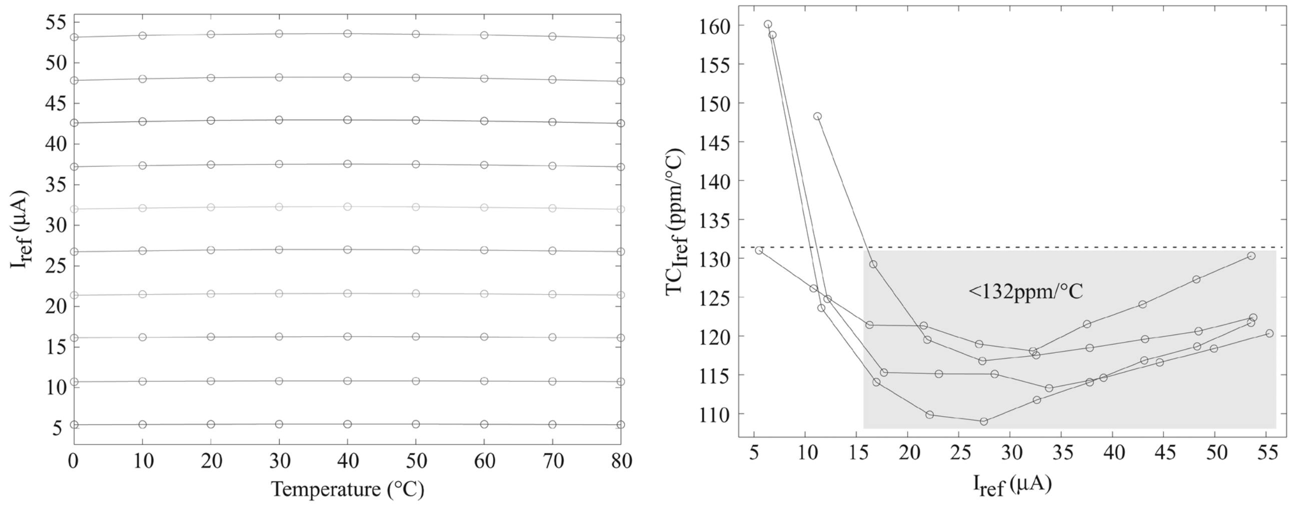
optimal V_{Q_2} of 2.51 V was extracted at a temperature of 40 °C, which corresponds to an $R_{\rm ds}$ of 4.2 kΩ.

Fig. 9(b) shows the temperature sensitivity of the proposed current reference programmed at the optimal point. The parabolic shape of the curve confirms the first-order TC cancellation; a temperature coefficient of 116 ppm/°C was obtained for a 40.78 μA reference. Although higher order temperature effects were expected due to the transistor mobility, it was found that the poly resistor introduced additional second-order terms. Simulations predict a temperature coefficient of only 50 ppm/°C for a linear temperature-dependent resistor.

Fig. 10(a) shows the current reference temperature behavior for five different prototypes from the same lot. All five chips were programmed using the optimal point extrapolated from the first device. A maximum temperature coefficient of 124 ppm/°C was obtained. Results indicated good temperature coefficient matching among chips. The direct influence of V_{Q_2} on the temperature sensitivity of the current reference can be observed in Fig. 10(b), where the normalized temperature sensitivity of a single prototype is plotted for different V_{Q_2} values.

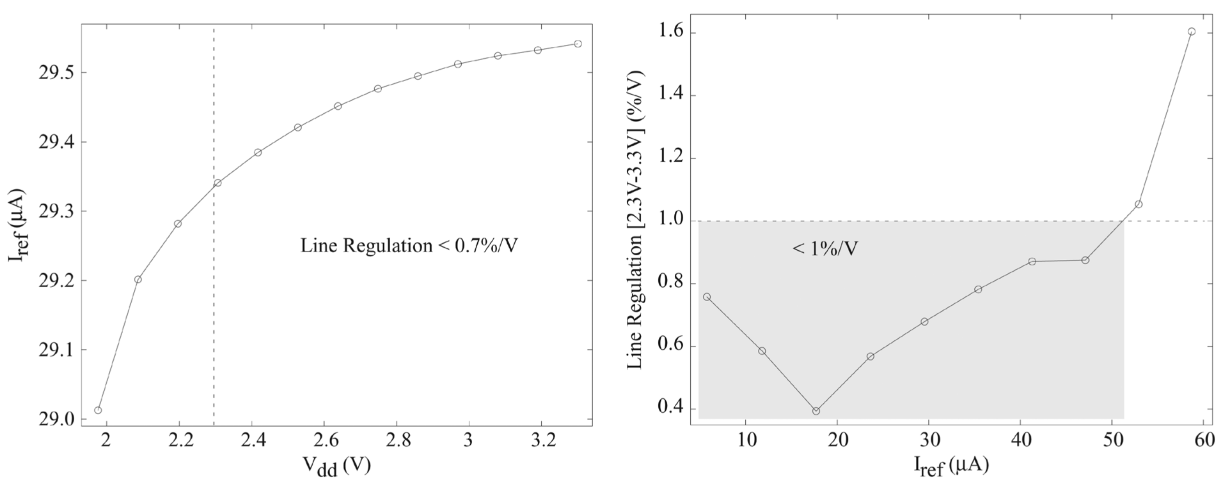
Characterization of the prototype over a wide range of currents was enabled by programming Q_1 accordingly. Temperature sensitivities for current references ranging from 5 μA to 53 μA are shown in Fig. 11(a). A maximum TC of 132 ppm/°C was measured for a current range of 16 μA to 53 μA as seen in Fig. 11(b). Degradation of the temperature coefficient at currents < 16 μA may be caused by the temperature dependence of the amplifier offset voltage. At this lower current, the offset voltage is no longer negligible since the reference voltage is < 250 mV.

Fig. 12(a) shows the line regulation for a current reference of 29.5 μA. A line regulation of < 0.7%/V was obtained for a supply voltage of 2.3 to 3.3 V. The reference exhibit a maximum line regulation of 1%/V for a current range of 5 μA to 53 μA as shown in Fig. 12(b).



(a) (b)

Fig. 11. Temperature coefficient: (a) Plot of the current reference against temperature for different programmed values. (b) Plot of the temperature coefficient obtained for different programmed current reference values from 4 different prototypes.



(a) (b)

Fig. 12. Power supply sensitivity. (a) Plot of the current reference against power supply variation. (b) Power supply sensitivity for different programmed current reference values.

Fig. 13 shows an error plot of different programmed current reference values, from 200 nA to 100 μA. A reference accuracy of $< 0.02\%$ was obtained for currents > 3 μA. A degradation in accuracy at the lower currents occurred due to resolution limitations; the measurement equipment was set to a fix range of 200 μA for the complete measurement. Table I presents a performance summary of the proposed circuit along with a comparison of the proposed current reference with some of the proposed architectures in the literature.

VII. Conclusion

A programmable current reference based on a low-TC resistor has been presented. This reference achieves first-order TC compensation by canceling the negative TC of an on-chip resistor with the positive TC of a transistor operating in the ohmic region. The proposed approach is robust against device parameter variations since the temperature compensation is obtained through charge modification. A wide range and high ac-

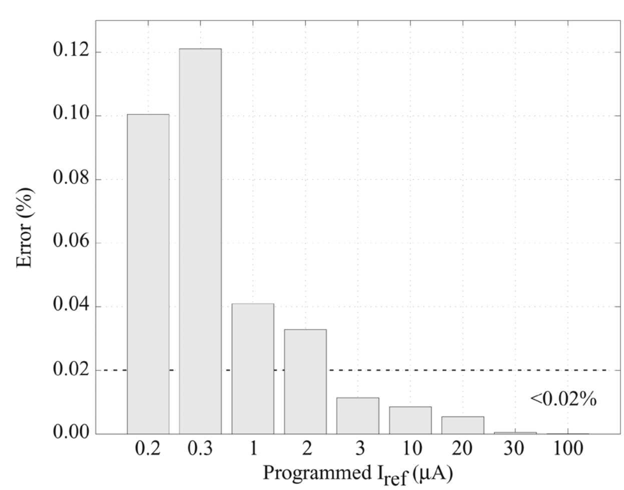


Fig. 13. Current reference precision. Percentage error of the programmed reference currents values from 200 nA to 100 μA.

TABLE I
PERFORMANCE COMPARISON FOR DIFFERENT CMOS CURRENT REFERENCES

	Unit	This Work	Sansen [5]	Chen [1]	Bendali [6]	De Vita [7]
Reference Current	μA	$16 - 50$ [a]	0.774	526	144	0.009
Reference Accuracy	$\%$	< 0.02	2.5	–	7	6.5
Temperature Coefficient	$ppm/^oC$	< 130	375	50	185	44
Temperature Range	^oC	$0 - 80$	$0 - 80$	$0 - 110$	$0 - 100$	$0 - 80$
Min. Power Supply	V	2.3 [b]	3.5	1	1	1.5
Supply Regulation	$\%/V$	< 1	0.015	0.22	–	0.05
CMOS Technology	μm	0.5	3.0	0.18	0.18	0.35

[a]The reference can set to any arbitrary current value within this range while preserving the performance reported.
[b]Minimum power supply that meets the specified performance.

curacy is obtained with precise charge programming. Temperature coefficients of < 130 ppm/°C were obtained for a current range of 16– 50 μA with a precision of $< 0.02\%$.

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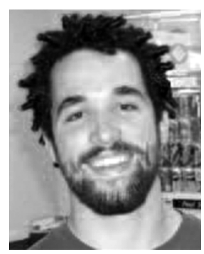

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