

A 20Gb/s SerDes Transmitter with Adjustable Source Impedance and 4-tap Feed-Forward Equalization in 65nm Bulk CMOS

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Abstract—The design and wafer probe test results of a 20Gb/s Source-Series Terminated SerDes transmitter are presented. The integrated circuit, fabricated in a 65nm bulk CMOS technology, transmits pre-emphasized data through the use of a 4-tap feed-forward equalizer. Transmitter output impedance is adjustable from 45 to 55 ohms. A power consumption of 167mW at 1.1V was measured at a transmit rate of 20Gb/s.

I. INTRODUCTION

Source-Series Terminated (SST) transmitters have been known to offer a lower power solution for SerDes signal transmission while maintaining the ability to handle a large range of termination voltages [1,2]. This makes this type of transmitter compatible with multiple termination standards compared to their CML counterparts. This paper will describe an SST transmitter with 4-tap feed-forward equalization (FFE) operating at data rates up to 20Gb/s. Key features of this work include adjustable source impedance for optimized matching to variations in transmission media impedances and the achievement of 20Gb/s data rate using a standard bulk CMOS technology. Also included is an on-chip programmable PRBS test pattern generator with an enhanced parallel architecture to meet the testing speed requirements. The output stage contains T-coils which enable broad-band impedance matching with a return loss of -11dB over 20GHz while still providing ESD protection for the macro [3].

II. Architecture

Figure 1 shows a high level block diagram of the SerDes transmitter. In this design, a programmable pattern generator is used to generate 8-bit wide pseudo-random data patterns. An 8:2 multiplexer serializes the pattern data into odd and even data streams. The half-rate interleaved transmitter passes both serial data streams through a 4-tap digital finite impulse response (FIR) filter. The FIR filter performs feed-forward equalization on the transmit data. The FIR filter is comprised of a four-delay shift register with tap sign select and 2:1 multiplexers integrated within the 64 driver slices. The tap sign select function allows each tap of the feed-forward equalizer to be assigned either a positive or negative value. The 2:1 multiplexers individually assign each of the 64 driver slices to the ‘main’ tap or to one of either the ‘pre’, ‘post1’ or ‘post2’ taps. Impedance adjustment can be used to offset output impedance variability across process variations as well

as to match the driver output impedance to the impedance of the desired channel fabric. The ESD device has been integrated into a T-coil which isolates the device capacitance of the ESD structure from the driver output. A configuration register is used to control the pattern generator, set FFE transfer function and adjust output impedance.

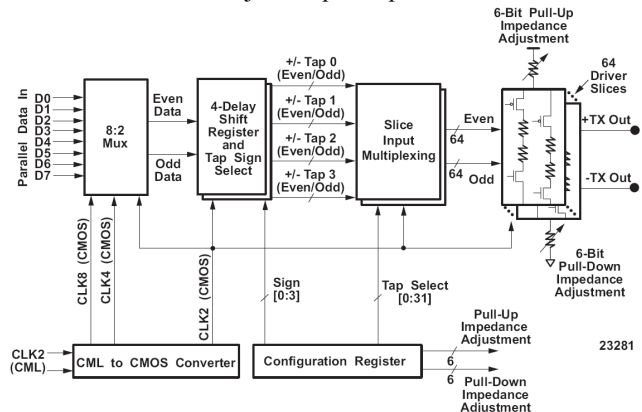


Fig. 1. SerDes Transmitter High-Level Block Diagram

The clock generation circuitry converts a reference current-mode logic (CML) half-rate clock signal into the full rail-to-rail CMOS clocks needed by the transmitter. Half-rate, quarter-rate and eighth-rate clocks are generated on-chip and distributed to the appropriate parts of the transmitter. Duty-cycle correction is incorporated on-chip to maximize the transmitter data rate while minimizing deterministic jitter [1].

III. Circuit Concepts

The transmitter accepts parallel input data via an 8-bit wide data bus at the 8:2 data multiplexer. The 8-bit data stream is generated by an on-chip programmable data generator described later in this section. A simplified schematic of the 8:2 data multiplexer is shown in Figure 2. The parallel input data is latched by eight flip-flops that are clocked at eighth-rate. Four latches, running on the opposite phase of the eighth-rate clock are used to delay four of the data bits by half a clock period. Four 2:1 multiplexers convert the 8-bit wide bus operating at eighth-rate into a 4-bit wide bus operating at quarter-rate. The process is repeated using two 2:1 multiplexers, two latches, and the quarter-rate clock to

create a 2-bit wide bus operating at half-rate. The 2-bit wide data (i.e. interleaved data) is used throughout the transmitter until it reaches the SST output driver, where it is converted into full-rate data.

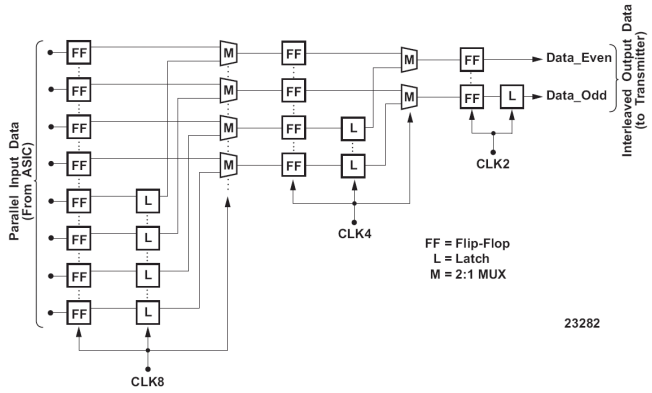


Fig. 2. Block Diagram of 8:2 data multiplexer

In order to implement a four-tap feed-forward equalizer, delayed versions of the interleaved transmitter data must be created. This is accomplished with the four-stage shift register shown in Figure 3. A four-tap FFE requires pre-cursor data, which occurs one bit before the main data, the main data, which has no time delay, post1 data, which is delayed by one bit relative to the main data, and post2 data, which is delayed by two bits. XOR gates are added into the data path for each of the four taps to allow the tap to have either a positive or negative sign.

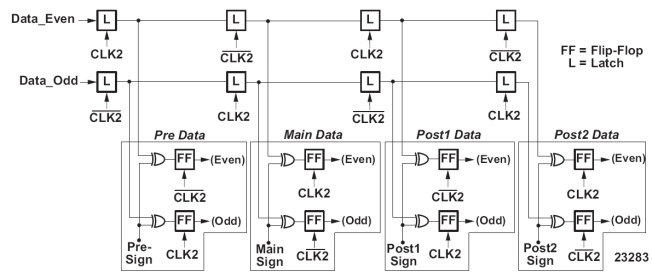


Fig. 3. Schematic of Four-Delay Shift Register With Tap Sign Select

The input to each of the 64 output driver slices has its own front-end logic to connect to the four-delay shift register. To allow every SST driver slice to be assigned to any tap weight, a 4:1 multiplexer would be required. However, in 65nm bulk CMOS, the propagation delay of a standard-cell 4:1 or 2:1 multiplexer could not meet the timing requirements for the period of a half-rate 20Gb/s clock. To achieve timing, a custom 2:1 multiplexer was used, which was implemented with four data capture latches and two transmission gates shown in Figure 4. The 2:1 multiplexer constraint on all driver slices limits equalization options. A choice was made to allow all 64 driver slices to act as main taps, but only a maximum of 8 can be programmed as pre taps, a maximum of 16 as post1 taps, a maximum of 8 as post2 taps and still have 32 assigned to the main tap. The SST differential driver slices require true

and complement data to be generated and present at their inputs with accurate timing placement between them. This was accomplished through the use of complementary pass-gate logic (CPL) latches, which accept the true and complement data (and associated skew) from the previous latch and inverter and aligns the complementary signals. In a similar transmitter design implemented in SOI [1], the driver slice logic used a standard cell 4:1 multiplexer and was able to meet timing requirements which resulted in significant power savings over this work.

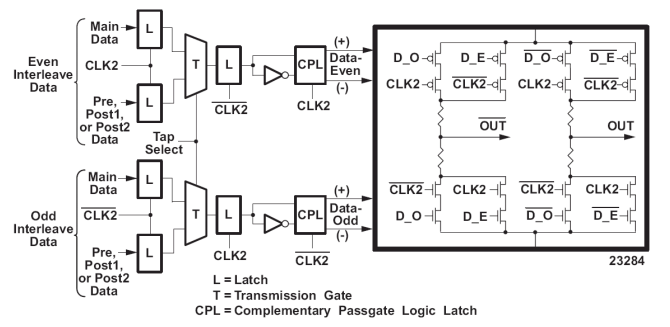


Fig. 4. Simplified Schematic of SST Output Driver Slice Logic

The method used for adjusting the source impedance of the transmitter outputs from 45 to 55 ohms is shown in Figure 5. An adjustable resistance is added in series with the pull-up and pull-down networks of all 64 transmitter slices. The selectable resistors compensate for the varying resistance of the FETs and resistors due to process variation. Additionally, the transmitter source impedance can be adjusted to match manufacturing variations in channel fabric impedances; minimizing reflections at the transmitter output.

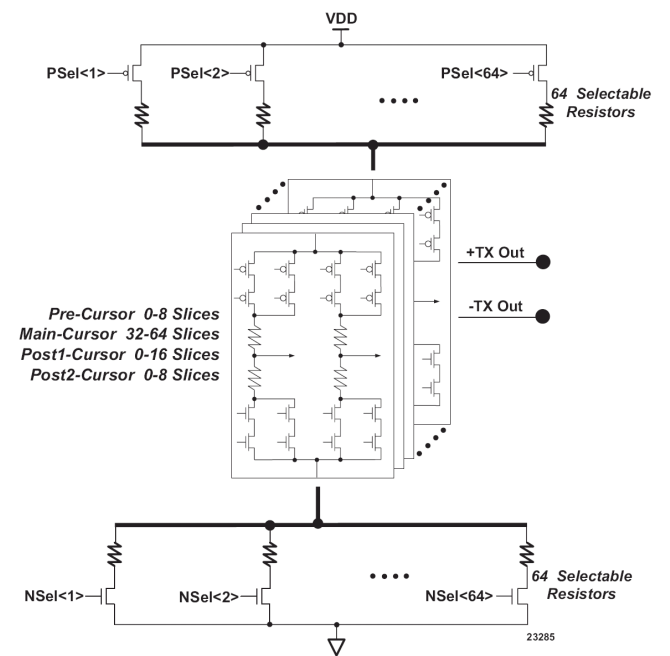


Fig. 5. Diagram of 64 Transmitter Slices With Source Impedance Adjustment

A photograph of the SST transmitter is shown in Figure 6. The die dimensions are 1.0mm x 1.0mm. Differential clock inputs enter from the top and are routed to the clock receiver with 50 ohm transmission lines. The differential outputs are routed through T-coil networks prior to exiting at the bottom. Shift register and pattern generation control occurs from the left and right sides. Embedded within the macro is 100pF of decoupling capacitance for supply noise suppression.

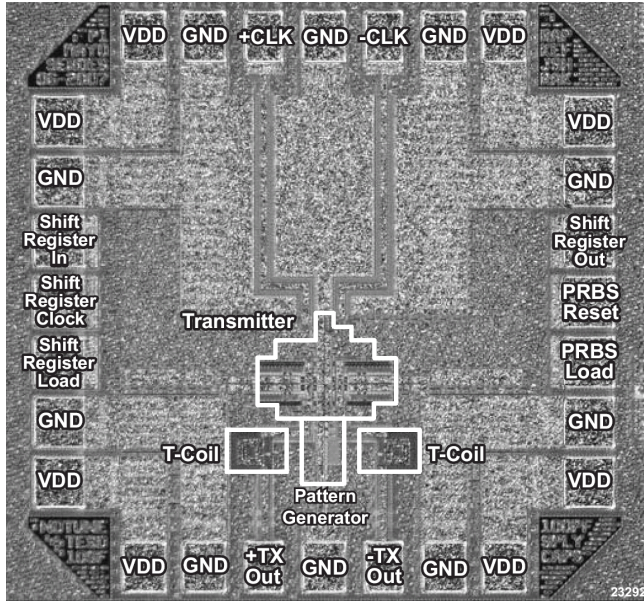


Fig. 6. Photograph of SST Transmitter Macro

The detailed circuit layout of the transmitter macro is shown in Figure 7. The 64 slices are partitioned into two halves. The impedance tuning circuitry is partitioned into four equal blocks located in each of the four layout quadrants. In the center of the macro are the data multiplexer, FFE tap control and CMOS clocking. The area of the macro is 0.025mm².

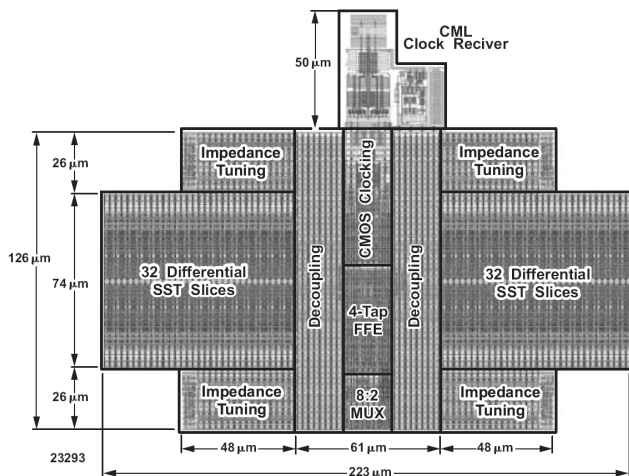


Fig. 7. Detailed Circuit Layout of Transmitter Macro

IV. Testing and Measured Performance

Testing of the SST transmitter was performed using a wafer probe station. An Agilent 8257D signal generator was used for the clock source due to its very low phase noise close-in to the carrier frequency. An Agilent Infiniium DCA-J 86100C scope with an Agilent 86107A precision time base was used to capture eye diagrams and measure jitter.

To simplify testing, a programmable pattern generator was integrated on-chip with the SST transmitter. A parallel design architecture, shown in Figure 8, was adopted to achieve input data speeds while minimizing power consumption [4]. Four pseudo-random bit sequence test patterns (2^7-1 , $2^{15}-1$, $2^{23}-1$, $2^{31}-1$) are available as well as a user-programmable 40-bit repeating pattern. An all-zero detect circuit is included to ensure the pseudo-random sequence generators start up in a valid state.

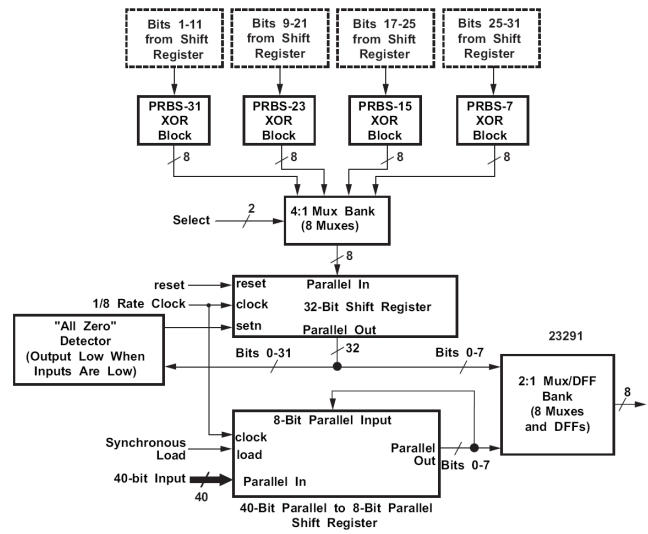


Fig. 8. Block Diagram of Programmable Pattern Generator

Figure 9 shows the measured eye diagram with FFE (pre=0, main=49, post1=11 and post2=4) applied to a 20Gb/s PRBS-15 signal at a supply voltage of 1.1V. The measured eye opening was 300mVpp. The measured random rms jitter was 239fs, with a duty cycle distortion error of 870fs (0.0174 UI). A deterministic jitter of 5.64ps was observed and a total jitter of 8.95ps was achieved at a BER of 1E-12. Figure 10 shows the return loss for three different transmitter output configurations: no ESD, with ESD and ESD embedded into a T-Coil. For each case, the output impedance was tuned to 50 ohms at DC. The best return loss of -11dB was achieved over broadband range up to 20GHz (supportive of a 40Gb/s data rate) with the use of a T-Coil. The measured power consumption of the transmitter including the CML clock receiver, but minus the pattern generator power, at different power supply voltages and data rates are shown in Figure 11. Table 1 compares our work to other transmitter examples in 65nm bulk CMOS and SOI. At 16Gb/s our design consumes twice the power of the reported SOI design due to the use of 64 driver slices versus 44 [1] and the custom 2:1 multiplexer

function and CPL latches required in each driver slice to meet timing requirements at 16Gb/s and 20Gb/s. This is the first known reported example of an NRZ-based transmitter achieving 20Gb/s with adjustable source impedance in a 65nm bulk or SOI CMOS technology.

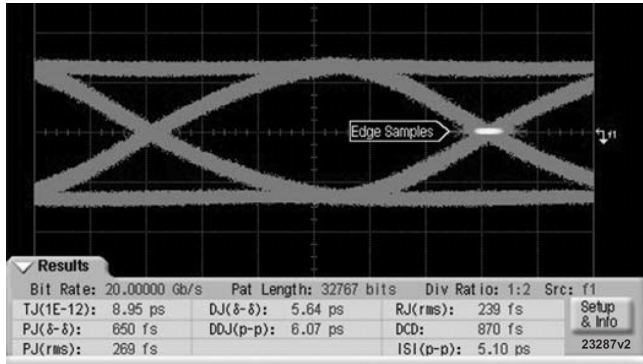


Fig. 9. Differential Eye Diagram of PRBS-15 at 20Gb/s After Equalization

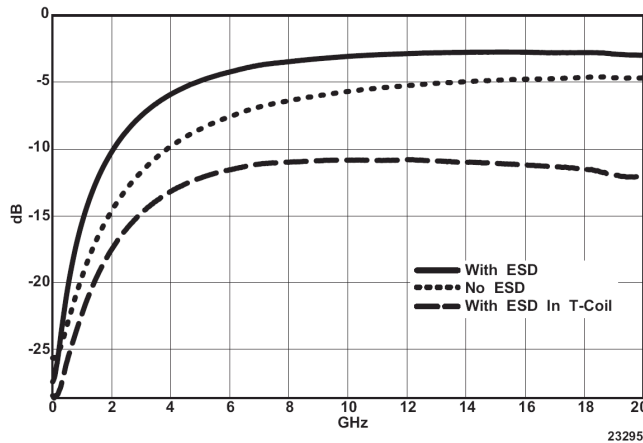


Fig. 10. Measured Return Loss of Transmitter Output

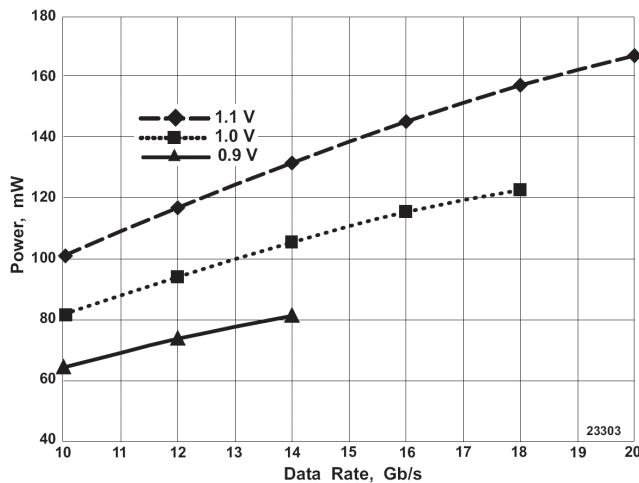


Fig. 11. Transmitter Power Consumption vs. Data Rate

Specification	This Work	This Work	IBM Zurich [1]	TI [5]
Technology	65nm bulk	65nm bulk	65nm SOI	65nm bulk
Maximum Data Rate	20Gb/s	16Gb/s	16Gb/s	12.5Gb/s
Power Consumption	167mW @ 1.1V	115mW @ 1.0V	57.7mW @ 1.0V	~130mW
Power Efficiency	8.3 mW/Gbps	7.2 mW/Gbps	3.6 mW/Gbps	~10.4 mw/Gbps
Feed Forward Equalization	4-tap FIR	4-tap FIR	4-tap FIR	4-tap FIR
Active Area	0.025mm ²	0.025mm ²	~0.013mm ²	~0.08mm ²

Table 1. Comparison of Mayo SerDes with Other Recent Examples

V. CONCLUSION

A 20Gb/s Source-Series Terminated (SST) SerDes transmitter using 65nm bulk CMOS technology has been developed and tested. Tunable output impedance was implemented to achieve a good source match at DC. A T-Coil was used to improve the output impedance matching over a broad frequency range. A 4-tap feed-forward equalizer was demonstrated which minimizes the total output jitter to 8.95ps at an error rate of 1e-12. A measured power consumption of 167mW at 1.1V was observed which is comparable to other 65nm bulk CMOS transmitters but has significant power consumption and area penalties compared to what can be achieved using SOI technology.

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