An Accurate Current Reference using Temperature and Process Compensation Current Mirror

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***Abstract*—In this paper, an accurate current reference using temperature and process compensation current mirror (TPC-CM) is proposed. The temperature independent reference current is generated by summing a proportional to absolute temperature (PTAT) current and a complementary to absolute temperature (CTAT) current. The temperature coefficient and magnitude of the reference current are influenced by the process variation. To calibrate the process variation, the proposed TPC-CM uses two binary weighted current mirrors which control the temperature coefficient and magnitude of the reference current. After the PTAT and CTAT currents are measured, the switch codes of the TPC-CM are fixed in order that the magnitude of reference current is independent to temperature. And, the codes are stored in the non-volatile memory. In the simulation, the effect of the process variation is reduced to 0.52% from 19.7% after the calibration using a TPC-CM in chip-by-chip. A current reference chip is fabricated with a 3.3V 0.35um CMOS process. The measured calibrated reference current has 0.42% variation.**

I. INTRODUCTION

A current reference is an important basic block of analog circuits. The temperature, process variation, and supply voltage insensitive current references are required for the high-performance analog integrated circuits. Several high-precision and temperature-compensated reference circuits have been proposed over the last decades [2]-[4].

In general, a current reference uses on-chip resistors and bipolar junction transistors (BJTs) to make the temperature independent reference current [1]. However, since the on-chip resistors and BJTs are affected by the process variation, the temperature coefficient and magnitude of the reference current have to be adjusted by trimming technology after fabrication. Although the current reference in [3] achieves 28ppm/℃ temperature coefficient, its reference current may change over 15% due to the process variation.

To calibrate the process variation, an area efficient accurate current reference using temperature and process compensation current mirror (TPC-CM) is proposed. It needs a small area and it is easy to increase the current tuning resolution, because it uses two binary weighted current mirrors for controlling the temperature coefficient and magnitude of the reference current.

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II. CURRENT REFERENCE ARCHITECTURE

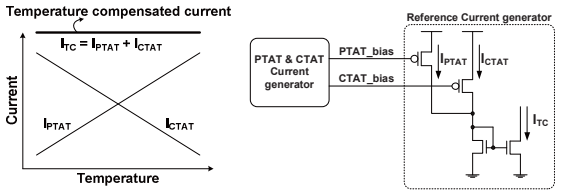

Figure 1. Typical temperature compensated current generator (a) basic principle (b) circuit

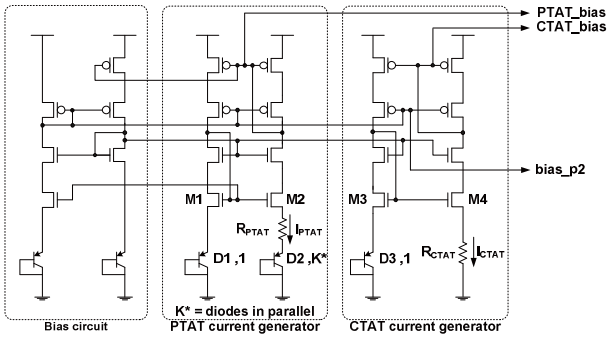

Figure 2. PTAT and CTAT current generator

Fig. 1 shows a typical temperature compensated current generator. The PTAT-CTAT current generator makes a proportional to absolute temperature (PTAT) current and a complementary to absolute temperature (CTAT) current. The temperature compensated current (I_{TC}) is made by summing the PTAT and CTAT currents, as shown in Fig. 1(b).

Fig. 2 shows the PTAT-CTAT current generator circuit. The PTAT current (I_{PTAT}) is produced by the diode D1, diode D2, and resistor R_{PTAT}. The diode D2 is K times larger than the diode D1. The CTAT current (I_{CTAT}) is produced by the diode D3 and resistor R_{CTAT}. The equations of the PTAT and CTAT currents are derived in [1].

The PTAT current flowing through the diode D2 and its temperature coefficient are as follow.

$$I_{PTAT} = \frac{n \cdot k \cdot \ln K}{q \cdot R_{PTAT}} \times T \quad (1)$$

$$TC\_I_{PTAT} = \frac{1}{I_{PTAT}} \times \frac{\partial I_{PTAT}}{\partial T} = \left(\frac{1}{T} - \frac{1}{R_{PTAT}} \times \frac{\partial R_{PTAT}}{\partial T} \right) \quad (2)$$

The poly resistor used in this paper has positive temperature coefficient.

$$R(T) = R(T_O) \times [1 + TC_{1R}(T - T_O) + TC_{2R}(T - T_O)^2] \quad (3)$$

The first temperature coefficient of the poly resistor (TC_{1R}) is 334.77ppm/℃ and the second temperature coefficient (TC_{2R}) is 3.0775ppm/℃. The PTAT current is considered to increase in proportional to temperature, because the temperature coefficients of the poly resistor are small.

The CTAT current flowing through the R_{CTAT} with the diode D3 voltage (V_{D3}) and its temperature coefficient are as follow.

$$I_{CTAT} = \frac{V_{D3}}{R_{CTAT}}. \quad (4)$$

$$TC\_I_{CTAT} = \frac{1}{I_{CTAT}} \times \frac{\partial I_{CTAT}}{\partial T} = \left(\frac{1}{V_{D3}} \times \frac{\partial V_{D3}}{\partial T} - \frac{1}{R_{CTAT}} \times \frac{\partial R_{CTAT}}{\partial T} \right) \quad (5)$$

In the equation (5), the temperature coefficient of the diode voltage V_{D3} is -2300ppm/℃ and the temperature coefficients of the resistor R_{CTAT} are positive values. Thus, the CTAT current has a negative CTAT temperature coefficient. The CTAT current is inversely proportional to temperature.

As shown in Fig. 1, the temperature compensated current (I_{TC}) is generated by adding the PTAT and CTAT currents having the inverse temperature coefficients. However, the PTAT and CTAT currents are changed by the process variations of the diodes, resistors, and transistors.

III. Proposed Current Reference

The reference current is made from the summing the PTAT current and the CTAT current. To make the temperature independent current, the absolute value of the temperature coefficient of the PTAT current (TC_I_{PTAT}) must be equal to that of the CTAT current (TC_I_{CTAT}). To do this, TC_I_{PTAT} is fixed and TC_I_{CTAT} is adjusted, because TC_I_{CTAT} is easy to control its magnitude than TC_I_{PTAT}.

As shown in Fig. 3(a), the PTAT current slope, which is TC_I_{PTAT}, is fixed. Fig. 3(b) shows that the CTAT current slope, which is TC_I_{CTAT}, is adjusted with 2^N resolutions by using an N-bit binary weighted current mirror. Fig. 3(c) shows that the PTAT-CTAT current, which adds the PTAT and CTAT currents, is changed by adjusting the CTAT current slope. The PTAT-CTAT current can be independent of temperature like as the target line. The reference current is made by adjusting the current level of the temperature independent PTAT-CTAT current. As shown in Fig. 3(d), the current level is controlled with 2^M resolutions by using the other M-bit binary weighted current mirror.

By using the two binary weighted current mirrors, the temperature coefficient and level of the reference current is easily adjusted. Even if large process variations exsist, the accurate temperature independent reference current is guaranteed by finding the proper switch codes of two current mirrors. The switch codes are selected after the individual chip measurement.

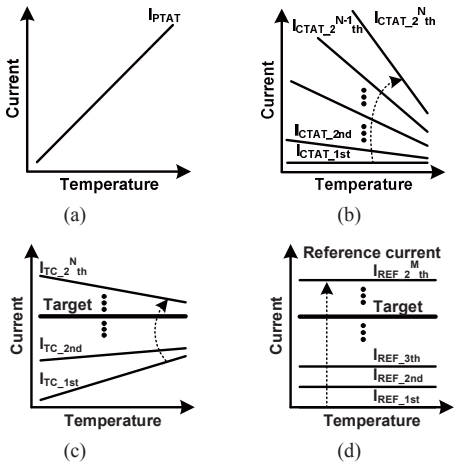

Figure 3. (a) fixed PTAT current vs. temperature (b) adjustable CTAT current vs. temperature (c) $I_{PTAT} + I_{CTAT}$ current vs. temperature (d) reference current level adjusting

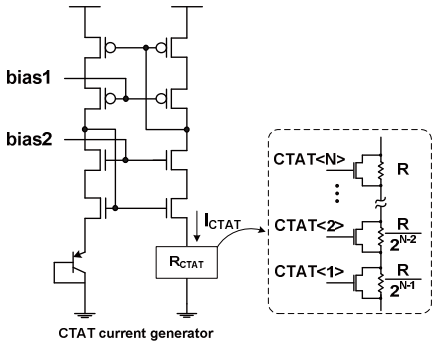

Figure 4. CTAT current adjusting circuit using a string of resistors

A general method to adjusting the CTAT current slope is changing the value of the R_{CTAT} with a string of binary weighted resistors after the chip test, as shown in Fig. 4. The value of R_{CTAT} is changed by turning on or off the switches connected to the binary weighted resistors. But, a large chip area is required to make the binary weighted resistors. Especially, as the number of the CTAT switch codes (N) increases linearly, the resistor area increase exponentially.

Fig. 5 shows the proposed temperature and process compensation current mirror (TPC-CM) circuit. It consists of a PTAT and CTAT current measure circuit, a CTAT current slope adjusting circuit, a PTAT and CTAT current adding circuit, and a reference current level adjusting circuit.

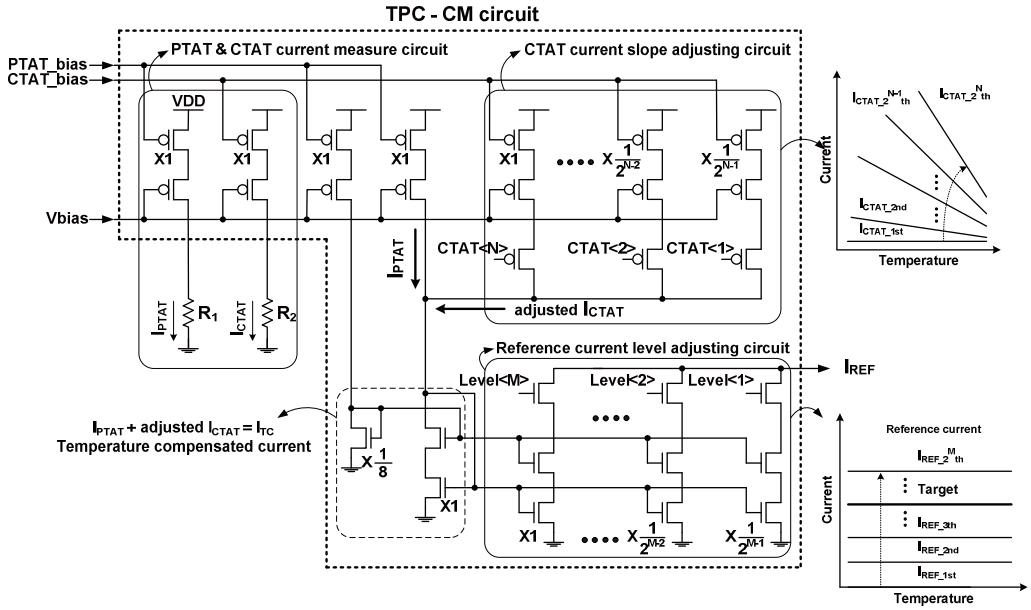

Figure 5. Temperature and process compensation current mirror (TPC-CM) circuit

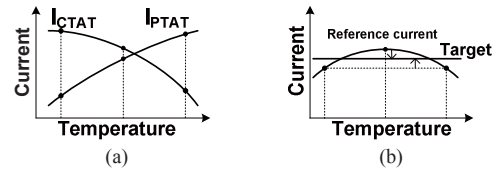

Figure 6. The PTAT and CTAT current slopes measuring method (a) measurement points (b) calibrated reference current

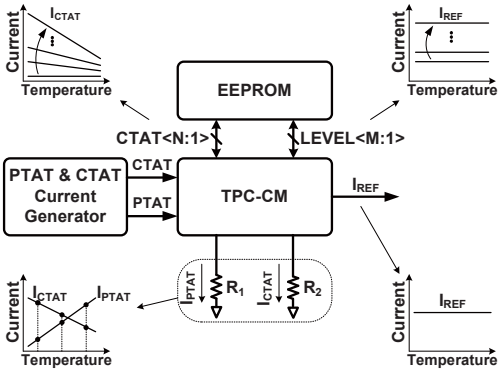

Figure 7. The block diagram of the proposed current reference circuit

The TPC-CM receives the PTAT and CTAT bias voltages for their currents from the PTAT and CTAT current generator. It also needs two switch codes to control the CTAT current slope and the reference current level. It makes the accurate temperature independent reference current.

The PTAT and CTAT current measure circuit has two terminals connected to two external resistors. I_{PTAT} and I_{CTAT} are measured with the voltages of the resistors. To calculate each current slope, I_{PTAT} and I_{CTAT} have to be measured at three different tempertature points, as shown Fig. 6. The reason is that I_{PTAT} and I_{CTAT} graphs are curved lines due to the resistors with the second order temperature coefficient. The ratio of the PTAT and CTAT current slopes becomes the N-bit switch code of the binary weighted current mirror in the CTAT current slope adjusting circuit. The adjusted CTAT current is generated by the CTAT current slope adjusting circuit. It can be changed between 0 and $2\times I_{CTAT}$.

The temperature compensated current is made by summing the adjusted CTAT current and the fixed PTAT current. Its current level is changed to the target current level in the reference current level adjusting circuit, which consists of the M-bit binary weighted current mirror. It can be changed between 0 and $2\times$(adjusted $I_{CTAT} + I_{PTAT}$).

Fig. 7 shows the block diagram of the proposed current reference circuit. It is composed of the PTAT-CTAT current generator, the temperature and the process compensation current mirror (TPC-CM) circuit, and the non-volatile memory to store switch codes of the TPC-CM.

IV. CHIP IMPLEMENTATION

The current reference using the TPC-CM circuit was implemented and simulated with a 3.3V 0.35um standard CMOS process. It is realized with a 10-bit (N=10) current-slope adjusting current mirror and an 8-bit (M=8) current-level adjusting current mirror.

Fig. 8 shows currents vs. temperature at five process corners, and three resistors with average ±3σ variation. The reference current has the maximum value in cases of fast-fast process corner and -3σ resistor variation. And, it has the minimum value in cases of slow-slow process corner and +3σ resistor variation. The reference current is heavily affected by the process variation. The simulation results in Fig. 8(c) and 8(d) show that the TPC-CM reduces the process variation effect to 0.52% from 19.7%. Fig. 8(e) and 8(f) show the

simulated reference current against the supply voltage. The reference current is constant over V_{DD}=2V.

Fig. 9(a) and 9(b) show the measured PTAT and CTAT currents and the measured reference current, respectively. Due to the process variation, the simulated I_{PTAT} and I_{CTAT} currents are different from the measured I_{PTAT} and I_{CTAT} currents of the fabricated chip. By measuring I_{PTAT} and I_{CTAT} at three different temperature points, two switch codes of the TPC-CM are obtained. The temperature compensated current with the target current level is generated. After the calibration, the measured reference current has only 0.42% variation for 20~100℃.

Fig. 10 shows chip area comparison of the reference current circuit layout using a string of resistors for the CTAT current adjusting and the proposed reference current circuit layout using the TPC-CM. The proposed circuit area decreases to 40% compared with the conventional reference circuit. Fig. 11 shows the fabricated current reference chip photograph. Table 1 presents the performance comparison of current references.

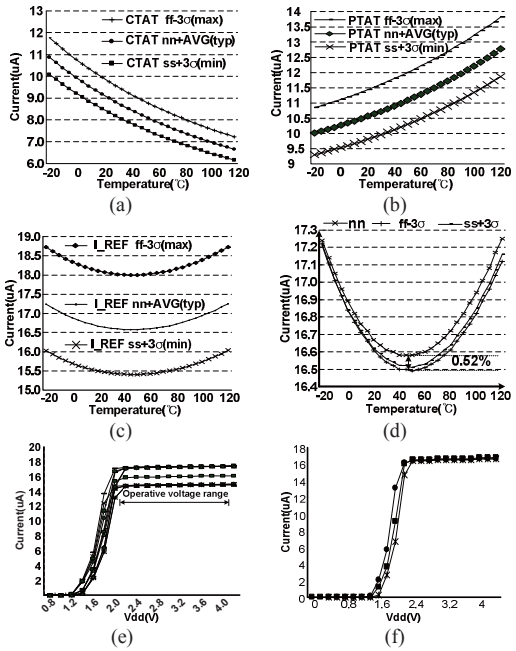

Figure 8. Currents vs. temperature at five process corners and three resistors with average ±3σ variation (a) CTAT current (b) PTAT current (c) reference current without the TPC-CM (d) reference current using the TPC-CM (e) reference current vs. supply voltage without the TPC-CM (f) reference current vs. supply voltage using the TPC-CM

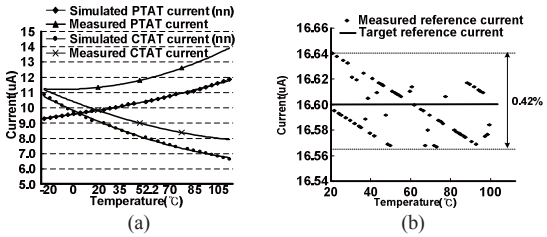

Figure 9. (a) Measured PTAT and CTAT currents (b) Measured reference current

I. CONCLUSION

The area efficient accurate current reference using the TPC-CM is proposed. To calibrate the process variation, the proposed TPC-CM uses two binary weighted current mirrors which control the temperature coefficient and magnitude of the reference current. After the PTAT and CTAT current measurements, the temperature and process compensation switch codes of the TPC-CM are stored in the non-volatile memory. In the simulation, the TPC-CM reduces the process variation effect to 0.52% from 19.7%. A current reference chip was fabricated with a 3.3V 0.35um CMOS process. The measured calibrated reference current has 0.42% variation for 20~100℃.

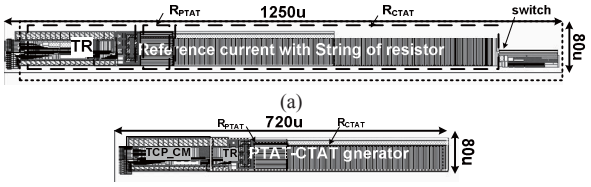

Figure 10. Chip area comparison (a) reference current circuit layout using a string of resistors for the CTAT current adjusting (b) proposed reference current circuit layout using the TPC-CM

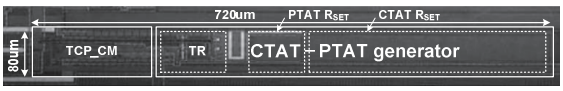

Figure 11. The fabricated current reference chip photograph

TABLE I. PERFORMANCE COMPARISION OF CURRENT REFERENCES

	This work	[6]	[3]
Technology	0.35um CMOS	0.25um CMOS	0.35um BiCMOS
Temperature coefficient [ppm/℃]	280	720	28
Resistor (poly) [Ω/□]	65 ± 10	N/A	N/A
Temperature range [℃]	-20~100	0~120	-30~100
Supply voltage [V]	3.3	2.5	3.3
Minimum supply voltage [V]	2	1.1	2.5
Area [mm^2]	0.0576	0.002	0.004
Process variation error [%]	0.52	N/A	15

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