Fully On-Chip Temperature, Process, and Voltage Sensors

Shi-Wen Chen, Ming-Hung Chang, Wei-Chih Hsieh, and Wei Hwang Department of Electronics Engineering & Institute of Electronics, and Microelectronics and Information System Research Center (MIRC) National Chiao-Tung University, Hsin-Chu 300, Taiwan dodolon.ee97g@nctu.edu.tw

Abstract-A process, voltage, and temperature (PVT) sensor without a voltage/current analog-to-digital converter (ADC) or bandgap reference is proposed for high accuracy, low power, and wide voltage range portable applications. Conventional temperature sensors rely on voltage/current ADC for digital output code conversion. The proposed temperature sensor generates a clock frequency proportional to the measured temperature, and converts the frequency into a corresponding digital code. The generated digital code is still under the influence of PVT variations. Two distinct sensors for voltage and process monitoring are also proposed to enhance temperature sensor environmental variation immunity. The property of zero temperature coefficient (ZTC) bias point is used to remove temperature effect. The proposed wide voltage range low power PVT sensor is designed in UMC 65nm bulk CMOS technology. It is capable of operating over a wide voltage range within 0.3V~1V. The power consumption is no more than $3.7\mu W$ at 0.3V supply voltage and a high sample rate of 10k samples/sec. The temperature error is merely -0.8~0.8°C.

I. INTRODUCTION

Wireless microsensor network (WSN) technology creates enormous possibility to have a positive impact on our lives in the near future. Advances in ultra-low voltage (ULV) circuit design have recently demonstrated capabilities compatible with wireless body area sensor networks (WBASNs) needs. To maximize the benefits of ultra-low power (ULP) techniques, weak inversion logic is essential for digital circuit elements [1]. Optimal ULP circuits operate in subthreshold region because supply voltage reduces dynamic energy consumption quadratically and minimum energy operation usually occurs in the weak conversion region [2]. However, leakage in weak inversion region increases dramatically and drain current decreases exponentially both impacting on-off current ratio. It can significantly degrade the performance and reliability of circuits when the ratio is getting too small. Weak inversion circuits are far more sensitive to PVT variations than super threshold ones. Thus, minimizing energy dissipation and improving variation immunity are far more important rather than operating frequency. Thus, a process, voltage, and temperature (PVT) aware subthreshold clocking design is essential to solve the one last puzzle in ULV circuits.

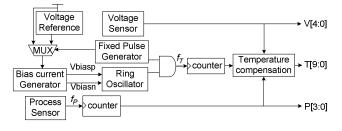


Figure 1. Architecture of proposed PVT sensor circuit.

For body sensors, power is interconnected because battery size directly relates to the degree of lifetime of the sensor node. Since wearable sensors are intended to be worn on the body, miniaturization and minimal weight are important [1]. Energy harvesting and 3D integration have the potential to solve above mentioned challenges. Energy harvesting [3] can exploit the external environment as a source of energy for sensor nodes operating over a full lifetime; while 3D integration [4], [5] can stack more die connected with a very high packing density of one chip. Through-silicon via (TSV) technology, however, led to higher power density that is much worse hot spot issues. Thus, a temperature aware power management unit for energy harvesting is also essential.

In a nutshell, weak inversion circuits are far more sensitive to PVT variations, and 3D integration technique has much worse hot spot issues. Thus, a PVT sensor is proposed to provide a real-time environment monitoring solution. The organization of this paper is as follows. An overview of the proposed PVT sensor is introduced in Section II. Section III present individual building blocks of proposed PVT sensor circuit. The simulation results of PVT sensor, which is implemented in UMC 65nm CMOS technology model, are shown in Section IV. Finally, conclusions are given in Section V.

II. ARCHITECTURE

The architecture of the proposed micro-watt and wide voltage range PVT sensor, shown in Fig. 1. The PVT sensor consists of four major blocks; they are temperature sensor, voltage sensor, voltage reference, and process sensor. Firstly,

This research is supported by Ministry of Economic Affairs, Taiwan, R.O.C., under Grant 97-EC-17-A-03-S1-005. The authors would like to thank Ministry of Education, Taiwan, R.O.C. and ITRI for their support.

temperature sensor generates a frequency (f_T) proportional to the measured environmental temperature. The output frequency digital code connects to "clock" pin of counter, and the counter can be positive edge triggered generating the corresponding digital output T[9:0]. The output T[9:0] represents the corresponding environmental temperature, but it is influenced by process and voltage variations. Therefore, a process sensor and voltage sensor are proposed to reduce PV variation of temperature sensor.

The real-time process and voltage environment information is also generated as P[3:0] and V[4:0], respectively. The process sensor use ZTC characteristic to design and it is independent of temperature variation. The process sensor also generates a frequency (f_P) proportional to the measured process corner. The operation is very similar to temperature sensor. The voltage sensor uses a voltage-to-time converter, which measures inverter chain delay time of corresponding supply voltage. The P[3:0] and V[4:0] can not only reduce PV variation of temperature sensor, but also provide the process and voltage environment information.

III. TEMPERATURE, PROCESS, AND VOLTAGE SENSORS

A. Process Sensor

MOS current varied with temperature, process, and voltage. Mutual compensation of mobility and threshold voltage temperature variations may result in a zero temperature coefficient (ZTC) bias point of a MOS transistor [7]. The process sensor is proposed with ZTC characteristic in Fig. 2. In UMC 65nm bulk CMOS technology, the ZTC points of NMOS and PMOS are at about 0.4V and 0.6V respectively. According to simulation results shown, the delay of unit inverter will not change with temperature variation at 0.5V. Because at 0.5V supply voltage, NMOS I_D decreases with temperature, PMOS I_D increases with temperature. The PMOS and NMOS mutual current compensation leads to the output frequency of ring oscillator is constant.

The proposed fixed pulse generator generates a pulse signal width independent of PVT variation. The detail schematic of the fixed pulse generator is drawn in Fig. 2. It is composed of D-type flip-flop, counter and comparator. When START signal rises, over a delay time (T_{d1}), the output of D-type flip-flop also rises. When "result" signal rises, over a delay time (T_{d2}), the output of D-type flip-flop will be reset to 0. The delay time T_{d1} and T_{d2} both affected by similar PVT variation, so it can be removed. From the above description, the output pulse signal width (W) is invariant from PVT variation.

The Monte Carlo simulation results of process sensor are shown in Fig. 3, and we can find the process corner is linear to the frequency of ring oscillator. Using the linear

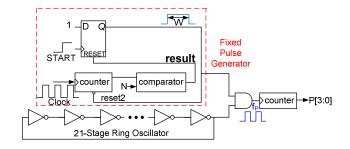
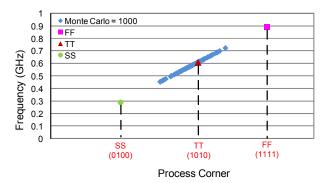
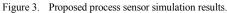


Figure 2. Proposed process sensor.





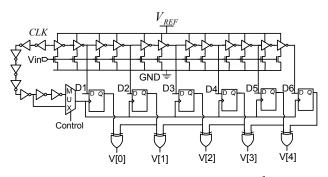


Figure 4. Proposed voltage sensor (based on ULV²TC).

characteristic, the counter converts the output frequency (f_P) to 4-bit digital code P[3:0] from SS corner (0100) to FF corner (1111). The digital code P[3:0] can provide information of process corner.

B. Voltage Sensor

Conventional high-speed, high-resolution ADC was presented in [8], and the power consumption is extremely high (~49mW) and chip area is too large (1.2mm²). The conventional ADC, however, consists of conventional op amplifier. Cascode architecture of conventional op amplifier did not have enough headroom, so it is difficult to design at sub-1V.

TABLE I. VOLTAGE SENSOR DIGITAL CODE TABLE

Vin	Digital Code					
	V[0]	V[1]	V[2]	V[3]	V[4]	
0.3V	1	0	0	0	0	
0.35V	0	1	0	0	0	
0.4V	0	0	1	0	0	
0.45V	0	0	0	1	0	
0.5V	0	0	0	0	1	

One way to overcome the challenge of the low-power and low-voltage design is to process the signal in time-domain. In voltage-to-time converter (VTC), the input analog voltage is converted to time or phase information. Thus, digital VTC circuit was presented in [9]. The circuit can replace conventional analog ADCs, and it can reach low-power, lowvoltage, and small area. However, the VTC is not accuracy with PVT variation. Therefore, a novel ultra-low voltage VTC (ULV²TC) circuit is proposed to improve accuracy.

The proposed ULV²TC with 0.5V voltage reference is presented in this paper, shows in Fig. 4. It converts input voltage to 5-bit digital code V[4:0]. The PVT-aware ULV²TC consists of current starved inverters, flip-flops, and XOR gate. The control bit is from process monitor, and it can reduce the ULV²TC output error. The control bit can compensate process variation, and TABLE I represents the V[4:0] with different voltage. The quantization step of ULV²TC is about 50mv.

C. Temperature Sensor

The proposed temperature sensor, it shows in Fig. 5. The bias current generator shows in Fig. 6, and N1, N2 transistors operate in weak inversion region. Alpha-power subthreshold drain current (I_{D_SUB}) [10] can be expressed as follows:

$$I_{D_{-SUB}} = \mu_0 C_{OX} \frac{W}{L} (m-1) (V_T)^2 \times e^{(V_{CS} - V_{th})/mV_T} \times (1 - e^{-V_{DS}/V_T})$$
(1)

Assume $V_{DS} >> V_T$, The term of $(1 - e^{-V_{DS}/V_T})$ can be ignored. Simplification of the formula can be expressed based on the following:

$$I_{IN} = \mu_0 C_{OX} \frac{W}{L} (m-1) (V_T)^2 \times e^{(V_{GS1} - V_{th})/mV_T}$$
(2)

$$I_{OUT} = \mu_0 C_{OX} \frac{W}{L} (m-1) (V_T)^2 \times e^{(V_{GS2} - V_{th})/mV_T}$$
(3)

Assume
$$I_o = \mu_0 C_{OX} \frac{W}{L} (m-1)$$
 (4)

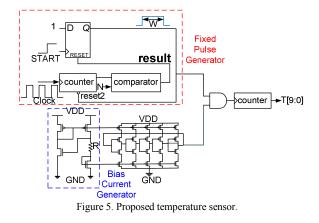
 P_1 and P_2 are current mirror.

So
$$\frac{I_{P_1}}{I_{P_2}} = \frac{W_{P_1}/L_{P_1}}{W_{P_2}/L_{P_2}} = \frac{I_{IN}}{I_{OUT}}$$
 (5)

Simplification (2) and (3) into (6) and (7), the equation becomes

$$V_{GS1} = mV_T \times \ln\left(\frac{I_{IN}}{I_{ON1}}\right) + V_{Ih}$$
(6)

$$V_{GS2} = mV_T \times \ln\left(\frac{I_{OUT}}{I_{ON2}}\right) + V_{th}$$
⁽⁷⁾



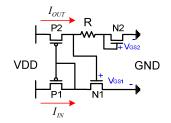
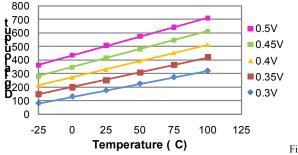
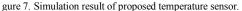


Figure 6. Self bias current generator.





And
$$\frac{I_{ON1}}{I_{ON2}} = \frac{W_{N1}/L_{N1}}{W_{N2}/L_{N2}}$$
 (8)

combine (5)-(8) into (9), the equation becomes

$$I_{OUT} = \frac{V_{GS1} - V_{GS2}}{R} = \frac{mV_T \times \ln\left(\frac{I_{IN} \times I_{ON2}}{I_{OUT} \times I_{ON1}}\right)}{R} = \frac{mV_T}{R} \times \ln\left(\frac{W_{p1}W_{N2} / L_{p1}L_{N2}}{W_{p2}W_{N1} / L_{p2}L_{N1}}\right)$$
(9)

II,
$$L_{P1} - L_{P2} - L_{N1} - L_{N2}$$

Then, $I_{OUT} = \frac{mV_T}{R} \times \ln\left(\frac{W_{p1}W_{N2}}{W_{p2}W_{N1}}\right)$ (10)

The output current of the bias current generator is proportional to temperature, as described in equation (10). The output current is used to charge the inverters, so the frequency of ring oscillator is also proportional to

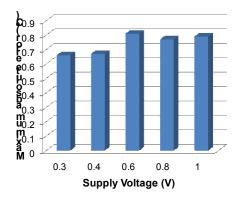


Figure 8. Maximum absolute error of proposed temperature sensor.

temperature. All of above mentioned characteristics have perfect linearity. The fixed pulse generator generates a pulse signal width independent of PVT variation. The ring oscillator output and fixed pulse through 2-AND gate, and the output frequency digital code connects to "clock" pin of counter, and the counter can be positive edge triggered generating the corresponding digital output T[9:0]. The output T[9:0] represents the corresponding environmental temperature, and T[9:0] will be adjusted by proposed PV sensor to reduce the error caused by PV variation.

When the supply voltage is $0.5V \sim 1V$, a voltage reference [6] was presented to generate output voltage below 0.5V. Thus, the output of voltage reference provides a voltage source to temperature sensor. The simulation result shows in Fig. 7, and using voltage sensor and process sensor result to compensation the digital output value.

IV. SIMULATION RESULTS AND COMPARISONS

The proposed PVT sensor is designed in UMC 65nm bulk CMOS technology. The maximum absolute error of the temperature sensor is shown in Fig. 8. At 0.3V supply voltage, the power consumption is only 3.7μ W at the conversion rates of 10k sample/sec. The temperature error is only $-0.8 \sim 0.8^{\circ}$ C. A comparison chart between this work and previously presented temperature sensors is shown in TABLE II. In TABLE II, the main characteristics, such as operation supply voltage, power, error, temperature range, sensor type, process technology, and conversion rate are compared. In this paper, the fully on-chip PVT sensor is proposed, and it can operate on ultra-low power, ultra-low voltage, wide voltage range, and high sample rate.

V. CONCLUSIONS

In this paper, a PVT sensor without a analog-to-digital converter (ADC) or bandgap reference is proposed for highaccuracy, ultra-low power, wide voltage range portable applications. Conventional temperature sensors rely on ADCs for digital output code conversion. The proposed temperature sensor generates a clock frequency proportional to the measured temperature, and converts the frequency into a corresponding digital code T[9:0]. A voltage sensor and process sensor are proposed to compensate temperature

TABLE II. TEMPERATURE SENSOR COMPARISONS

	[11]	[12]	[13]	Proposed
Supply (V)	3.0	1.0	3.0	0.3~1.0
Power (µW)	10	25	4.5	3.7
Error (°C)	-0.7~0.9	-1.0~0.8	-0.6~0.6	-0.8~0.8
Temperature (°C)	0~100	50~125	-40~60	-50~+125
Sensor Type	Temp- to-Pulse	Analog Voltage	Temp-to- Pulse	Temp-to- frequency
Process	0.35um	90nm	0.35um	65nm
Conversion Rate (samples/sec)	10k	4	10	10k

sensor. The voltage sensor and process sensor used ZTC point to design. The sensor was designed in a 65nm CMOS technology. It operate over a wide voltage range from $0.3V\sim1V$. The power consumption is under 3.7μ W at 0.3V and a sample rate of 10k samples/sec. The temperature error is merely $-0.8\sim0.8^{\circ}$ C.

REFERENCES

- B. H. Calhoun, et al., "Sub-threshold operation and cross-hierarchy design for ultra low power wearable sensors," in *IEEE Int'l Symp. Circuits and Systems*, pp. 1437-1440, May 2009.
- [2] B. H. Calhoun, S. Khanna, R. Mann, and J. Wang, "Sub-threshold circuit design with shrinking CMOS devices," in *IEEE Int'l Symp. Circuits and Systems*, pp. 2541-2544, May 2009.
- [3] J. A. Paradiso and T. Starner, "Energy scavenging for mobile and wireless electronics," in *IEEE Pervasive Comput.*, vol. 4, no.1, pp. 18-27, 2005.
- [4] T. Vucurevich, "The long road to 3D integration: are we there yet?," in *3D Architecture Conference*, Keynote Speech, 2007.
- [5] X. Dong and Y. Xie, "System-level cost analysis and design exploration for three-dimensional integrated circuits (3D ICs)," in Asia and South Pacific Design Automation Conf., pp. 234-241, Jan. 2009.
- [6] H. C. Lai and Z. M. Lin, "Ultra-low temperature coefficient CMOS voltage reference," in *IEEE Intl. Electron Devices and Solid-State Circuits Conf.*, pp. 369-372, Dec. 2007.
- [7] I. M. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits," in *IEEE Trans. Circuits Syst.* I, vol. 48, pp. 876-884, Jul. 2001.
- [8] Y. J. Cho and S. H. Lee, "An 11b 70-MHz 1.2-mm² 49-mW 0.18-μm CMOS ADC with on-chip current/voltage references," in *IEEE J. Circuits and Systems*, vol. 52, no. 10, pp. 1989-1995, Oct. 2005.
- [9] M. A. Farahat et al., "Only digital technology analog-to-digital converter circuit," in *IEEE Int'l Symp. Midwest Symposium on Circuits* and Systems, vol. 1, pp. 178–181, Dec 2003.
- [10] K. A. Bowman et al., "A physical alpha-power law MOSFET model," in *IEEE J. Solid-State Circuits*, vol. 34, no. 10, pp. 1410–1414, Oct. 1999.
- [11] P. Chen et al., "A time-to-digital-converter-based CMOS smart temperature sensor," in *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1642-1648, Aug. 2005.
- [12] M. Sasaki et at., "A temperature sensor with an inaccuracy of -1/+0.8 °C using 90-nm 1-V CMOS for online thermal monitoring of VLSI circuits," in *IEEE Trans. Semiconductor manufacturing*, vol. 21, no. 2, pp. 201–208, May 2008.
- [13] C.-C. Chen et al., "An accurate CMOS delay-line-based smart temperature sensor for low-power low-cost systems," *Meas. Sci. Technol.*, vol. 17, no. 4, pp. 840–846, Apr. 2006.