A Resistor-Free Temperature-Compensated CMOS Current Reference

Wei Liu, Waleed Khalil and Mohammed Ismail
Department of Electrical and Computer Engineering
The Ohio State University
Columbus, OH 43210, USA
Email: {liuw, khalil, ismail}@ece.osu.edu

Edith Kussener
Department of Micro and Nanoelectronics
Institut Materiaux Microelectronique Nanosciences de Provence (IM2NP), ISEN_Toulon,
Pompidou, 83000 Toulon, France
Email: edith.kussener@isen.fr

***Abstract*—This paper presents a resistor-free temperature compensated CMOS current reference designed in a standard 0.18 µm CMOS process. The temperature compensation scheme is achieved by combining a PTC (Positive Temperature Coefficient) current generator circuit with a NTC (Negative Temperature Coefficient) current generator circuit. The proposed design is shown to be less sensitive to process and temperature variations and well suited for integration into other circuits as an accurate and stable current source. Simulation results for the proposed current reference show a temperature coefficient of 170 ppm/°C over a temperature range of –20 °C to 120 °C and an output current variation of 3% over a power supply range of 2 V to 3 V.**

I. INTRODUCTION

Analog building blocks such as operational amplifiers, data converters and phase-locked loops (PLLs) rely on current reference circuits to provide accurate and stable current supply. Furthermore, high performance analog circuits require a stable bias point across a wide range of process, voltage and temperature (PVT) conditions. A common method to generate a reference current is to use a voltage reference, such as a bandgap, and resistors as current defining devices. However, the highly process dependent resistors make this scheme sensitive to process and temperature variations. Moreover, the implementation of the voltage reference will consume high power and large silicon area. Recently, a lot of works has been devoted to achieve a resistor-free temperature-compensated CMOS current reference. Research effort using switched capacitor equivalent resistor to substitute the current-defining resistor was reported in [1]. However, the required clock source and on-chip capacitors tend to result in more complexity and large silicon area. Moreover, the impact of the clocking noise on the reference current circuit is another issue that needs to be addressed. Another research focusing on the use of sub-threshold region in MOSFET transistors was reported in [2]-[3]. However, operating the device in sub-threshold is sensitive to both process and temperature variations. Quasi beta multiplier and bandgap reference-based techniques were also proposed in [4]-[5]. Nevertheless, their implementation complexity leads to an increase both in silicon die area and power consumption. Research using floating-gates transistors was reported in [6]. However, the use of high-voltage charge pump and negative-voltage charge pump puts high gate stress on devices, which may induce device reliability failure.

In this paper we propose an area efficient CMOS current reference circuit based on the sum of a PTC current generator and a NTC current generator. Unlike traditional current reference designs, the proposed scheme does not require the use of on-chip resistors or amplifiers. Moreover, since the transistors in this design are all operated in strong-inversion, it is less sensitive to process and temperature variations compared to sub-threshold operation.

This paper is organized as follows. In section II, the architecture of the proposed resistor-free temperature-compensated CMOS current reference is introduced; Moreover, a simplified design analysis showing the dependency on temperature and other device parameters is also described. In section III, detailed transistor-level simulation results illustrating the operation of the proposed design in TSMC's 0.18 µm CMOS process is presented. Finally, the paper concludes with a brief summary of the results in section IV.

II. PROPOSED CIRCUIT ARCHITECTURE AND DESIGN PROCEDURE

The schematic of the proposed CMOS current reference is shown in Fig.1. The main idea behind this circuit is to achieve a temperature-compensated current reference by summing two current cells; one increasing with temperature (PTC) and another one decreasing with temperature (NTC). The temperature coefficients of the PTC and NTC cells are designed to cancel out each other by properly setting the aspect ratios of key devices in the PTC and NTC current generators. The proposed current reference consists of five parts: the startup part, the PTC current generator, the NTC current generator, the bias voltage generation part and the summing part.

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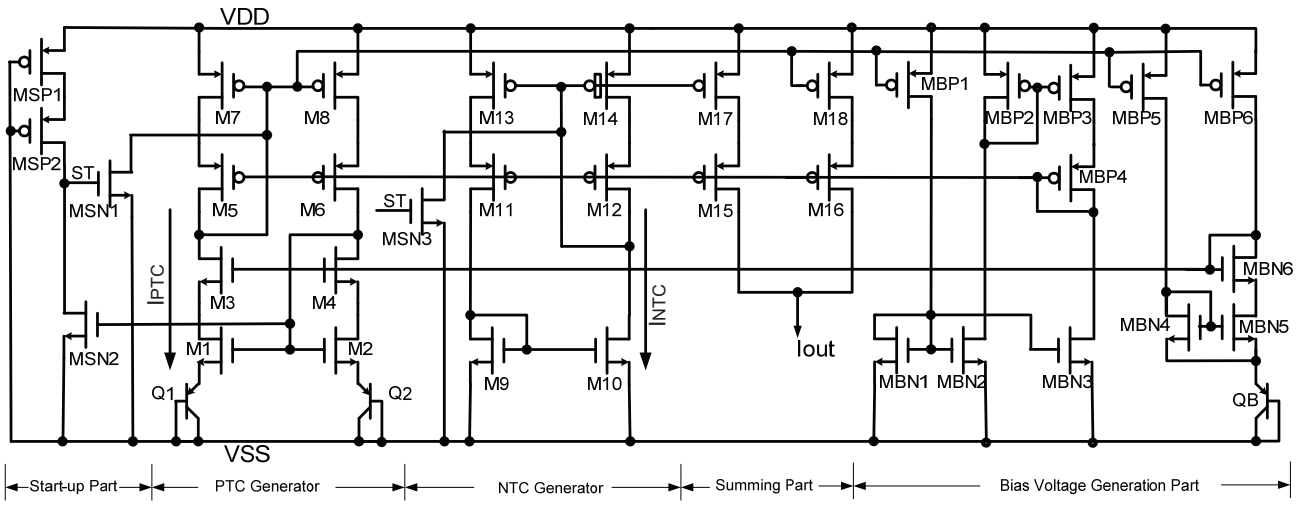

Figure 1. Schematic of the proposed current reference

A. *Positive Temperature Coefficient (PTC) Current Generator*

The PTC current generator consists of transistors M1-M8 as well as bipolar transistors Q1 and Q2 which are operated as diode connected devices [7]. Transistors M5-M8 form a cascode current mirror. Applying Kirchhoff's voltage law around the loop formed by Q1, Q2, M1, and M2, we have:

$$V_{BE1} + V_{GS1} = V_{BE2} + V_{GS2} \tag{1}$$

Also,

$$V_{BE} = V_T \ln(I_E / I_S) \tag{2}$$

$$V_{GS} = \sqrt{2I_D / (K_N S)} + V_{TH} \tag{3}$$

where V_{TH} is the threshold voltage of the MOSFET transistor, K_N is the NMOS device conductivity parameter, V_T is thermal voltage, S is the aspect ratio of the NMOS device (i.e. W/L) and I_E, I_S are the emitter current and the saturation current of the bipolar transistor. Substituting (3)-(2) into (1) and neglecting the body effect in transistors M1 and M2, we have:

$$I_{PTC} = I_{D1} = I_{D2} = \frac{K_N S_2}{2}\left(\frac{V_T \ln m}{\sqrt{n}-1}\right)^2 \tag{4}$$

where m is the emitter areas ratio of bipolar transistor Q1 over Q2, and n is the W/L aspect ratio of M2 over M1. Since K_N is equal to $\mu_n C_{ox}$, where C_{ox} is the gate oxide capacitance per unit area, and μ_n is the mobility of electrons, and given that μ_n is proportional to $T^{-1.5}$ and V_T is equal to kT/q [8], where k is the Boltzmann's constant, then the final current I_{PTC} can be shown to be proportional to $T^{0.5}$.

B. *Negative Temperature Coefficient (NTC) Current Generator*

Transistors M9-M13 and thick oxide MOSFET M14 form the NTC current generator [9], where M13 and M14 share the same n-well. The threshold difference between a nominal MOSFET M13 and a thick oxide MOSFET M14 is used to generate the NTC current. The drain currents of M9 and M10 are given by

$$I_{D9} = I_{D13} = \frac{1}{2} K_P S_{13} (V_{GS13} - V_{TH13})^2 \tag{5}$$

$$I_{D10} = I_{D14} = \frac{1}{2} K_{PT} S_{14} (V_{GS13} - V_{TH14})^2 \tag{6}$$

where K_P and K_{PT} are the conductivity parameters of M13 and M14, respectively. Since I_{D9} is equal to I_{D10} and assuming S_{14}/S_{13} is set equal to A, then (5) can be combined with (6) to arrive at

$$I_{NTC} = I_{D9} = I_{D10} = \frac{A K_P K_{PT} S_{13} (V_{TH14} - V_{TH13})^2}{2\left(\sqrt{AK_{PT}} - \sqrt{K_P}\right)^2} \tag{7}$$

For a given MOSFET transistor, the threshold voltage can be expressed as [8]:

$$V_{TH} = \Phi_{MS} + 2\Phi_F + \sqrt{4q\varepsilon_{si}\Phi_F N_{sub}} / C_{ox} \tag{8}$$

where Φ_{MS} is the difference between the work function of the polysilicon gate and the silicon substrate, N_{sub} is the doping concentration of the n-well, Φ_F is the surface inversion potential and ε_{si} is the permittivity of silicon. Substituting (8) into (7) and noting that:

$$\Phi_F = V_T \ln(N_{sub}/n_i) \quad (9)[8]$$

$$n_i = K_{si} T^{\frac{3}{2}} e^{\frac{-E_g}{2kT}} \quad (10)\ [8]$$

where n_i is the intrinsic carrier concentration of silicon, E_g is the silicon bandgap energy and K_{si} is the temperature coefficient of the intrinsic carrier concentration of silicon. We can then arrive at:

$$\frac{\partial I_{NTC}}{\partial T} = \frac{-3.03\mu_p \varepsilon_{ox} (C_{ox13} - C_{ox14})^2 q N_{sub} S_{13} A}{T(\sqrt{AC_{ox14}} - \sqrt{C_{ox13}})^2} (V_T \ln \frac{N_{sub}}{n_i} + \frac{E_g}{q}) \quad (11)$$

where ε_{ox} denotes the permittivity of silicon dioxide and μ_p is the mobility of holes. Equation (11) shows that a NTC current can be obtained since the temperature coefficient of I_{NTC} at a given temperature T is negative.

Finally, the net reference current is obtained by summing the PTC and NTC currents using transistors M15-M18:

$$I_{OUT} = I_{PTC} + I_{NTC} = \frac{K_N S_2}{2} (\frac{V_T \ln m}{\sqrt{n} - 1})^2 + \frac{A K_P K_{PT} S_{13} (V_{TH14} - V_{TH13})^2}{2\left(\sqrt{AK_{PT}} - \sqrt{K_P}\right)^2} \quad (12)$$

In order to arrive at zero temperature dependency for I_{OUT}, the temperature coefficient of I_{PTC} should be set equal to the temperature coefficient of I_{NTC} at a given temperature T. For I_{PTC}, we have:

$$\frac{\partial I_{PTC}}{\partial T} = \frac{K_N S_2 V_T^{\ 2}}{4T} (\frac{\ln m}{\sqrt{n} - 1})^2 \quad (13)$$

Therefore, different sets of values for m, n and A could be set to make the temperature coefficient of I_{PTC} equal to the temperature coefficient of I_{NTC}.

To reduce the power supply dependency in the proposed current reference, cascode transistors (M3-M6, M11, M12, M15 and M16) are added in the PTC current generator, NTC current generator and the summing circuits.

III. Simulation Results

The resistor-free current reference circuit in Fig.1 was designed in TSMC's 0.18 μm CMOS process with nominal NMOS and PMOS devices threshold voltages of 0.48 V and –0.45 V as well as a thick oxide PMOS device with nominal threshold voltage of –0.69 V. A 2.0 V power supply was used in this design. The emitter areas ratio, m, of bipolar transistor Q1 over Q2 was set as 8; the aspect ratios of M2 over M1, n, and M14 over M13, A, were set as 4 and 9, respectively. The dimensions of different transistors and the most significant performance parameters of the circuit are summarized in Table I and Table II, respectively. The temperature dependency of the proposed current reference was investigated by sweeping the temperature from –20 °C to 120°C and the simulation result is depicted in Fig.2. A temperature coefficient of 170 ppm/°C was calculated from the simulation results. The power supply dependency of the circuit was simulated by sweeping the supply from 2 V to 3 V. As shown from the simulated results in Fig.3, the worst case variation in I_{OUT} across the supply range is only 3%. In order to evaluate the combined process and temperature effects, a Monte-Carlo simulation was performed using the combined process and mismatch analysis from Cadence's circuit simulator. Fig.4 shows the Monte-Carlo simulation result. The mean net reference current value of 10 μA was achieved for 500 samples. Moreover, the standard deviation on I_{OUT} is only 428 nA, which represents a dispersion of ±2.14% for an average value of 10 μA. As shown in Fig.5, the proposed current reference circuit is able to start up successfully when the power supply is ramped from 0 to 2 V within 10 μS. All simulations were run on BSIM3v3 spectre models.

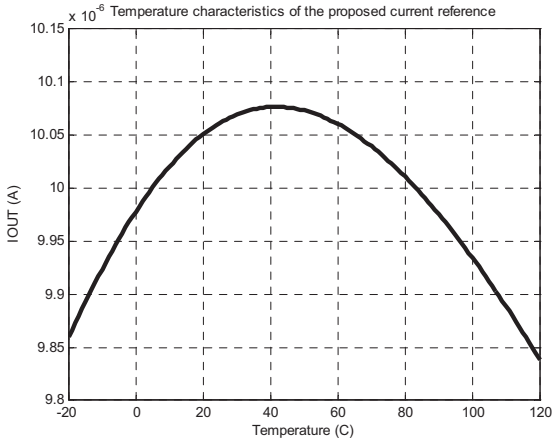

Figure 2. Temperature Characteristics of the proposed current reference

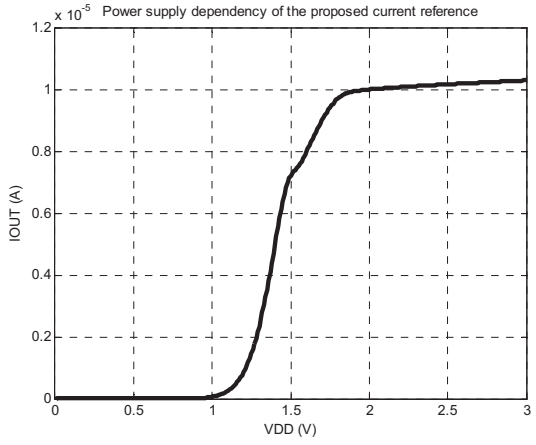

Figure 3. Power supply dependency of the proposed current reference

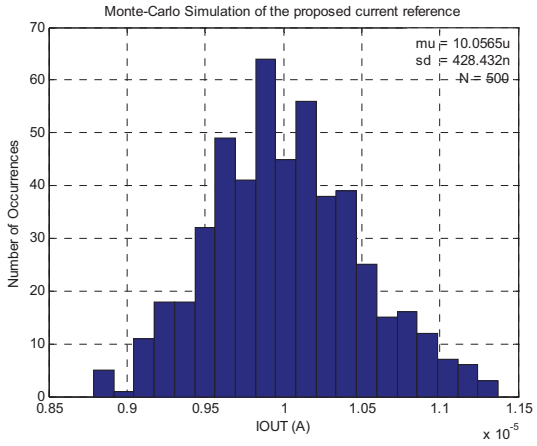

Figure 4. Monte-Carlo simulation result of the proposed current reference

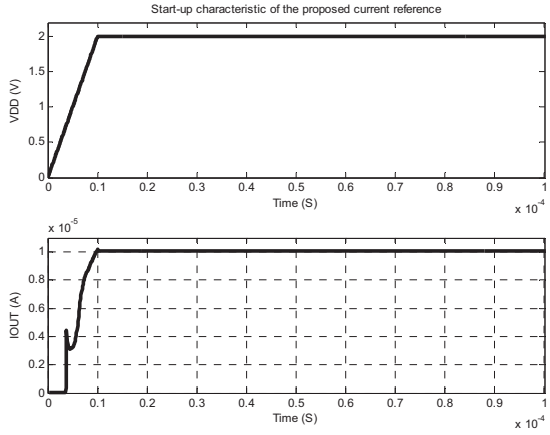

Figure 5. Start-up simulation of the proposed current reference

TABLE I. DIMENSIONS OF TRANSISTORS

Transistors	W (µm)	L (µm)
M5-M8,M11,M12,M15,M16,M18, MBP1~MBP6	5	0.4
M13,M17	2	1
M1,M3,MBN1,MBN2,MBN3,MBN 4	2	0.4
M2,M4,MBN5,MBN6	8	0.4
M9,M10	4	1
M14	18	1
MSP1,MSP2	0.5	20
MSN1,MSN2,MSN3	5	0.4
Q1:Q2	8 : 1	

TABLE II. PERFORMANCE SUMMARY

Parameters	This work	[1]*	[5]
Power Supply Voltage (V)	2.0	4.5	0.8
CMOS Technology (µm)	0.18	1.5	0.13
Reference Current (µA)	10	2.15	10
Power Consumption (µW)	80	N/A	N/A
Temperature Coefficient (ppm/°C)	170	214	21000
Temperature Range (°C)	–20 ~ 120	25 ~ 170	-10~90
Power Supply Dependency	3%	1.7%	10%

* Additional clock source required

IV. CONCLUSION

A new temperature compensation scheme for current references circuits was described. The proposed circuit exploits the threshold difference between a nominal MOSFET device and a thick oxide MOSFET transistor to generate the reference current without using resistors. The circuit was designed in a standard 0.18 µm CMOS process. Simulation results showed a temperature variation coefficient of 170 ppm/°C for the output current across a temperature range of –20 °C to 120 °C and an output current variation of 3% across a supply range of 2 V to 3 V. The results clearly illustrate that the proposed circuit is well suited to provide both cost effective and accurate current source across a wide range of PVT conditions and thus can be integrated into future analog or digital circuits.

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