A Novel High-Speed and Low-Power Negative Voltage Level Shifter for Low Voltage Applications

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***Abstract*—A novel high-speed and low-power negative level shifter suitable for low voltage applications is presented. To reduce the switching delay and leakage current, a novel bootstrapping technique is designed for the level shifter. Furthermore, a pull-down driver is proposed to have high driving capability under different operation modes. The circuit has been designed in 130nm 1.5V/5V triple-well CMOS technology with a nominal power supply V_{DD} of 1.5V and a negative voltage of -4.5V. Simulation results show that the switching delay and power consumption have been significantly reduced by roughly 62% and 65%, respectively. In addition, the proposed level shifter realizes a wide operation margin with a lower V_{DD} compared to conventional implementations.**

I. INTRODUCTION

A negative level shifter is used to convert a positive input signal with swing from ground (Gnd) to a positive voltage V_{DD} into a negative output signal with swing from Gnd to a negative high voltage V_{NN} ($|V_{NN}| > V_{DD}$). Negative level shifters are widely used in various applications such as standby mode activation in SoC systems [1], ESD protection [2], and especially in the flash memories for F-N tunneling erase operation of memory cells [3][4]. Conventionally, negative level shifters are designed with cross-coupled structure or feedback structure [4-7]. However, as V_{DD} lowering below 1.5V, the contention between the pull-up transistors and pull-down transistors becomes very serious during the transient switching, leading to an increased switching delay and large dynamic power consumption [4]. Therefore, high-speed and low-power negative level shifters are of great importance in low voltage applications.

In this paper, a novel negative level shifter is presented with the proposed bootstrapping switch and pull-down driver. The bootstrapping switch is able to reduce the transient time and dc current leakage. Consequently, the level shifter achieves high performance and low power consumption. For single voltage supply systems, the negative high voltage is generated by charge pump circuits, which will decrease to Gnd level in standby mode, a pull-down driver is also proposed to achieve high driving capability in both normal mode and standby mode.

This work is supported by the National Basic Research Program of China (No. 2006CB302700) and the National Nature and Science Funding (No. 60876076).

II. CONVENTIONAL NEGATIVE LEVEL SHIFTERS

A. Conventional Negative Level Shifter Type-1

The conventional negative level shifter, which consists of two serially connected cross-coupled level shifters, is shown in Fig. 1(a) [6]. The first level shifter receives a signal with swing from Gnd to V_{DD} and provides a signal with swing from a negative voltage V_{NN} to V_{DD}. The second level shifter receives the output of the first level shifter and provides a signal with a swing from V_{NN} to Gnd. The cross-coupled NMOS load in the first level shifter is used to perform positive feedback action which results in fully V_{NN} voltage in internal nodes. During every input signal transition, the pull-up PMOS transistors MP1 and MP2 have to overcome the NMOS latch action before the output state changes. The current driving capability of the pull-up PMOS transistors is determined by the overdrive voltage and the W/L ratio. The overdrive voltage is mainly affected by the regular supply voltage V_{DD}. As V_{DD} scaling down, the pull-up driving capability is reduced dramatically, leading to the increase in the transient time and dc current leakage. To maintain adequate driving capability, the size of MP1 and MP2 has to be much larger than MN1 and MN2, resulting in large silicon area.

B. Conventional Negative Level Shifter Type-2

Fig. 1(b) shows another negative level shifter based on feedback structure [7]. Instead of using two serially connected level shifters, this negative level shifter uses an inverter to switch the output voltage. Serious contention between the pull-up transistors and pull-down transistors also exists in this level shifter. It can be seen that during the input transition, the gate-source voltage of MP1 is V_{DD} while the maximum gate-source voltage of MN1 is $|V_{NN}| + V_{DD}$. Supposing V_{DD} is 1.5V and V_{NN} = -4.5V, the relative small current driving capability of the pull-up transistors makes it difficult to overcome the pull-down NMOS latch and change the output state. Another drawback of this level shifter is no pull-down driving capability in standby mode. In standby mode, the input signal IN goes low, the negative voltage V_{NN} will decrease to Gnd level since charge pump circuits stop working. Under this condition, the invert at the output stage acts as a triple gate and

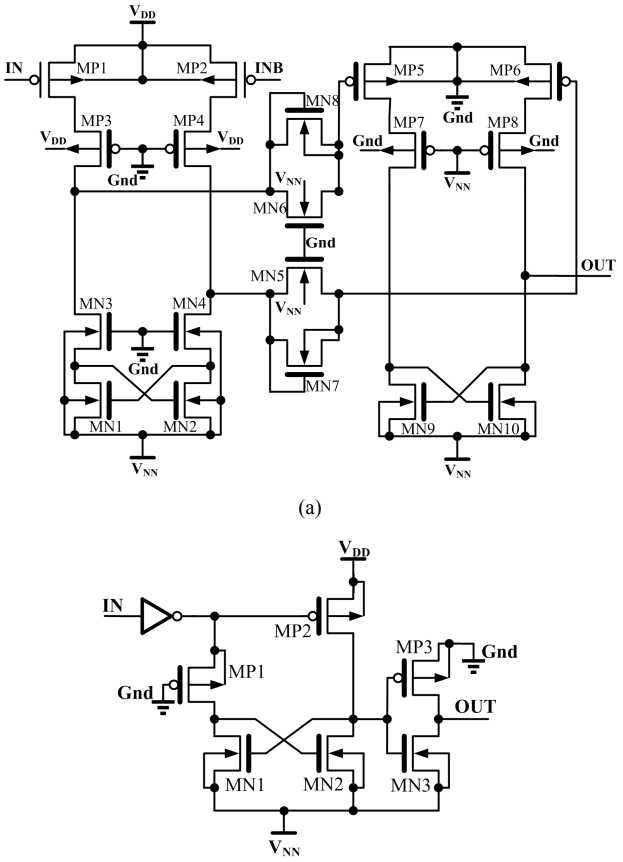

Fig. 1. Conventional level shifter (a) type-1 [6] and (b) type-2 [7]

the output node OUT is floating. Hence, there is no dc path to ground to drive the next stage.

Furthermore, both conventional negative level shifters above have scaling limitation. As the transistor dimensions shrink aggressively, the threshold voltage becomes difficult to scale down with the supply voltage V_{DD} [4]. In GSMC 130nm embedded flash memory process, the high threshold voltage of the high voltage (HV) transistor is comparable to half of V_{DD}. Hence, the operation margin of the level shifter is further reduced, and this feature is not suitable for wide range voltage application. It is possible to enhance the driving capability by increasing the W/L ratio of pull-up transistors, however, that also increases the parasitic capacitances, the switching noise caused by gate-drain coupling, and the silicon area.

III. Proposed Negative Level Shifter

The proposed negative level shifter is composed of two bootstrapping switches, a cross-coupled level shifter, and a pull-down driver of the output stage. Fig. 2 shows the schematic of the proposed bootstrapping switch which targets to enhance the drivability of pull-up transistors. C_{boost} is the bootstrapping capacitance; MN2 is the precharge transistor, and MP1, MP2, MN1 form a CMOS inverter to switch the output. It needs to be pointed out that MN1 and MN2 are triple-well NMOS transistors and should be planted in a stand-alone p-well to isolate from other NMOS transistors, since their bulk node N_1 is fluctuant during transient operation. As a result, a parasitic capacitance C_{ppw} is formed between the p-well and deep n-well. C_{load} is the load capacitance on the output node BOOT. According to the values of C_{ppw} (which depends on the size of MN1 and MN2) and C_{load}, the proper C_{boost} value is selected in order to achieve the required voltage level. The transistor MP2 biased at Gnd is able to relax the gate-drain voltage stress of MP1. The detailed operation of the proposed bootstrapping switch is described below.

When the input signal IN is low, the transistor MN1 is cut off and MP1 turns on, pulling the output node BOOT up to V_{DD}. As a result, node N_1 is pulled down to Gnd through the feedback transistor MN2.

When IN goes high, MN1 immediately turns on while MP1 is cut off. As a result, the output node BOOT is directly connected to node N_1, thereby BOOT is discharged by MN1 and MN2.When the voltage on node BOOT falls down to the threshold voltage of MN2, MN2 is cut off and node N_1 is isolated. At the same time the node N_2 changes from V_{DD} to Gnd. In this way, the node N_1 is boosted down by C_{boost}. The main capacitances connected to node N_1 are C_{boost}, C_{ppw}, and C_{load}. Other parasitic capacitances on node N_1 are small and their effect can be negligible compared to main capacitances. With the charge preservation on node N_1, the value of its potential V_1 can be expressed as:

$$V_1 = -V_{DD} \times \frac{C_{boost}}{C_{boost} + C_{ppw} + C_{load}} \tag{1}$$

After the boost operations, the potential on output node BOOT is almost equal to the voltage of V_1. During the transient time of switching, MN2 slightly discharges the bootstrapped level of node N_1, because MN2 remains on until the voltage of node BOOT is low enough to cut off MN2. But the charge lost through MN2 is much less than the total charge on N_1.

From Fig. 2, it can be seen that the maximum voltage stress applied in all the transistors is no more than V_{DD} except MN1. Therefore, MN1 has to be a HV transistor and other transistors are V_{DD} transistors.

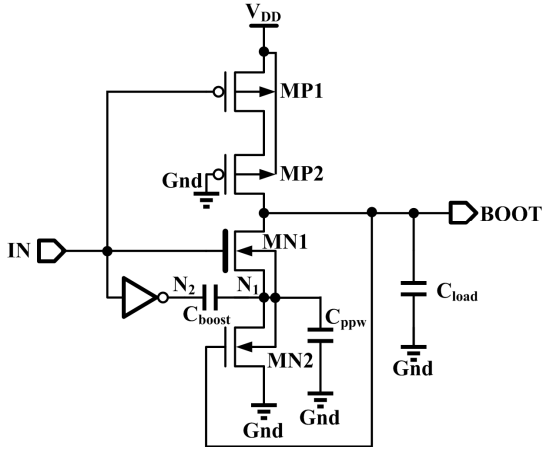

Fig. 2. Proposed bootstrapping switch

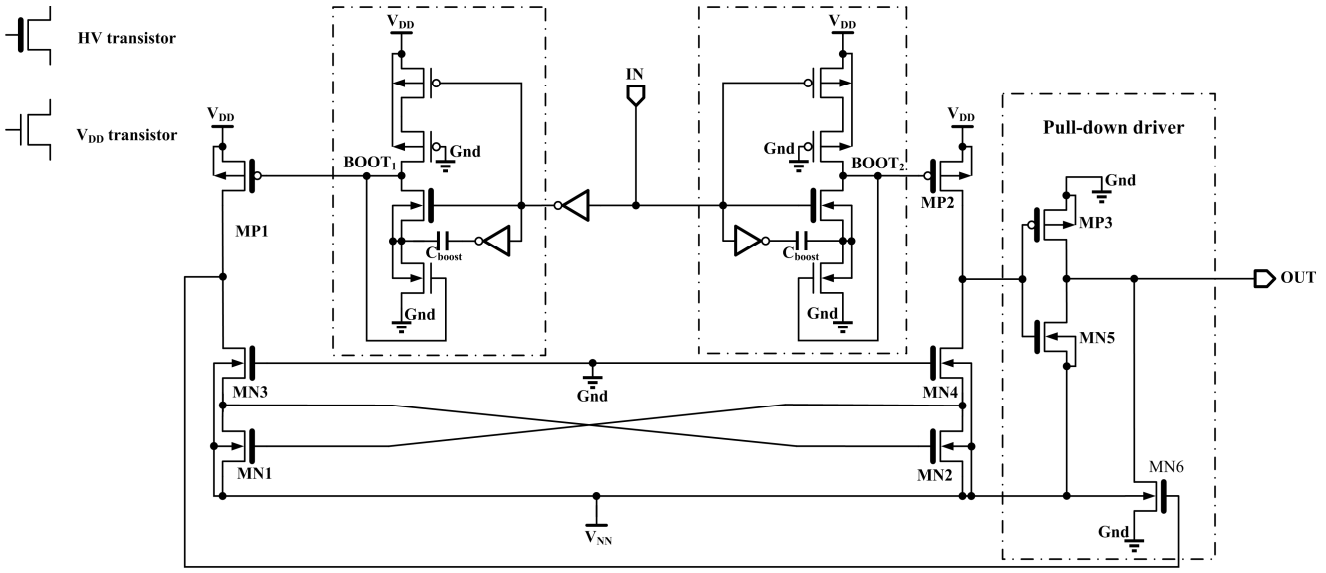

Fig. 3. Schematic of the proposed negative level shifter

Fig. 3 illustrates the proposed negative level shifter based on the bootstrapping switch. The bootstrapping switches receive the input signal IN with swing from Gnd to V_{DD} and provide a bootstrapped signal with swing from $-V_{DD}$ to V_{DD}, and then the cross-coupled level shifter receives the output signal of the bootstrapping switches and provides a signal with swing from V_{NN} to V_{DD}. Finally, the pull-down driver provides a signal with swing from V_{NN} to Gnd.

With the bootstrapping switches, the maximum gate-to-source voltage of the pull-up transistors increases from V_{DD} to $2V_{DD}$, thereby the operation margin of the proposed negative level shifter is improved. In addition, the transistors MN3 and MN4 are biased at Gnd to reduce the contention caused by the pull-down transistors MN1 and MN2. It can be obtained that the gate-to-source voltage of the pull-down transistors is reduced from $V_{DD}+|V_{NN}|$ to $|V_{NN}| - V_{THN}$ (where V_{THN} is the threshold voltage of HV NMOS transistor) during the transient switching. As a result, the driving capability of pull-up transistors is doubled and the contention between pull-up transistors and pull-down transistors is reduced dramatically, therefore, the proposed negative level shifter is able to improve the switching delay as well as dynamic power consumption.

In the pull-down driver, MN5 is used to switch the voltage of the OUT node to V_{NN} while MP3 and MN6 are used to switch the voltage of the OUT node to Gnd. It is worth noting that the negative level shifter should have adequate pull-down driving capability in both normal mode and standby mode. In normal mode, the charge pump generates the high negative voltage V_{NN}. The voltage of the node OUT can be pulled up to Gnd mainly through the transistor MP3 due to its large driving capability, whereas transistor MN6 has little driving capability owing to the serious body effect. In standby mode, the charge pump stops and V_{NN} is decreased to Gnd level. Under this condition, MP3 is cut off while MN6 turns on and pulls down the node OUT to Gnd.

Compared to conventional level shifters, additional layout area for the bootstrapping switches is needed in the proposed negative level shifter. However, since most transistors in the bootstrapping switches are V_{DD} transistors, the area penalty is smaller than that of large HV transistors in conventional level shifters under low V_{DD}. Therefore, the proposed negative level shifter is suitable for low voltage applications.

IV. Simulation Results and Discusion

The proposed negative level shifter has been designed in GSMC 130nm 1.5V/5V triple-well CMOS technology. Fig. 4(a) shows the HSPICE simulated waveforms of the bootstrapping switch with V_{DD}=1.5V. From the waveform, it can be seen that the voltage of the output node BOOT swings from 1.5V to -1.3V when IN goes from low to high. In this way, the swing voltage of the gate input for the pull-up transistors is nearly doubled, and their drivability can be dramatically enhanced. The output waveform of the proposed level shifter is also shown in Fig. 4(b), it is clear that the proposed negative level shifter is able to convert the input signal with swing from Gnd to regular power supply voltage 1.5V into a negative output signal with swing from Gnd to a negative high voltage -4.5V.

To show the improvement of the proposed level shifter, performance comparisons are made between the proposed one and the conventional ones. Fig. 5 represents the results of the switching delay comparison under different supply voltages (V_{DD}). As shown in Fig. 5, the switching delay is significantly reduced by roughly 62% with the proposed level shifter at V_{DD} of 1.5V. This is because the current driving capability of pull-up transistors is enhanced with the bootstrapping technique and the contention between the PMOS transistors and NMOS transistors is significantly reduced. In addition, as V_{DD} lowers below 1.0V, the proposed negative level shifter has better operation margin compared to conventional ones.

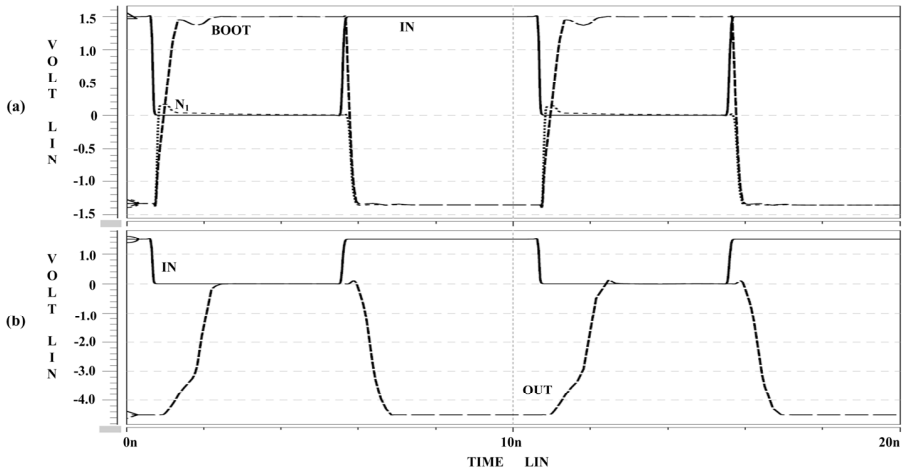

Fig. 4. Simulation waveforms of the proposed (a) bootstrapping switch and (b) negative level shifter

Fig. 6 illustrates the power consumption comparison results. In conventional level shifters, the power consumption increases rapidly at V_{DD} under 1.0V, which is caused by the dc current leakage from Gnd to V_{NN} during long transient switching. Hence, the power consumption on V_{NN} is dominant. In the proposed negative level shifter, the power consumption is significantly reduced by 65% at V_{DD} of 1.5V. This is because that the improvement of the switching delay reduces the dc current leakage between V_{NN} and Gnd during the transient switching. Furthermore, the proposed level shifter has a low power consumption feature at a wide range of supply voltage V_{DD}. The proposed negative level shifter is able to reduce the power consumption while keeping a high performance level in low voltage applications.

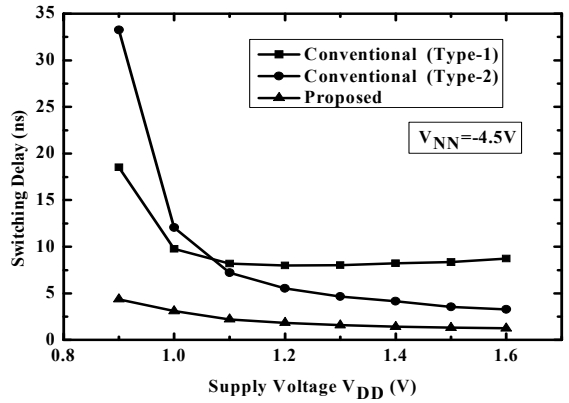

Fig. 5. Comparison of switching delay on different V_{DD}

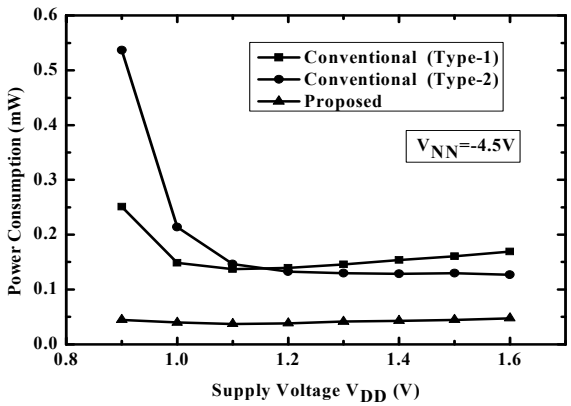

Fig. 6. Comparison of power consumption on different V_{DD}

V. CONCLUSION

In this paper, a novel negative level shifter is proposed to reduce the switching delay and dc leakage current. A bootstrapping switch is proposed to improve the drivability of pull-up transistors in the level shifter. Furthermore, a pull-down driver is designed to have high driving capability under different modes. Simulation results show that the proposed circuit achieves fast switching speed and low power consumption at V_{DD} lower than 1.5V.

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