A Low Jitter 2.125GHz Serial Link for Optical Transmission

Zhongyuan Hou[1], Junhua Liu[*2], Fan Yang[2], Xin Zhang[2]

1. Zhongyuan Hou
The Key Laboratory of Integrated Microsystems,
Peking University Shenzhen Graduate School,
Shenzhen, China
Email: houzhongyuan@pku.edu.cn

2. Junhua Liu, Fan Yang, Xin Zhang
Institute of Microelectronics
Peking University
Beijing, China
Email: junhua.liu@pku.edu.cn

***Abstract*— In this paper, a 2.125GBd 10bit Serialize/Deserialize (SERDES) system has been implemented, transmitter section and receiver section are capable of working simultaneously. A new architecture of CDR and PLL has been proposed. The same coarse loop is used in the PLL and CDR to set each digital control bits of VCO. And a pre-emphasis driver is utilized to compensate for the high frequency attenuation in channel. The measurement results show that SERDES has a RMS jitter of 28ps.**

I. INTRODUCTION

With rapid development of broadband data communications, the growing gap between on-chip gates and off-chip I/O bandwidth is reaching the critical proportions. Therefore, interconnects between chips often limit the performance of a system in application. Composed of dedicated serializer/ deserializer pairs, SERDES technology opens the door to tremendous increases in bandwidth vs. previous technologies. In the Fibre Channel, high-speed I/O links are key technological elements that determine the performance, physical footprint and power dissipation. Several specifications must be met by CDR circuits used in this application. [1]

To improve the noise performance, the loop bandwidth of CDRs should be small. However, it will result in a small capture range. In the literature work, the CDR without frequency acquisition loops might need either additional reference clock or off chip tuning [2]. In this paper, a new CDR architecture consists of two loops has been proposed — a coarse loop to set the digital control bits of the VCO, limiting the frequency to a narrow range, and a fine loop to retime the random data. Based on this CDR structure, a 2.125GBd receiver (RX) and transmitter (TX) systems for Fibre Channel are presented in this paper.

II. ARCHITECTURE

The proposed SERDES architecture is shown in Figure 1, which consists of two parts: transmitter and receiver.

In the transmitter section, the input data is at 106.25Mbps. The input latch accepts 10-bit wide single ended SSTL_2 parallel data at inputs TX [0:9]. Then A 10:1 multiplexer (MUX) serializes them into 2.125GBd serial data signal for application to the pre-emphasis driver stages. The pre-emphasis driver provide to boost purely the high frequency components of the signal, while leaving the low frequency components in their original state to compensate for the high frequency attenuation in channel. A phase locked loop (PLL) with 2.125GHz output frequency generates the reference clock for the multiplexer.

In the receiver section, the input selector is used to select the serial input data or parallel loopback data. A two-stage tree structure is used in the 1:10 demultiplexer (DEMUX), which processes the data from high speed serial data to lower speed parallel ones. The CDR unit is responsible for frequency and phase locking onto the incoming serial data stream and retime data to the DEMUX. Output driver transmits the signal to SSTL_2 voltage level. The transmitter section and receiver section is capable to work simultaneously. Some of these building blocks will be discussed as follows.

III. BUILDING BLOCK

A. CDR & PLL

Optical telecommunication transport standard such as Synchronous Optical Networks (SONET) and Synchronous Digital Hierarchy (SDH) require a narrow loop bandwidth to meet the jitter transfer specification. Clock and data recovery

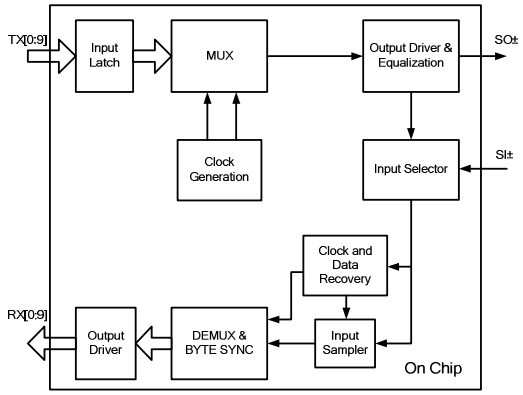

Figure 1 System Architecture

circuits designed is limited by the capture range of a simple phase-locked loop (PLL). For this reason, a coarse tuning structure is utilized to set the digital control bits of the voltage- controlled oscillator (VCO) switched capacitor array, which for frequency acquisition in addition to phase-locking, reducing the overall lock time. Since the coarse loop is disabled after frequency acquisition the digital circuitry remain relatively quiet during phase lock, and the high sensitivity of coarse control does not lead to high jitter.

A new architecture of BB-CDR and PLL has been proposed in Figure 2. In the proposed structure, the LC-tank VCO used in PLL loop and CDR loop is exactly the same, so the same coarse tuning loop can be shared in the PLL and CDR. A three-order PLL is implemented. And a low jitter 2.125Gbps bang-bang clock and data recovery circuit is proposed in this work. The CDR loop consists of two loops: a coarse tuning structure to set the digital control bits of the VCO, and a fine loop to drive the fine control voltage of the VCO retiming for random data, thereby presenting a low-noise control to VCO. A bang-bang phase detector has been implemented in circuit level design.

In the proposed design, the phase detector adopts traditional Alexander PD structure, shown in Figure 3. For monolithic implementation, bang-bang phase detector (PD) has excellent match between retiming latch and PD latch- allows for operation at highest latch toggle frequency. From the whole process describe above, it provides an approach to get the gain of nonlinear phase detector. As shown in Figure 4, the slope of the input/output characteristic of the PD together with the V/I converter approach zero is the bang-bang phase detector's gain [3]. Then,

$$K_{PD} = \frac{\alpha \bullet T}{2\pi}(\mu A / rad)$$

α denotes the slope of the curse approaching zero value.

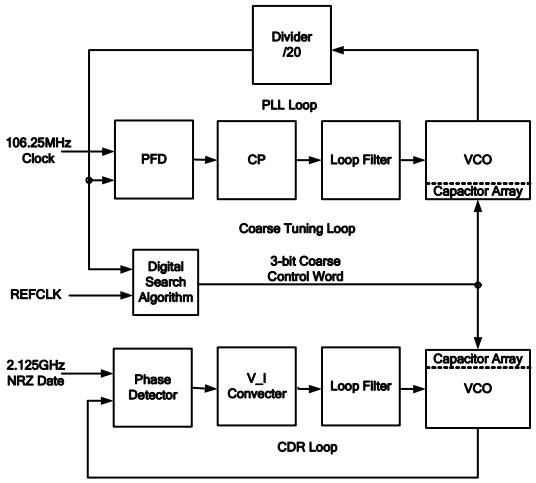

Figure 2 Clock and Data Recovery Unit

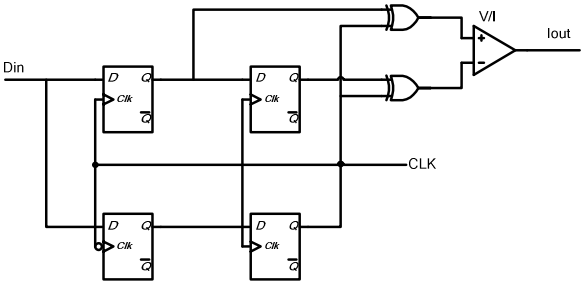

Figure 3 Alexander PD structure

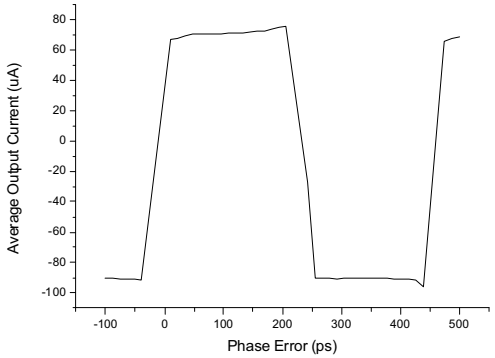

Figure 4 Simulated input/output characteristic of the PD together with the V/I converter

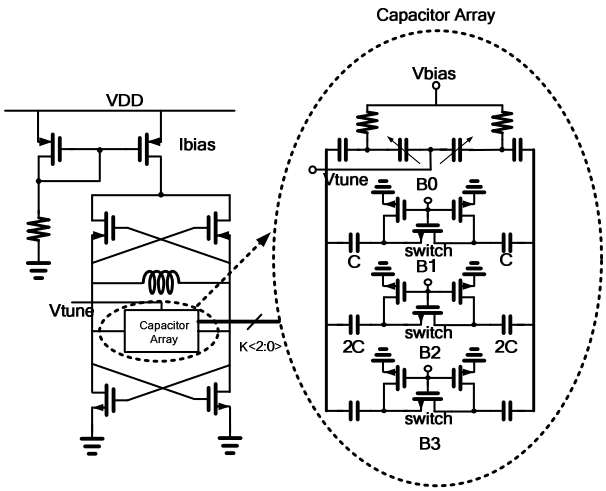

Figure 5 VCO Structure

Figure 5 shows the structure of negative impedance LC VCO. In order to obtain a wider frequency range, low phase noise and high linearity, the coarse tuning structure is utilized to control switched capacitor array to reduce the VCO gain in the circuit topology.

B. MUX & DEMUX

In SERDES system, the multiplier processes the data from n-bit lower speed parallel interface to high speed. In the proposed work, values of n which are multiples of 10 are useful for protocols which use 8B/10B coding (The 8B/10B encoder is generally implemented by logic outside the SERDES core [4]). As shown in Figure 6, the data serialize through two branches respectively, then output by a 2-1 selector. So the clock frequency of each branch can be reduced to half of original one. The 10-bit parallel data are divider into two 5-bit data and delayed appropriately by the synchronization block.

De-multiplier (DEMUX) transforms high speed serial data into n bit parallel one. In order to reduce the speed of module of the speed, we can use a similar principle of MUX structure. Figure 7 shows the block structure of DEMUX. Each DFF generates half-cycle delay, so the input signal serial is sampled every half cycle. Then the sampling clock frequency of DEMUX is reduced to the half speed of the 2.125GHz. In addition, a divider-by-5 is used to control the parallel data to recognize comma character. When a comma character is detected, it would realignment of the parallel data.

The SCL DFF and 2:1 selector is adopted in both MUX and DEMUX.

C. Output Driver with Pre-emphasis

High speed signals transmitted over a channel tend to suffer from high frequency attenuation, which makes it difficult for the receiver to interpret the information. The principle solution of pre-emphasis is to provide a method of boosting purely the high frequency components of the signal,

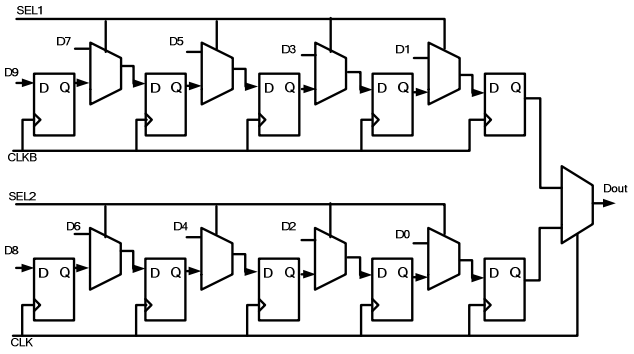

Figure 6 Block Structure of MUX

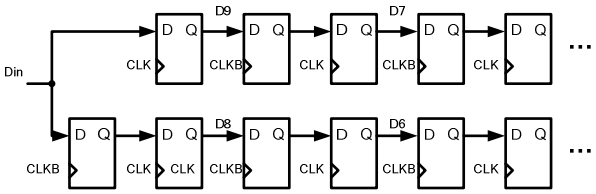

Figure 7 Block Structure of DEMUX

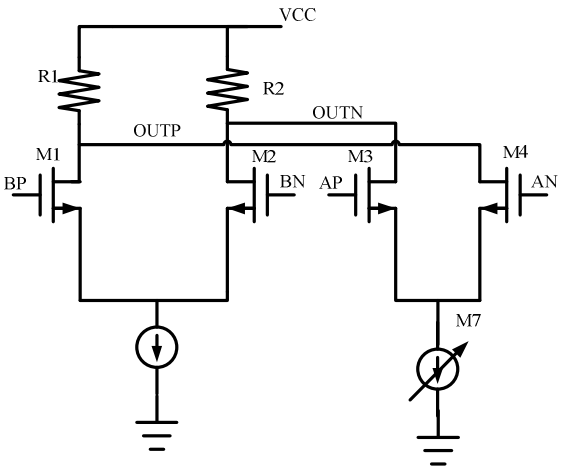

Figure 8 Schematic of Output Driver

while leaving the low frequency components in their original state.

As shown in Figure 8, the signal of B is one cycle delay of A. The output of the pre-emphasis driver is the different between the two signals. So the output driver with pre-emphasis circuit acts as encoding a symbol into a current or voltage for transmission— low-to-high and high-to-low signal transitions on output have greater amplitude than low-to-low and high-to-high signal transition. The rail current of A can be adjusted for pre-emphasis level control.

IV. EXPERIMENT RESULTS

The SERDES circuits have been fabricated in a 0.18-μm CMOS technology. Figure 9 shows a photo of the die, which measure 3.0×3.0 mm^2. The setup of measure the proposed eye diagram is shown in Figure 10. Figure 11 depicts the SERDES output waveforms under locked condition in response to a

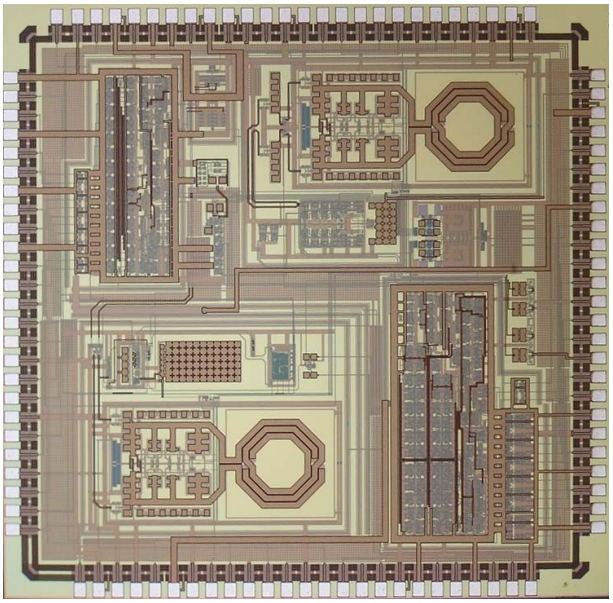

Figure 9 Chip micrograph of proposed SERDES

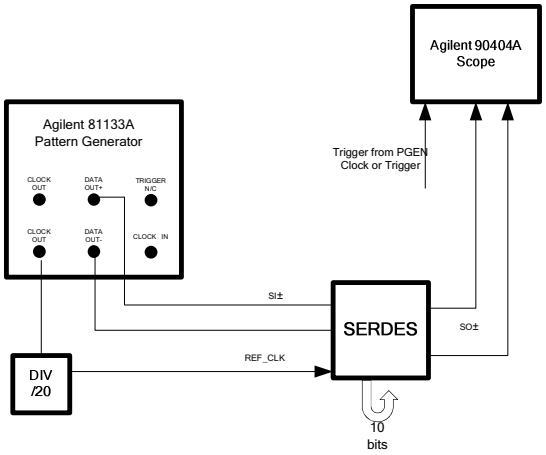

Figure 10 Test Setup

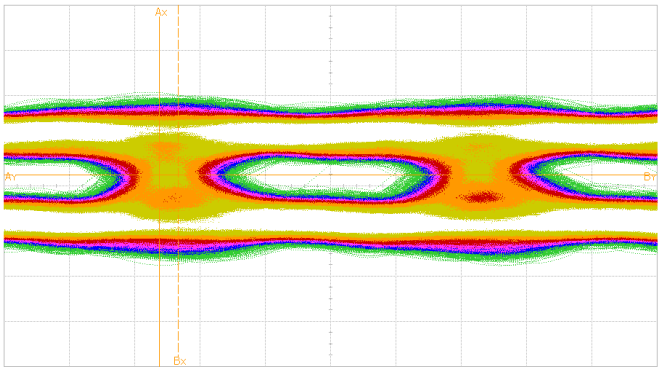

Figure 11 Serial output eye diagram with Tx pre-emphasis off

pseudorandom sequence of length 2^{31}-1. Figure 11 shows the deterministic RMS jitter 28ps.

V. CONCLUSION

In this paper, we proposed 2.125GBd transmitter and receiver architecture. A low jitter 2.125GBd bang-bang clock and data recovery circuit is presented in this work and a new architecture has been adopted which consists of two loops: a coarse loop to set the digital control bits of the VCO, pulling the frequency to a narrow range, and a fine loop to retime for random data. The measurement results show that SERDES has a RMS jitter of 28ps, and conforms to the SERDES specifications correctly.

REFERENCES

[1] K. Iniewski, R. Badalone, M. Lapointe, M. Syrzycki, "SERDES Technology for Gigabit I/O Communications in Storage Area Networking", IEEE IWSOC'04, 2004.

[2] Ming-ta Hsieh and Gerald E. Sobelman, "Architectures for Multi-Gigabit Wire-Linked Clock and Data Recovery", IEEE circuits and SYSTEMS, fourth quarter 2008.

[3] Jri Lee, Kenneth S. Kundert and Behzad Razavi, "Analysis and Modeling of Bang-Bang Clock and Data Recovery Circuits", IEEE solid-state Vol.39. No.9, 2004, pp. 1571-1580.

[4] David R. Stauffer and etc, "High Speed SERDES Device and Applications", Springer, 2008.