20.4 An 8.4mW/Gb/s 4-Lane 48Gb/s Multi-Standard-Compliant Transceiver in 40nm Digital CMOS Technology

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The bandwidth limitation of existing backplanes has become an obstacle to meeting the increasing demand for high-data-rate wireline transmission. In order to compensate for this limitation, TX pre-emphasis, RX continuous-time linear equalizer (CTLE) and DFE are necessary [1,2]. This work presents a 4-lane transceiver implemented in 40nm CMOS technology that operates over a wide range of data rates from 1 to 12Gb/s (48Gb/s aggregated) using NRZ coding. The supply voltages are 0.9V and 1.8V. An algorithm is developed to adapt the CTLE and DFE to cancel the channel ISI. No inductors are used in the design and ring oscillators are used for both the TX and RX clock generation. This provides a wide frequency-tuning range, small layout area, and high design portability. With extensive use of digital programmability this transceiver is capable of meeting specifications of different standards, such as PCIe, SATA, and 1 to 10Gb/s Ethernet.

The RX front-end (Fig. 20.4.1) consists of a programmable attenuator (ATT), a CTLE and a 5-tap DFE that is followed by a CDR and a de-serializer. The ATT uses an AGC loop to set the desired signal level at the input of the DFE. A sign zero-forcing (S-ZF) adaptation algorithm with pattern filtering is used to adapt the CTLE and the DFE taps. The error signals for the S-ZF algorithm are generated from the same comparators used by the CDR, eliminating the need for additional comparators for adaptation. In addition, during test and debugging modes one of the edge comparators is re-used as an on-chip eye-monitor. The CDR is based on a half-rate bang-bang phase detector and a digital loop filter consisting of both a proportional and an integral path. The proportional signals from the phase detector directly control the CDR VCO. The integral path incorporates an up/down counter, which provides control over loop stability and programmability for optimum performance at different data rates. The VCO is based on a four-stage current-controlled ring oscillator with a 1 to 6GHz tuning range. The wide bandwidth of the bang-bang CDR loop significantly suppresses the ring oscillator inherent phase noise. The VCO coarse tuning is achieved by switching load capacitors at the delay cell outputs. The VCO fine control is achieved through a current DAC. At start up, digital calibration uses the same current DAC to pull the VCO frequency close to the locking condition. After that, the control is switched to real time CDR closed loop. The frequency error that the CDR loop can lock to is within ±5000ppm.

The ATT is realized using a passive capacitive divider (Fig. 20.4.2). A wide tuning range is achieved by using both programmable series and shunt capacitors. Switches are used to reconfigure series capacitors as shunt capacitors, which allows for a compact implementation. The CTLE is a 3 stage equalizer. Each stage consists of a differential-pair with an NMOS active inductor load (Fig. 20.4.2). Using the active inductors improves the portability of the design to other technologies/metal stacks. The DFE (Fig. 20.4.2) employs four low-power comparators: comprised of two data and two edge comparators. Each comparator contains a main branch, an identical offset branch, and 5 tap branches with tap 1 branch being ½ the main branch size and taps 2 to 4 being ¼ the main branch. This scaling helps reduce the DFE power consumption. The comparators use a common-source topology to allow for high-speed operation from a 0.9V supply. This requires the input common-mode to be accurately set, which is achieved through the CMFB in the CTLE. Furthermore, this common-mode reference voltage is used to set the mid-voltage of a resistive ladder which is used to generate the offset and tap voltages.

The DFE coefficients are adapted to minimize the ISI at the zero-crossings of the received data, which also improves the x-opening of the received eye, thus reducing the recovered clock jitter. The error signal for adaptation is the edge comparator output. However, the error signal is only used for specific patterns, which significantly simplifies the calibration procedure and allows calibrating the taps independently. Similar to the approach outlined in [3] for a 1-tap DFE, the approach used here selects the appropriate patterns to adapt each tap. However, as opposed to using 2 different patterns per tap and obtaining the error signal by combining the individual error signals from each pattern, the technique used here uses a single pattern per tap and computes the error signal from multiple edge decisions for a lone 1 or 0 following these patterns. This same technique is also used to adapt the CTLE by choosing a pattern that generates an error signal that is proportional to the sum of the first 5 edge-ISI components. Compared to a SS-LMS algorithm, this algorithm produces much less noise on the tap weights and does not diverge in the case of no transitions. The same technique was also extended to adapt the far-end Tx pre-emphasis taps by transmitting back these error signals.

The TX driver is based on an H-bridge architecture (Fig. 20.4.3), which uses a replica circuit and a buffer to set the driver common-mode output voltage. This method of common-mode control is essential for PCIe receiver-detect requirements. The output driver consists of sixteen identical driver/pre-driver cells placed in parallel. Each of these cells is controlled individually to facilitate four-tap TX FFE equalization (1-tap pre-cursor, 1 main tap, 2-tap post-cursor) and slew-rate control. Each cell includes a MUX that selects between the current and delayed data to achieve up to 3dB pre-emphasis and/or 12dB de-emphasis. The slew rate programmability is achieved by individually controlling the delay of the pre-driver cells. The differential output amplitude is programmable from 200 to 1000mV$_{pp}$, which is controlled by changing the bias of the H-bridge current sources. The VCO used for the TX CMU is also based on a four-stage ring oscillator architecture. To minimize the TX output jitter an on-chip regulated supply is used for the VCO and the TX clock path. Similar to the CDR VCO, the CMU VCO is calibrated at start up to achieve optimum tuning range for the desired data rate.

Figure 20.4.7 shows the die micrograph. The measured insertion and retun loss of a 52 inch FR4+ backplane is shown in Fig. 20.4.4. This channel is used to generate the RX bathtub curves for an 8Gb/s PRBS31 before and after the CTLE/DFE adaptation. It clearly shows the effectiveness of the adaptation in opening the eye at the input of the sampler. Furthmore, the RX performance is evaluated by measuring the BER for 2.5 to 11.3Gb/s PRBS31 inputs after 12 to 52 inch of the backplane. The test for 12Gb/s data is missing due to equipment limitation. The on-chip eye monitor is used to measure the internal eye after the CTLE as it is shown in Fig. 20.4.4. This is used to verify the results of the ATT and CTLE adaptation. The measured TX output eye diagram at 12Gb/s PRBS31 is shown in Fig. 20.4.5; the eye height is 660mV$_{pp}$. Figure. 20.4.6 provides the measured performance summary.

Acknowledgment:
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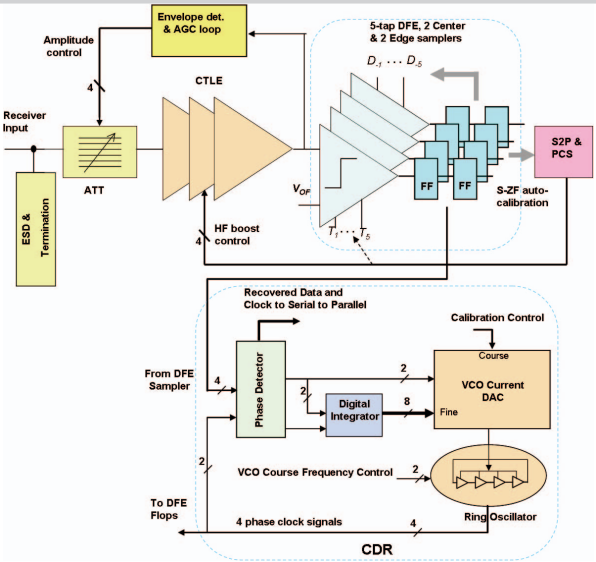

Figure 20.4.1: Receiver block diagram.

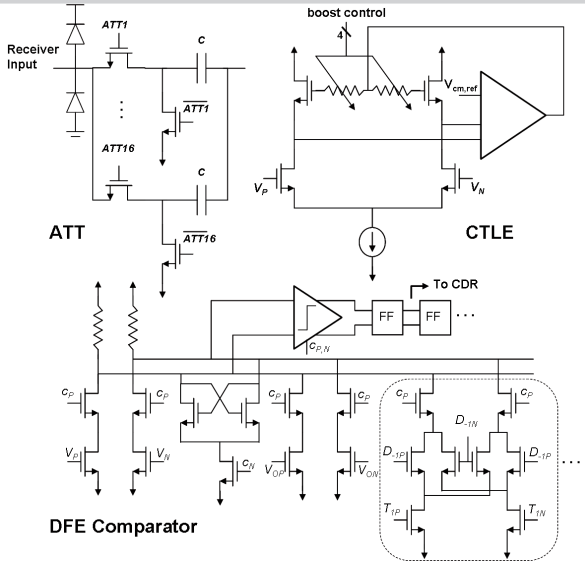

Figure 20.4.2: Receiver front-end schematics.

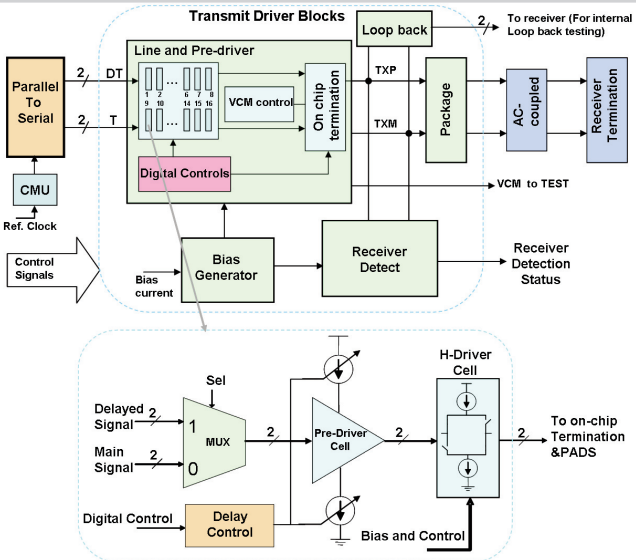

Figure 20.4.3: Transmitter block diagram.

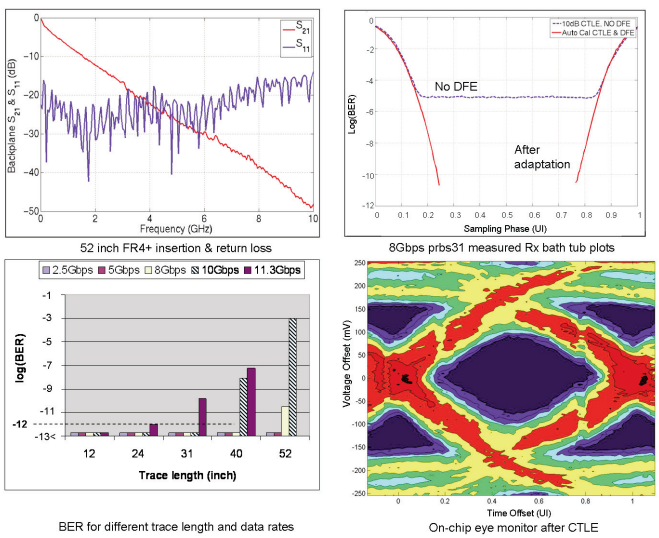

Figure 20.4.4: Receiver performance.

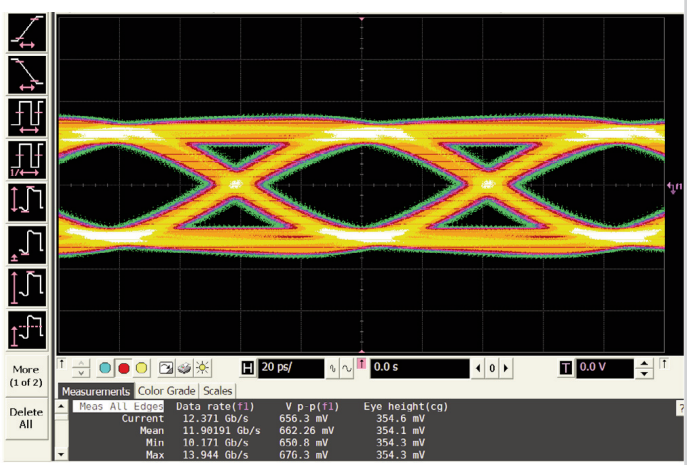

Figure 20.4.5: Transmitter performance at 12Gb/s.

Technology		40nm CMOS
Package		Flip-chip BGA
Supply voltage	VDDA	0.9V
	VDDHA	1.8V
Speed		1-12Gbps
DFE taps		5
Tx FIR taps		4
Power per lane at 10.3125Gbps	800mV output differential swing	87mW
Power per lane at 8Gbps	800mV output differential swing	73mW
Open loop VCO phase noise @ 5GHz (10Gbps) (No LC tank)	1MHz offset	-80dBc/Hz
Tx driver jitter @10Gbps	800mV output swing	1.4ps (rms)
Area	Lane	360um x 750um
	CMU	180um x 880um

Figure 20.4.6: Transceiver measured performance summary (per lane).

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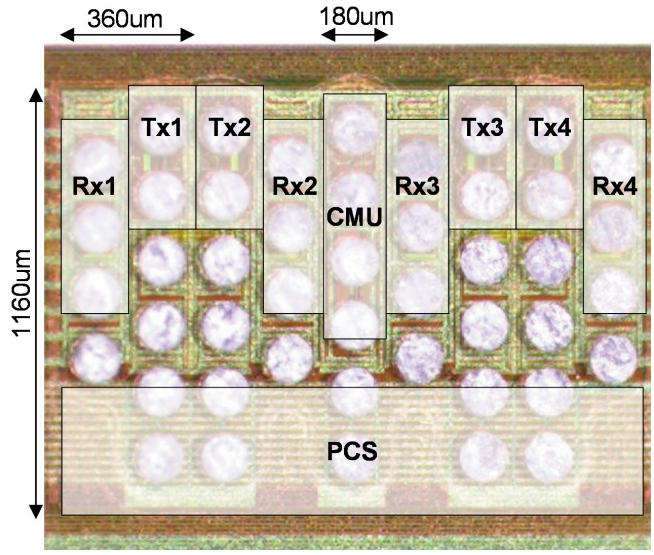

Figure 20.4.7: Die photo.

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