An On-Chip Calibration Technique for Reducing Temperature and Offset Errors in a Programmable Voltage Reference

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***Abstract*—We present an on-chip calibration method for reducing offset errors and variations of the temperature coefficient of the output voltage of a programmable voltage reference. The offset calibration can be performed by an automatic on-chip calibration procedure or by directly programming an appropriate calibration value via a Three-Wire-Interface. Variation of the temperature coefficients can be compensated by taking into account the measured output voltage at two arbitrary temperatures during e.g. wafer sort and final test, and setting a corresponding calibration value.**

Extensive simulations and measurements indicate that the error due to variations in temperature coefficients can be reduced by 40% and the overall offset error can be improved up to 90% of the uncalibrated voltage reference.

***Keywords*-voltage reference; calibration; temperature coefficient; offset voltage; programmable**

I. Introduction

Voltage references are important building blocks in many of today's electronic circuits. Most analog-to-digital converters or radio transceivers, for instance, rely on stable reference voltages.

In addition to changing environmental conditions (temperature, supply voltage,...), mismatch and process variations, which manifest in e.g. resistor mismatch, offset voltages in operational amplifiers etc., cause unavoidable temperature and offset errors of reference voltages.

Recent advances in miniaturization and therefore shrinking transistor/resistor dimensions make it even harder to design inherently accurate voltage references. For this reason, we present a programmable voltage reference whose inherent variations (viz. offset error and poor temperature coefficient) can be reduced during testing of the ASIC. We further propose a semiautomatic calibration process which minimizes the amount of test time needed for the calibration procedure.

II. Circuit Description

The proposed voltage reference (Fig. 1), which was realized in a $3.3V$, 250nm CMOS process, consists of three main blocks:

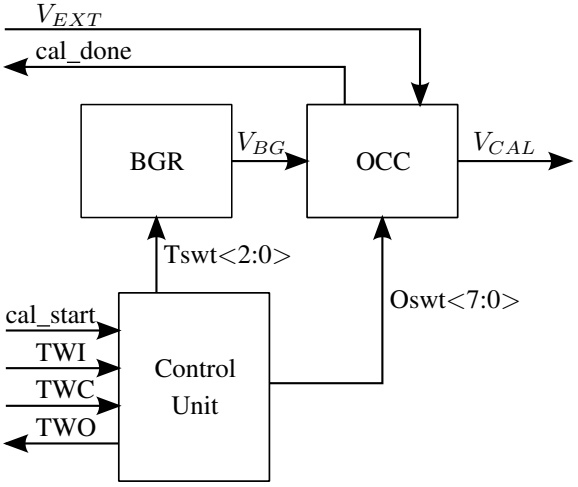

Figure 1. Block diagram of the proposed programmable voltage reference

A. Bandgap Reference - BGR

The bandgap voltage reference (BGR), based on [1], with adjustable temperature coefficient (Fig. 2): It provides an output voltage of $V_{BG} \approx 1.22V$. The temperature behavior can be controlled via three digital ports *Tswt<2:0>*. The output voltage can be described by

$$V_{BG} = \underbrace{V_{xD}}_{\text{neg. Tempco}} + \underbrace{V_T \cdot \ln(x)\,(1 + R_2/R_{swt})}_{\text{pos. Tempco}} \qquad (1)$$

V_{xD} is the diode voltage, $V_T = kT/q$ the thermal voltage and x the size factor of both diode-connected BJTs.

The change of the temperature coefficient is realized by changing the resistor value of R_{swt}. It consists of one fixed part (about $8k\Omega$) and three binary weighted smaller resistors. Depending on the chosen temperature compensation T_{swt}, the three smaller resistors can by bypassed by low ohmic transmission gates. [2]

B. Offset Calibration Circuit - OCC

The offset calibration circuit OCC (Fig 3) increases the voltage V_{BG} to the desired output voltage and compensates for offset errors of the programmable BGR. According to

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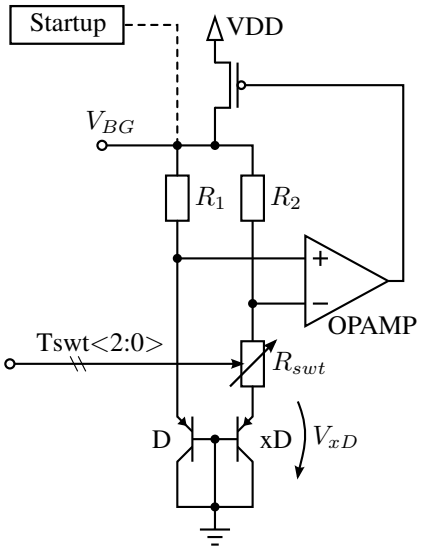

Figure 2. Bandgap reference with programmable temperature coefficient

the resistors R_{Oi}, V_{CAL} can be set between $V_{CAL,max}$ and $0V$. The highest output voltage was chosen to be $V_{CAL,max} = 2.5V$ in the design at hand, but can be increased depending on e.g. available supply voltage and fabrication process etc. In the implemented design, V_{CAL} was set to $2.0V$. The offset compensation can be controlled via eight digital ports *Oswt<7:0>*. The calibration range of the OCC is approximately $\pm 100mV$, which is sufficient enough to compensate virtual all possible offset variations of the programmable BGR [2], [3].

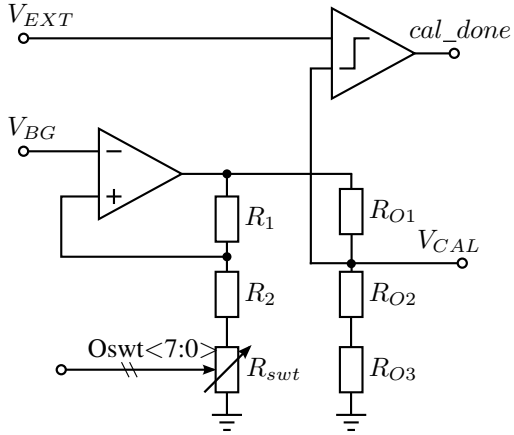

Figure 3. Offset calibration circuit and comparator

In addition to the offset calibration capabilities, the OCC includes a comparator which compares an externally provided reference voltage V_{EXT} with the internally generated voltage V_{CAL} and is used during the automatic on-chip offset calibration.

C. Control Unit

The control unit executes the automatic offset calibration and provides a communication interface through a Three-Wire-Interface (ports TWI, TWO and TWC). It can be used to manually set each calibration state (T_{swt} and O_{swt}). This is especially useful for debugging or if the offset calibration has to be done manually.

The automatic on-chip offset calibration can be started via port cal_start which triggers a counter that continuously increases the value of *Oswt<7:0>* until the comparator detects that the internal voltage V_{CAL} exceeds the external voltage V_{EXT}. The calibration stops at this point and the output cal_done is set.

As an alternative to the simple counter, which continuously increases the output voltage, a more complex method e.g. a successively approximation algorithm [4] can be used. It provides results much quicker (which saves test time), but also increases the requirements of the comparator and the overall reference circuit regarding parasitic oscillations.

III. Calibration Procedure

The overall calibration process consists of two main parts. The first step (Fig. 4) is executed at an arbitrary temperature T_1, for example $T_1 = 80°C$ during wafer sort. The second, more complex part (Fig. 5) is done at a second arbitrary temperature T_2. This temperature should be as different as possible to T_1. As an example, it can be done during final testing of the chip at $T_2 = 40°C$.

A. Part 1 at T_1

The first calibration step is used to measure all values of the reference output voltage V_{CAL}, regarding the temperature calibration values T_{swt} at a default calibration value of the offset compensation O_{swt} at a constant temperature T_1. The value of O_{swt} is arbitrary, but has to be the same throughout the entire calibration. The whole process is shown in the flowchart in Fig. 4. In the proposed voltage reference, T_{swt} consists of three control bits, therefore eight data pairs, consisting of the value of T_{swt} and V_{CAL}, and the according chip number have to be saved.

These data points correspond to the measured data point at $80°C$ in the example shown in Fig. 6.

B. Part 2 at T_2

The second part of the calibration is done at temperature T_2. First of all the measurements of part one are repeated. These measurements correspond to the measurement data points at $40°C$ in the example shown in Fig. 6. With the help of this measurement and the measurement from part one, the optimal temperature compensation can be processed:

$$T_{swt,opt} = \left\{ T_{swt} \;\middle|\; \min_{i=0..7} |\Delta V_{CAL,i}| \right\} \quad (2)$$

$$\Delta V_{CAL,i} = \left(V_{CAL}\,|_{T_1, T_{swt}=i} - V_{CAL}\,|_{T_2, T_{swt}=i} \right) \quad (3)$$

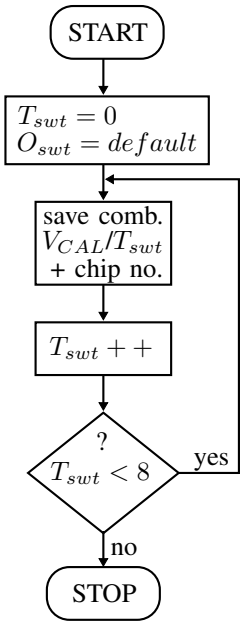

Figure 4. Flowchart of the first part of the calibration sequence which measures all combinations of V_{CAL} and T_{swt} at a given temperature T_1

The value of T_{swt} which results in the smallest difference of output voltages V_{CAL} at temperatures T_1 and T_2 is selected. In the example shown in Fig. 6, the value $T_{swt} = 2$ is chosen (curve marked with 'O').

After processing and setting $T_{swt,opt}$, the calibration of the temperature coefficient its done. It is important to perform the temperature calibration before the offset calibration, because it affects the overall offset of the voltage V_{CAL}.

The offset calibration is started by setting cal_start. The control unit sets O_{swt} to zero (i.e. $V_{CAL} = V_{CAL,min}$), and continuously increases the value of O_{swt} and therefore the value of V_{CAL} until it reaches the externally provided voltage V_{EXT}. This transition is indicated by the comparators output voltage cal_done going high. It terminates the offset calibration.

The voltage V_{EXT} can be provided through a dedicated pad, or like in the given design, through a probe pad. The determined calibration values for T_{swt} and O_{swt} can then be saved on any kind of nonvolatile on-chip memory. In the given design laser fuses are used to permanently save the calibration states.

IV. Measurement Results

An example for how far the temperature coefficient of the BGR can be changed is presented in Fig. 6. It shows the output voltage of the reference over a temperature range from -40 to $+125°C$. The line marked with '*' represent the uncalibrated output, the line with 'O' shows the output voltage with optimized temperature coefficient.

Fig. 7 shows measurement results of 38 different voltage references. Eight are manufactured at nominal process

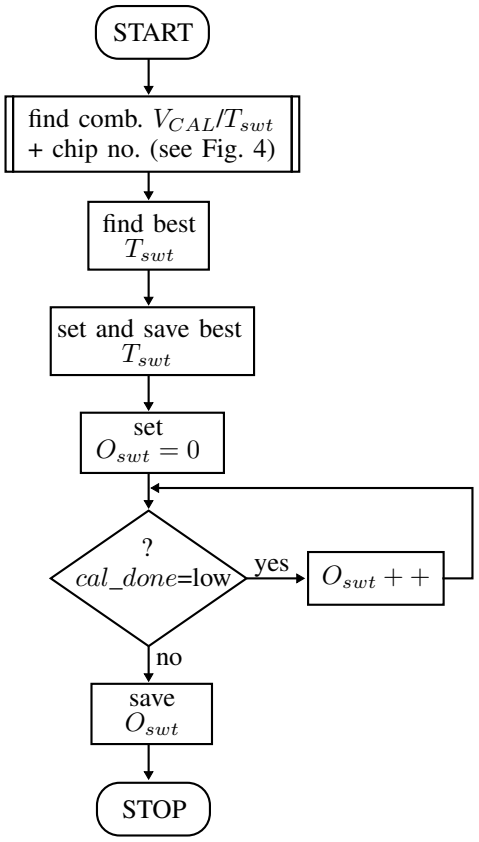

Figure 5. Flowchart of the second part of the calibration sequence which repeats the measurements of part one, identifies and saves the optimal temperature compensation and performs the offset calibration at a oven temperature T_2

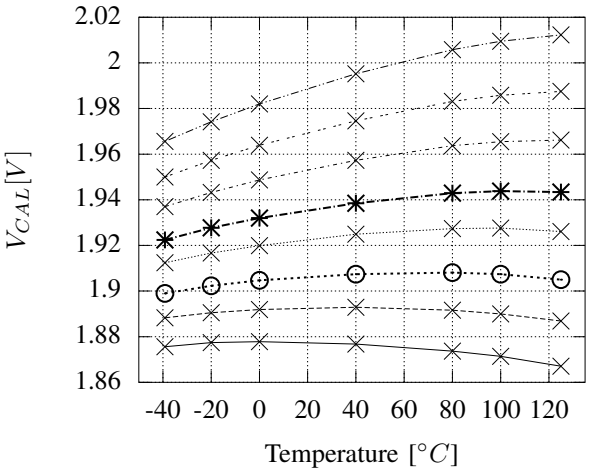

Figure 6. Output voltage V_{CAL} as a function of all possible values of *Tswt<2:0>*. The line marked with '*' represent the uncalibrated output, the line with 'O' shows the output voltage with optimized temperature coefficient. $T_{swt} = 0$ is the lowest, $T_{swt} = 7$ the highest curve

conditions, the remaining ones are from a corner lot which consists of eight different wafers where every wafer was

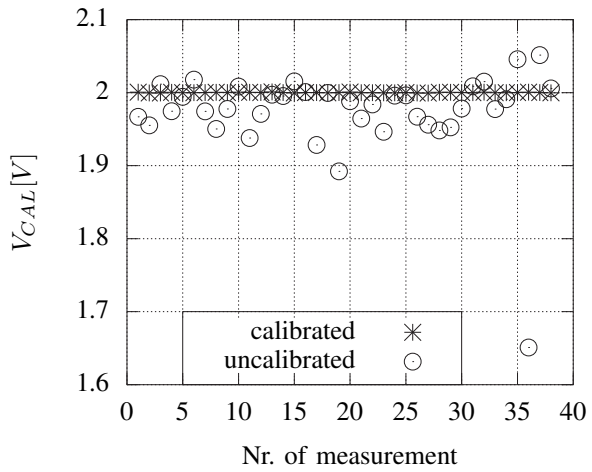

Figure 7. Comparison of the offset calibrated and uncalibrated output voltage V_{CAL}. Target value is $V_{CAL} = 2.0V$.

intentionally produced at selected process corners (e.g. 'fast' low threshold voltages, 'slow' high threshold voltages, 'HR' high resistance, etc.). After offset calibration the output voltage is within $+1.2mV$ to $-0.6mV$ around the desired $2V$ output.

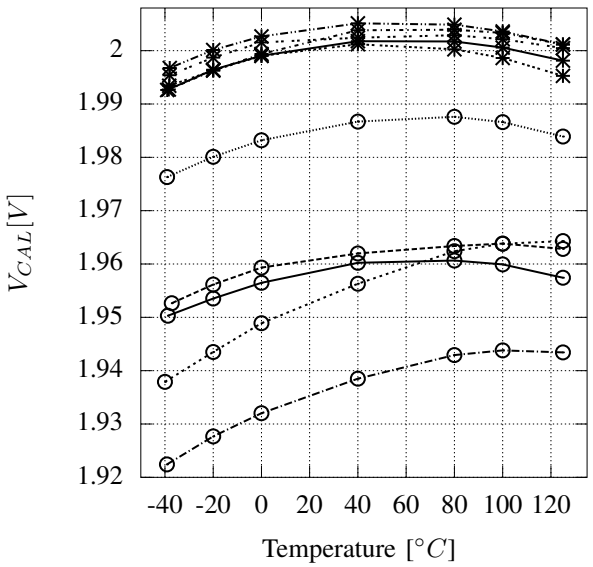

Figure 8. Comparison of five uncalibrated reference voltages (marked with 'O') and the corresponding output voltages V_{CAL} with calibrated temperature coefficient and offset (marked with '*'). Target value is $V_{CAL} = 2.0V$.

Fig. 8 shows a comparison of five uncalibrated reference voltages (marked with 'O') and the corresponding output voltages whereat the temperature coefficient and the offset error is calibrated (marked with '*'). The overall error over a temperature range of $165^{\circ}C$ around the target voltage $V_{CAL} = 2V$ is reduced from $\Delta V_{CAL} = 65mV$ ($V_{CAL} = 1.987V \ldots 1.922$) to $\Delta V_{CAL} = 11mV$ ($V_{CAL} = 2.004V \ldots 1.993V$).

V. Conclusions

This paper demonstrates a novel voltage reference design and calibration methodology that is not only able to compensate for process and material dependent variations of the temperature coefficient but also mitigates against offset errors that are unavoidable in production due to variations in process conditions and mismatch.

Calibration of ASICs at two different temperatures mean additional logistic and technical work and expenses but results in voltage references with low temperature dependency and high initial accuracy and is an appealing alternative to other calibration methods e.g. laser timing.

Our measurements and simulations show that in this regard the circuit is superior to untrimmed alternatives.

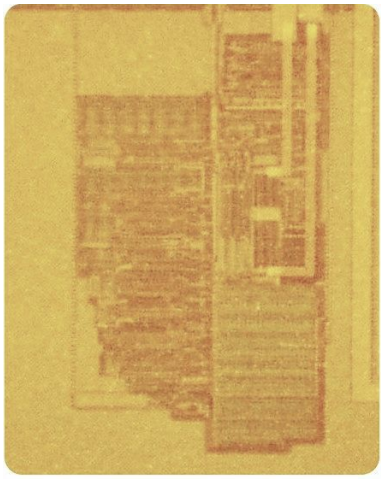

Figure 9. Photograph of the chip die

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