An Ultra-Low Temperature-Coefficient CMOS Voltage Reference

H. C. Lai and Z. M. Lin

***Abstract* –A CMOS voltage reference, which is based on the same magnitude of gate-source voltage of an NMOS and a PMOS operating in saturation region, is presented. The voltage reference is designed for CMOS low-dropout linear regulators and has been implemented in TSMC 0.18 μm CMOS process. The effect area is only 18 μ m × 25 μ m. It gives a temperature coefficient of not greater than 0.68 ppm/℃ from -70℃ to 150℃ without trimming, while consuming a maximum of 1 μA with a supply voltage of 0.9 V.**

I. Introduction

Voltage reference circuit is an important building block in the design of many mixed-signal and analogue integrated circuits such as oscillators, OPAs and ADC/DAC. The specifications of a voltage reference such as temperature coefficient and manufacture drift directly affect the performance of those circuits. The voltage reference is usually a bandgap reference, which can be implemented using parasitic vertical BJTs in any standard CMOS technology [1]. But in all these designs, either diodes or BJTs are used to generate a "proportional to absolute temperature" (PTAT) voltage, which is then used to compensate the negative temperature coefficient of the bipolar junction drop (V_{BE}). BJTs present several problems in the implementation of the bandgap references [2]: (a) The parasitic bipolar transistor in a CMOS process is usually not very well characterized; (b) The output voltage is fixed since the base of the parasitic transistor is grounded; (c) Curvature compensation is needed for precision applications because V_{BE} is not a linear function of temperature over the entire temperature range.

In this paper, a voltage reference in a standard CMOS technology based on the same magnitude of gate-source voltage of an NMOS and a PMOS transistor operating in saturation region is presented. It does not use any diodes or BJTs, so it overcomes the problems listed above. The performance of the proposed voltage reference is better than classical bandgap circuits. It is suitable for temperature-independent reference applications.

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II. Circuit Design

First, we will introduce a technique, which is called Widlar current source. This technique could produce a reference voltage independent of power supply variation. Second, we discuss various phenomena that arise from the variation of temperature in semiconductors.

A. *Power Supply Independent*

Fig. 1 shows the schematic of this circuit. In Fig. 1, MS1, MS2 and MS3 are the start-up circuit. It can provide a current in M4 to prevent the undesired situation, where I_1 and I_2 are zero. The main circuit consists of M1, M2, M3, M4, and R. M3 and M4 form the current mirror and force the current I_1 and I_2 to be equal. It can be easily shown that [3]

$$I_2 = \frac{2}{\mu_n C_{ox}(W/L)_N} \cdot \frac{1}{R^2}\left(1-\frac{1}{\sqrt{K}}\right)^2 \qquad (1)$$

Where K is the W/L ratio of M1 and M2, and body effect is neglected. In equation (1), I_2 is independent of power supply. Therefore, using a current mirror can get a power supply stable voltage reference. (But still is a function of temperature).

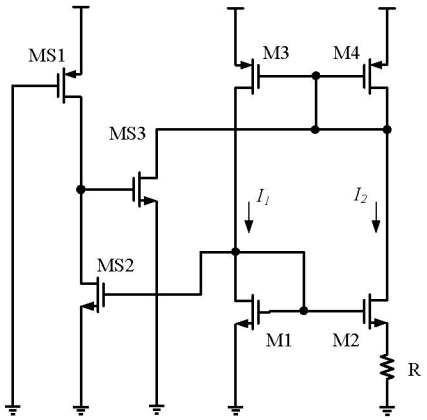


Fig. 1. Widlar Current Source with start-up circuit.

B. *Temperature-Stable*

Due to the improvement on the fabrication techniques, smaller feature sizes, higher packing density

and rising power consumption lead to a dramatic increase on the temperature of integrated circuits. So, temperature dependence of CMOS components is an important performance characteristic in analog circuit design. The primary temperature-dependent parameters in CMOS are mobility and threshold voltage.

Threshold voltages and mobility are the two major sources of temperature-sensitivity in realizing CMOS circuits. The temperature-dependence of threshold voltage (V_T) can be modeled [4] as

$$V_T(T) = V_T(T_0) + \alpha(T - T_0) \tag{2}$$

Where T_0 = 300 K and α is the temperature coefficient of the threshold voltage. As to the mobility, the typical equation of mobility used to characterize the temperature dependence is given as

$$\mu(T) = \mu_0(\frac{T}{T_0})^m \tag{3}$$

Where m is the mobility-temperature exponent. The coefficient m usually takes on a value between -1.5 and -2 [5] depending on the process.

The threshold voltages of NMOS and PMOS have opposite temperature dependence. This characteristic can be used to design a temperature-compensation circuit. The concept is similar to the principle of the voltage reference in Fig. 2. By subtracting V_{TP} and V_{TN}, the temperature coefficients are cancelled and the resulting voltage can be adjusted to the desired output reference voltage.

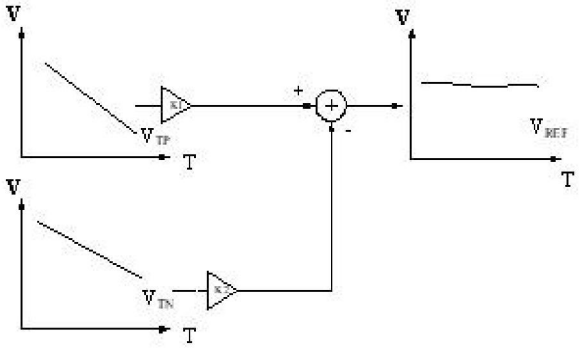


Fig. 2. Voltage reference concept.

Fig. 3 shows a proposed initial voltage reference circuit. Referring to the left part of this figure is a Widlar current source which can produce a bias current independent of the power supply. The right part is the designed circuit that produces the temperature-stable voltage reference. In the circuit, transistors M7 and M8 have the same magnitude of gate-source voltage that provides a temperature-compensation mechanism for the variations of threshold voltage and mobility. If both transistors are driven in saturation by the same magnitude of bias currents, the drain currents of transistors M7 and M8 are equal in magnitude and can be given as

$$I_{D7} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS7} - V_{TN})^2 = \frac{1}{2}\beta_n(V_{GS7} - V_{TN})^2 \tag{4}$$

$$I_{D8} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{GS8} - V_{TP})^2 = \frac{1}{2}\beta_p(V_{GS8} - V_{TP})^2 \tag{5}$$

where β_n and β_p are the device gain factors of the n- and p-transistors, respectively. Seeing Fig. 3, the V_{GS} of M7 and V_{SG} of M8 are the same. By letting $I_{D7} = I_{D8}$, the reference voltage V_{REF} for the above circuit can be derived as

$$V_{REF} = V_{GS7} = \frac{V_{TP} + \sqrt{\frac{\beta_n}{\beta_p}}V_{TN}}{\sqrt{\frac{\beta_n}{\beta_p}} - 1} \tag{6}$$

Considering each term in (6) with respect to temperature, it can be shown that the terms of mobility dependence are completely cancelled out. In the previous discussion, the variation of threshold voltage with respect to temperature is linear and the slopes are -0.13 mV/℃ and 0.2 mV/℃ for NMOS and PMOS, respectively. This means that the first term and the second term in numerator of (6) are in opposite sign, and the variations due to the drift of temperature can be minimized by an appropriate choice of the device gain factors in (6) over the temperature range.

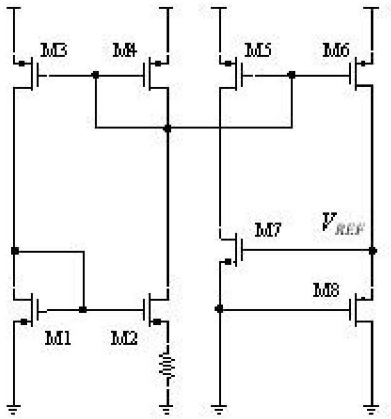


Fig. 3. Proposed initial voltage reference circuit.

In order to decrease the numbers of transistors to achieve low-power dissipation, a novel ultra-low temperature-coefficient and a low power voltage reference is proposed as shown Fig. 4. The Widlar current source is made of transistors M1, M3, M4, M6 and R, and the temperature-stable circuit is made of transistors M1, M2, M4 and M5. Similarly, from equations (1), (4), and (6), the current I_3 of the Widlar current source are supply-insensitive, and the variation due to temperature is balanced by M1 and M2, respectively, and all currents are equal. The voltage reference V_{REF} is expected to be stable to supply voltage and temperature.

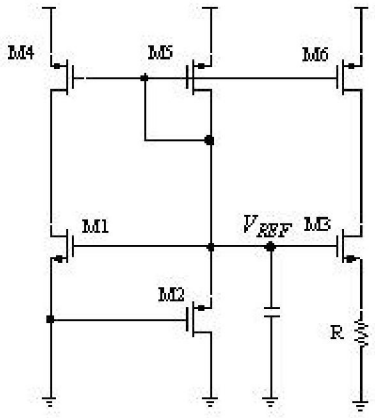


Fig. 4. The novel ultra-low temperature-coefficient and low power voltage reference circuit.

III. Simulation Results

The proposed design was fabricated in a 0.18 μm CMOS technology offered by TSMC. The core layout and die photograph are shown in Fig. 5. The simulation results show that the proposed voltage reference generates a mean reference voltage of about 557 mV. Fig. 6 shows the output voltage dependence on temperature for different process corners (TT, FF and SS) with supply voltage of 0.9 V and static current of 1.03 μA. The variation in output voltage is ±115 μV or 0.68 ppm/℃, over a -70℃ to 150℃ range. The maximum temperature coefficient is only 2.25 ppm/℃ with supply voltages from 0.7 V to 1.4 V, as shown in Fig. 7. All the simulation characteristics and comparisons with other reported circuits are summarized in Table I. Compared with the previous voltage references, the performances of the proposed circuit is superior in quiescent power consumption and thermal stability.

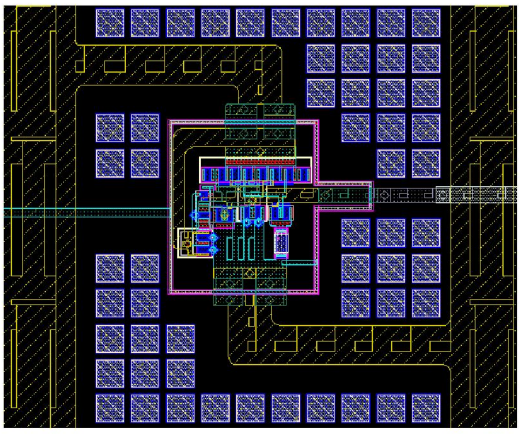


Fig. 5. The core layout of the proposed voltage reference, the effective area is 18 μmx25 μm.

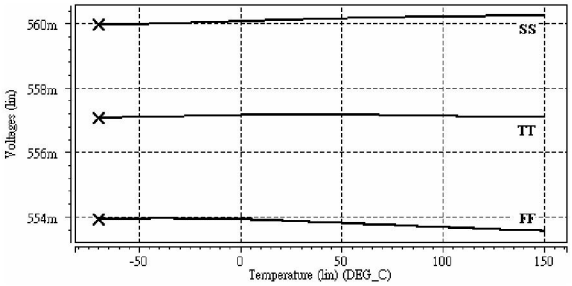
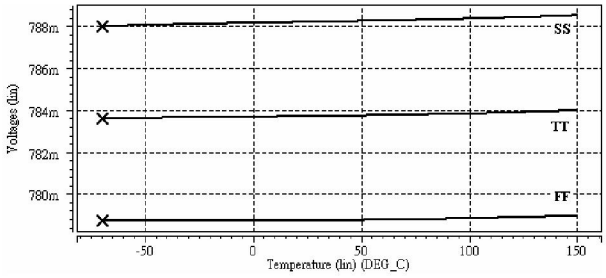
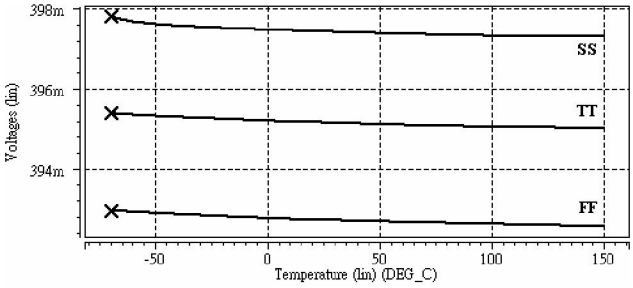


Fig. 6. Simulated output voltage versus temperature in different process corners.



(a)



(b)

Fig. 7. Simulated output voltage versus temperature with maximum and minimum supply voltage of (a) 1.4 V and (b) 0.7 V in different process corners.

TABLE I
PERFORMANCE COMPARISON OF VOLTAGE REFERENCES

	2004 [5]	2005 [7]	2006 [6]	**This work**
Process	CMOS 0.18μm	CMOS 0.35μm	CMOS 90nm	**CMOS 0.18μm**
Supply voltage	1.8 V	0.9 V	1.2 V	**0.9 V**
Output voltage	640 mV	513.1 mV	723 mV	**557 mV**
Thermal stability	4.0 ppm/℃ ±0.615 mV -50~150 ℃	13.6 ppm/℃ ±0.68 mV 0~100 ℃	59.8 ppm/℃ ±5.06 mV -20~90 ℃	**0.68 ppm/℃ ±0.115 mV -70~150 ℃**
Static current	53 μA	3.6 μA	1.3 μA	**1.03 μA**

IV. CONCLUSION

In this paper, we propose a CMOS voltage reference, which is based on the same magnitude of gate-source voltage of NMOS and PMOS transistors operating in saturation region that provides the temperature-compensation mechanism. The voltage reference has been implemented in TSMC 0.18 μm CMOS process. The effective area is only 18 μm×25 μm. It gives a temperature coefficient of less than 0.68 ppm/℃ from -70℃ to 150℃ without trimming, while consuming a maximum of 1.03 μA with a supply voltage of 0.9 V. The reference voltage is around 557 mV.

ACKNOWLEDGEMENT

This work was supported in part by the National Chip Implementation Center and by the National Science Council of Taiwan, R.O.C., under Grants 96-2221-E-018-024.

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