TOWARDS A SUB-1 V CMOS VOLTAGE REFERENCE

Laleh Najafizadeh, Igor M. Filanovsky

Department of Electrical and Computer Engineering
University of Alberta, Edmonton, Alberta, Canada, T6G 2V4
E-mail: laleh@ece.ualberta.ca, igor@ece.ualberta.ca

ABSTRACT

A sub-1-V CMOS voltage reference, which takes advantage of summing the gate-source voltages of two NMOS transistors operating in saturation region, is presented. Both transistors are working below zero temperature coefficient point and thus the voltage reference is able to operate with low supply voltage. The circuit is implemented in a standard 0.18-μm CMOS process and gives a temperature coefficient of 4 ppm/°C in the range of -50°C to 150°C.

Keywords: Analog electronics, mobility, temperature effects, threshold voltage, voltage references

1. INTRODUCTION

A voltage reference is an essential part of many analog and digital circuits, such as precision power supplies, A/D and D/A converters, DRAM and flash memories. A band-gap voltage reference is generally used since it's output voltage is stable against temperature and process variations. Band-gap references can be implemented in CMOS technology using parasitic bipolar transistors [1]. However, when the supply voltage becomes below 1 V, the performance of a conventional band-gap reference degrades [2]. It is predicted in the ITS road map that in year 2010 the mainstream power supply voltage will be around 0.6 V [3]. At these voltages, IC designers will be challenged with possibility of temperature instability and thermal ran-out [4], especially when the transistors are operating below the zero-temperature coefficient (ZTC) point. From the other side, as shown in this paper, the presence of ZTC point can be used for the design of low-voltage CMOS reference circuits with the performance comparable to the performance of the bandgap voltage references and better than the performance of other low voltage non-bandgap CMOS references.

These other non-bandgap CMOS references include voltage references based on threshold voltage subtraction between two MOS transistors [5], [6] and threshold voltage summation [7]. But both techniques require multi-threshold transistors, which can be implemented using additional fabrication steps in CMOS technology. The ZTC point has also been used for the design of CMOS voltage references [8], [9]. However, for low voltage design, the power supply might be lower than the ZTC point in a certain technology [3].

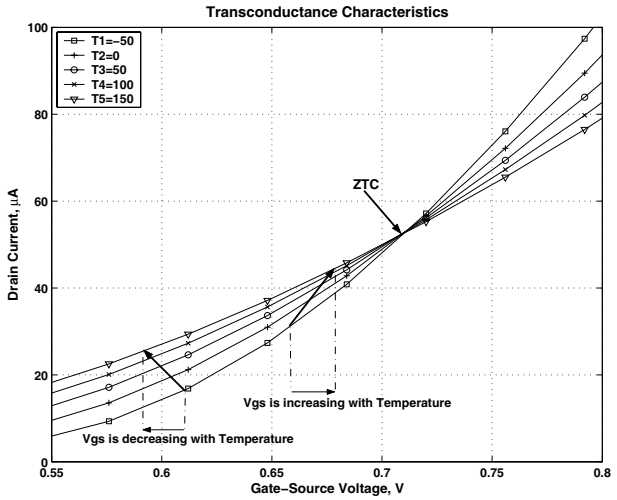

Fig. 1. Simulated transconductance characteristics of a NMOS transistor

In this paper, we present a sub-1 V voltage reference which can be realized in a standard CMOS technology, using PTAT current sources. The PTAT current sources are used to bias two diode-connected NMOS transistors, both operating below their ZTC points, in such a way that, their drain voltages will have opposite temperature coefficients. Then, on a resistor connecting these drains, one can find a point where the voltage does not change with temperature.

The remainder of this paper is organized as follows. In section 2, we consider the temperature behavior of the gate-source voltage of a diode-connected transistor biased with a PTAT current. In Section 3, we present the proposed voltage reference circuit and we investigate the design conditions for achieving a temperature independent output voltage. Simulation results based on the circuit proposed in Section 3 are given in Section 4. Finally, the results are summarized in Section 5.

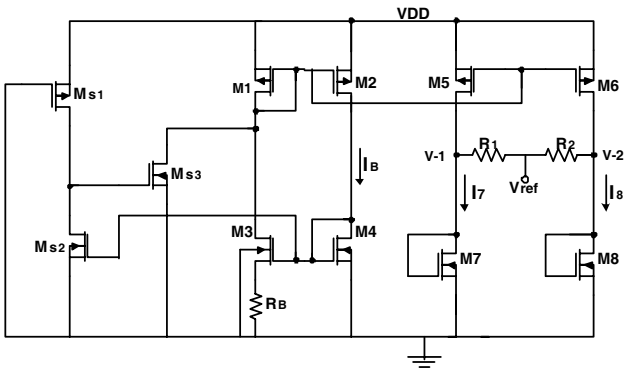

Fig. 2. The proposed voltage reference

2. BASIC CONCEPT

In this section we investigate the temperature behavior of the gate-source voltage of a diode-connected transistor biased with a PTAT current source.

Fig. 1 shows the simulated transconductance characteristics (with temperature as a parameter) for a normal NMOS transistor in 0.18μm CMOS technology. The ZTC point is clearly shown in the figure.

Let the diode connected NMOS transistor with such characteristics be biased with the PTAT current, $I_D(T)$, that can be expressed as

$$I_D(T) = I_{D0}[1+\gamma(T-T_0)] \tag{1}$$

where T_0 is the reference temperature and γ is a positive constant. Following [9], [10] and [11], the gate-source voltage of an NMOS transistor can be written as

$$V_{GS}(T) = V_{TH0} - \alpha_{VT}(T-T_0) + K(T/T_0)^{\frac{m}{2}}\sqrt{I_D(T)}, \tag{2}$$

where m and α_{VT} are positive constants and

$$K = \sqrt{\frac{2}{\mu_0 C_{ox}(W/L)}}. \tag{3}$$

In (2), we have assumed that the threshold voltage, V_{TH}, decreases with temperature linearly as

$$V_{TH}(T) = V_{TH0} - \alpha_{VT}(T-T_0), \tag{4}$$

and mobility, $\mu(T)$, depends on temperature as

$$\mu(T) = \mu_0(T/T_0)^{-m}. \tag{5}$$

At $T = T_0$ the gate-source voltage is equal to

$$V_{GS}(T_0) = V_{TH0} + K\sqrt{I_{D0}}. \tag{6}$$

Now, if the temperature is increased from $T = T_0$ by a small amount of δT to $T_0 + \delta T$, then the gate-source voltage of the above transistor will be equal to

$$\begin{aligned} V_{GS}(T_0+\delta T) =& V_{TH0} - \alpha_{VT}\delta T \\ &+ K(1+(\delta T/T_0))^{\frac{m}{2}}\sqrt{I_{D0}(1+\gamma\delta T)}. \end{aligned} \tag{7}$$

Subtracting (6) from (7), we find the change of the gate-source voltage with temperature as

$$\begin{aligned} \delta V_{GS} =& -\alpha_{VT}\delta T \\ &+ \lambda[\sqrt{(1+\gamma\delta T)}(1+(\delta T/T_0))^{\frac{m}{2}} - 1] \end{aligned} \tag{8}$$

where $\lambda = K\sqrt{I_{D0}}$. Using the approximations

$$\sqrt{(1+\gamma\delta_T)} \cong 1 + (\gamma\delta T/2) \tag{9}$$

and

$$(1+\frac{\delta T}{T_0})^{\frac{m}{2}} \cong 1 + \frac{m}{2}\frac{\delta T}{T_0}, \tag{10}$$

equation (8) can be written as

$$\frac{\delta V_{GS}}{\delta T} \cong [-\alpha_{VT} + \frac{\lambda}{2}(\frac{m}{T_0} + \gamma)]. \tag{11}$$

Equation (11) shows that the temperature coefficient of $V_{GS}(T)$ for the diode-connected MOS transistor, biased with a PTAT current source, can be controlled by the PTAT current source parameters, λ and γ. These parameters can be chosen to make the temperature coefficient of this voltage positive, negative or zero. Two cases are clearly shown in Fig. 1.

3. VOLTAGE REFERENCE CIRCUIT

The proposed voltage reference circuit is shown in Fig. 2. The circuit consists of three parts: (1) a start-up circuit (transistors M_{s1}-M_{s2}) (2) a low-voltage standard [12] bias circuit (transistors M_1-M_4 and resistor R_B) for the realization of PTAT currents, and (3) the reference core circuit (two diode-conne- cted transistors M_7 and M_8 operating below the ZTC point, and two resistors, R_1 and R_2). Transistors M_5 and M_6 supply PTAT currents to the transistors M_7 and M_8. We now show that the current I_B is proportional to temperature. The current, I_B is equal to [12]

$$I_B = \frac{2[\sqrt{(L/W)_4} - \sqrt{(L/W)_3}]^2}{C_{ox}R_B^2\mu(T)}. \tag{12}$$

We assume that the resistor R_B in (12) temperature dependent and can be written as

$$R_B = R_{B0}[1 + \alpha_{R1}(T-T_0) + \alpha_{R2}(T-T_0)^2]. \tag{13}$$

Substituting (13) in (12), and using a first order approximation, we can write the current I_B as

$$I_B \approx I_{B0}[1+\gamma(T-T_0)] \tag{14}$$

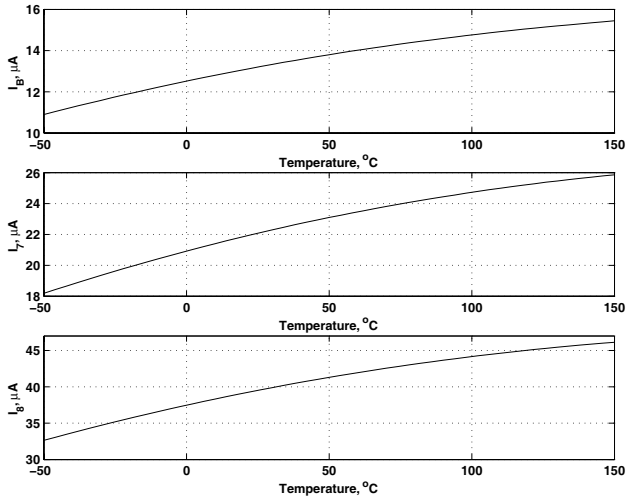

Fig. 3. Temperature dependencies of I_B, I_7 and I_8

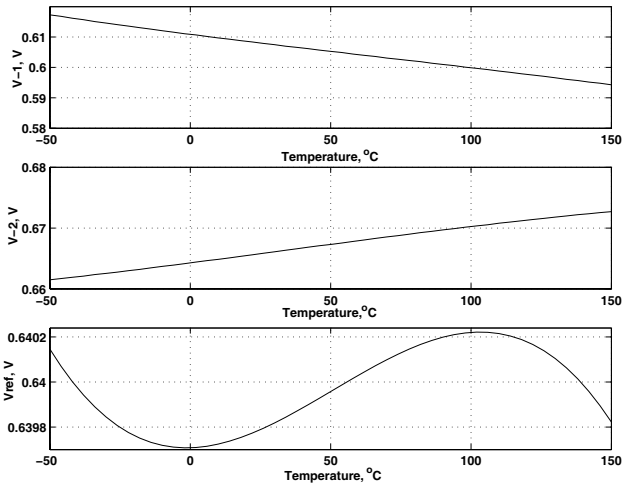

Fig. 4. Temperature dependencies of V_{GS7}, V_{GS8} and V_{ref}

where

$$I_{B0} = (2/C_{ox})\mu_0^{-1}R_{B0}^{-2}\left(\sqrt{(L/W)_4} - \sqrt{(L/W)_3}\right)^2 \quad (15)$$

and

$$\gamma = \frac{m}{T_0} - 2\alpha_{R1}. \quad (16)$$

We have used N^+ nonsilicide diffusion layer with $\alpha_{R1} = 1.47\times10^{-3}\text{deg}^{-1}$ for realization of the resistor, R_B. With this choice, γ would be in the range of $(2\times10^{-3}\text{deg}^{-1}$ to $3.7\times10^{-3})\text{deg}^{-1}$, and the current I_B will be proportional to temperature. Transistors M_5 and M_6 mirror the current I_B and supply PTAT currents, with the temperature coefficient of γ, to transistors M_7 and M_8. The diode-connected transistors M_7 and M_8 have the same length and width, (K_7=K_8), to ensure that their threshold voltage characteristics are sufficiently close. The output voltage, V_{ref}, is then given by

$$V_{ref} = \frac{V_{GS7}}{1+(R_1/R_2)} + \frac{V_{GS8}}{1+(R_2/R_1)}. \quad (17)$$

As it can be seen the reference voltage depends on the ratio of the resistors R_1 and R_2. Therefore, the sensitivity of the output voltage to the variation of resistors (say, due to non-optimized layout) is reduced. Also, to have matched resistors, we assume that $R_1 = R_2$.

The temperature coefficient of the output voltage is obtained by taking the derivative of equation (17) with respect to the temperature. Doing so and using (11), the temperature coefficient of the output voltage will be equal to

$$\begin{aligned}\frac{\delta V_{ref}}{\delta T} &= 0.5\left(\frac{\delta V_{GS7}}{\delta T} + \frac{\delta V_{GS8}}{\delta T}\right) \\ &= -\alpha_{VT} + (\lambda_7+\lambda_8)\left(\frac{m}{4T_0} + \frac{\gamma}{4}\right)\end{aligned} \quad (18)$$

where $\lambda_7 = K_7\sqrt{\frac{(W/L)_5}{(W/L)_1}I_{B0}}$, $\lambda_8 = K_8\sqrt{\frac{(W/L)_6}{(W/L)_1}I_{B0}}$ and γ is given by (16). If the sizes of transistors M_5 and M_6 are chosen to satisfy

$$\sqrt{\left(\frac{W}{L}\right)_5} + \sqrt{\left(\frac{W}{L}\right)_6} = \frac{2\alpha_{VT}\sqrt{(\frac{W}{L})_1}}{(\frac{m}{T_0}-\alpha_{R1})(K_7\sqrt{I_{B0}})} \quad (19)$$

then the reference voltage will be temperature independent.

The minimum required power supply for this reference is given by

$$V_{DD_{\min}} = (V_{THn})_{\max} + |V_{DS5}(sat)| \quad (20)$$

The circuit can be easily designed with the saturation voltage, $V_{DS}(sat)$, less than 0.2 V and with $V_{DD_{\min}}$ less than 1 V.

4. SIMULATION RESULTS

The circuit shown in Fig. 2 was designed for realization in 0.18 μm TSMC technology. All the resistors are realized using N+ nonsilicide diffusion layer and their temperature dependencies are given by (13) where $\alpha_{R1} = 1.47\times10^{-3}$ deg^{-1} and $\alpha_{R2} = 0.832\times10^{-6}\text{deg}^{-2}$. The circuit was simulated in the temperature range of -50°C to 150°C. Fig. 3 shows the simulation results for the currents I_B, I_7 and I_8. As it can be seen the currents increase as the temperature increases. The simulation results for the gate-source voltages of transistors M_7 and M_8 and the output voltage, V_{ref}, are shown in Fig. 4. The temperature stability of the voltage reference output, V_{ref} obtained in simulations is equal to 4 ppm/°C. The results of simulation verify that the circuit operates according to the analysis given in Sections 2 and 3.

Since the temperature-dependence of the threshold voltage and the reference current are not exactly linear in the

Table 1. Temperature stability of different voltage references

Technique	Temperature dependency of output voltage
Bandgap Reference [2]	$\pm$59 (ppm/$^\circ$C)
CMOS Voltage reference based on V_{TH} difference [6]	33.8 (ppm/$^\circ$C)
CMOS voltage reference using ZTC point [9]	10 (ppm/$^\circ$C)
Proposed voltage reference	4 (ppm/$^\circ$C)

whole temperature range, there is nonlinear residue appearing on the reference voltage output. Table 1, compares the temperature performance of the proposed voltage reference with previously designed references. One can see from Table 1 that the proposed voltage reference provides a better performance on temperature-dependence compared to the previously designed CMOS voltage references. The circuit has been sent for fabrication and will be ready in 4 months for experimental measurements.

5. DISCUSSIONS AND CONCLUSIONS

A new approach for the design of low-voltage CMOS voltage references is proposed. Based on this idea a circuit is designed and simulated. The circuit uses resistors and standard CMOS transistors operating in saturation region. The proposed voltage reference provides a better performance on temperature-dependence compared to the previously designed CMOS voltage references. The additional power consumption is approximately equal to that of one stage of an operational amplifier. At the present time, we do not have experimental data (we hope to have them to the time of symposium). But even if they will be 10 times worse than the results in simulations, the proposed circuit will still be comparable with other circuits designed for lower than 1 V power supply [13].

6. REFERENCES

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