A CMOS Voltage Reference Based on Weighted $\Delta V_{\rm GS}$ for CMOS Low-Dropout Linear Regulators

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***Abstract*—A CMOS voltage reference, which is based on the weighted difference of the gate–source voltages of an NMOST and a PMOST operating in saturation region, is presented. The voltage reference is designed for CMOS low-dropout linear regulators and has been implemented in a standard 0.6-μm CMOS technology ($V_{thn} \approx |V_{thp}| \approx 0.9$ V at 0 °C). The occupied chip area is 0.055 mm^2. The minimum supply voltage is 1.4 V, and the maximum supply current is 9.7 μA. A typical mean uncalibrated temperature coefficient of 36.9 ppm/°C is achieved, and the typical mean line regulation is $\pm 0.083\%$/V. The power-supply rejection ratio without any filtering capacitor at 100 Hz and 10 MHz are -47 and -20 dB, respectively. Moreover, the measured noise density with a 100-nF filtering capacitor at 100 Hz is 152 nV/$\sqrt{\text{Hz}}$ and that at 100 kHz is 1.6 nV/$\sqrt{\text{Hz}}$.**

***Index Terms*—CMOS voltage reference, line regulation, mobility, noise, power-supply rejection ratio, temperature coefficient, threshold voltage.**

I. Introduction

A LINEAR regulator, which is an inductor-less, ripple-less, and low-noise power converter, is widely used in many battery-operated devices. In the past, linear regulators have been implemented in BJT technology. However, the power efficiency is not sufficient for low-power operations due to the fact that the ground current is load-current dependent and the dropout voltage is large. With the rapid evolution of CMOS technology, many CMOS low-dropout linear regulators (LDOs) have become available [1], [2]. The ground current is load-current independent, and the LDOs can operate at a low supply voltage, which is suitable for single-cell and two-cell battery applications.

A voltage reference is necessary for LDO design, and it provides a low-supply-dependence and low-temperature-drift reference voltage to define the LDO output voltage. The voltage reference is usually a bandgap reference, which can be implemented using parasitic vertical BJTs in any standard CMOS technology [3], [4]. As an alternative, voltage references in MOS technology can also be implemented by the principle of threshold-voltage difference, which is based on selective channel implant [5], [6], flat-band voltage difference with different gate materials [7] and work-function difference with different gate dopings [8]. However, these reported solutions are not applicable in standard low-cost CMOS technologies since additional fabrication steps are needed.

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In this paper, a voltage reference in standard CMOS technology based on weighted gate–source voltage difference between an NMOST and a PMOST is presented [9], [10]. It is particularly useful as an alternative voltage reference for CMOS LDOs. In Sections II and III, the concept of the proposed voltage reference and circuit implementation are discussed in detail. Then, experimental results are reported to verify the theory.

II. Proposed CMOS Voltage Reference

The proposed CMOS voltage reference is based on the different temperature dependencies of the threshold voltages of an NMOST and a PMOST. A low-temperature-drift reference voltage ($V_{\rm REF}$) can be obtained by mutually compensating the temperature drifts of V_{thn} and V_{thp}. In fact, the magnitudes of V_{thn} and V_{thp} decrease with temperature linearly and can be modeled as [11]–[15]

$$V_{thn}(T) = V_{thn}(T_o) - \beta_{vthn}(T - T_o) \quad (1)$$

$$|V_{thp}(T)| = |V_{thp}(T_o)| - \beta_{vthp}(T - T_o) \quad (2)$$

where T_o is the reference temperature, and β_{vthn} and β_{vthp} are the temperature coefficients of the threshold voltages of an NMOST and a PMOST, respectively. These values are technology dependent [13], and for the AMS[1] 0.6-μm CMOS technology, $\beta_{vthn} = 1.4$ mV/°C and $\beta_{vthp} = 1.9$ mV/°C [15].

For the proposed voltage reference, $V_{\rm REF}$ is basically obtained by subtracting $|V_{thp}|$ from a scaled V_{thn}. This concept can be implemented by the circuit shown in Fig. 1, which is a simple, low-voltage, opamp-less and CMOS-compatible circuit structure.

A low-voltage bias circuit is formed by M1–M4 and R_B. A startup circuit formed by MS1–MS3 is embedded. The bias current to the core reference circuitry is supplied by M5. The core reference circuitry is formed by MN, MP, R_1, and R_2. It is noted that the source-bulk voltage of MP is set to zero to eliminate body effect and improve the power-supply rejection ratio (PSRR). From the circuit, the reference voltage is given by

$$V_{\rm REF} = \left(1 + \frac{R_1}{R_2}\right) V_{\rm GSn} - |V_{\rm GSp}|. \quad (3)$$

Moreover, the principle of operation of the proposed voltage reference is based on all transistors, especially MP and MN, operating in saturation region. Thus, careful design of the bias current is required. Moreover, channel-length modulation effect should be also minimized, and therefore, long-channel devices are chosen.

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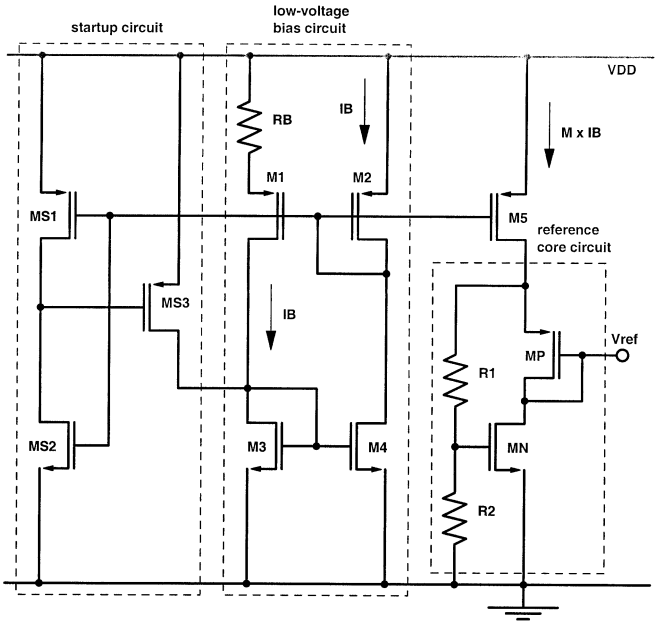


Fig. 1. Proposed CMOS voltage reference.

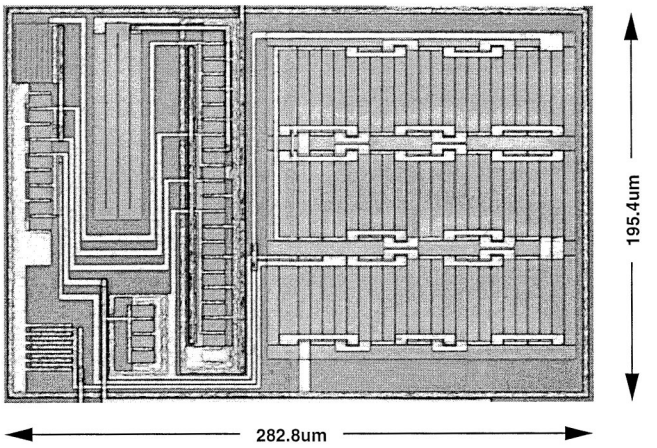


Fig. 2. Micrograph of the proposed CMOS voltage reference.

A. Design Conditions for Optimization

The temperature functions of the mobilities (μ_n and μ_p) of an NMOST and a PMOST with a reference temperature T_o are $\mu_n(T) = \mu_n(T_o)(T/T_o)^{-\beta_{\mu n}}$ and $\mu_p(T) = \mu_p(T_o)(T/T_o)^{-\beta_{\mu p}}$ [9]–[15] where $\beta_{\mu n} = 1.9$ and $\beta_{\mu p} = 1.4$ are the mobility exponents in AMS 0.6-μm CMOS process [15]. The temperature dependence of the reference voltage can be obtained by differentiating (3) with respect to temperature and is given by

$$\begin{aligned}\frac{\partial V_{\mathrm{REF}}}{\partial T} &= \left(1+\frac{R_1}{R_2}\right)\frac{\partial V_{\mathrm{GSn}}}{\partial T} - \frac{\partial |V_{\mathrm{GSp}}|}{\partial T} \\ &= \left[-\left(1+\frac{R_1}{R_2}\right)\beta_{vthn} + \beta_{vthp}\right] \\ &\quad + \frac{\beta_{\mu_p}}{T_o}\sqrt{\frac{2MI_B(T_o)}{\mu_p(T_o)C_{ox}\left(\frac{W}{L}\right)_p}} \\ &\quad \times \left[\left(1+\frac{R_1}{R_2}\right)\left(\frac{1}{2}+\frac{\beta_{\mu_n}}{2\beta_{\mu_p}}\right)\sqrt{\frac{\mu_p(T_o)\left(\frac{W}{L}\right)_p}{\mu_n(T_o)\left(\frac{W}{L}\right)_n}}\right. \\ &\quad \left. \times \left(\frac{T}{T_o}\right)^{(\beta_{\mu p}+\beta_{\mu n}-2/2)} - \left(\frac{T}{T_o}\right)^{\beta_{\mu p}-1}\right] \quad (4)\end{aligned}$$

where $I_B(T_o) = (2/\mu_p(T_o)C_{ox}{R_B}^2)\left[1/\sqrt{(W/L)_2} - 1/\sqrt{(W/L)_1}\right]^2$. As shown in (4), the temperature dependence of the proposed voltage reference is governed by a linear term and a nonlinear term. To obtain $(\partial V_{\mathrm{REF}}/\partial T)|_{T=T_r} = 0$ (where T_r is room temperature), the linear term is set to zero by the resistor ratio, which is given by

$$\frac{R_1}{R_2} = \frac{\beta_{vthp}}{\beta_{vthn}} - 1 \quad (5)$$

and the nonlinear term is set to zero at $T = T_r$ by the transistor size ratio, which is given by

$$\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} = \frac{\frac{\mu_n(T_o)}{\mu_p(T_o)}\left(\frac{T_r}{T_o}\right)^{\beta\mu p-\beta\mu n}}{\left(\frac{\beta_{vthp}}{\beta_{vthn}}\right)^2\left(\frac{1}{2}+\frac{\beta_{\mu_n}}{2\beta_{\mu_p}}\right)^2}. \quad (6)$$

Equations (5) and (6) show that the temperature coefficient can be optimized by circuit parameters instead of refining the process parameters. Freedom on optimization can be done on circuit design level and on-chip trimming.

Since the temperature dependence of the threshold voltage is not perfectly linear and a complete cancellation of the temperature dependence of μ_p and μ_n is not possible in the whole temperature range, a nonlinear temperature-dependent error voltage appears at the reference output voltage.

B. Minimum Supply Voltage

The above analysis is based on the first-order equations of MOS transistors operating in saturation region. The conditions stated in (5) and (6) are independent of the magnitude of the bias current. However, if the bias current decreases, MN and MP may leave saturation region and enter triode region. Thus, the minimum supply voltage must be maintained in order to prevent the current source M5 from being forced to operate in triode region.

The minimum supply voltage should be evaluated at the lowest operating temperature as V_{thn} and $|V_{thp}|$ are maximum. Since both MN and MP operate in saturation region, it is suggested to set V_{GSn} and $|V_{\mathrm{GSp}}|$ larger than their threshold voltages by at least 100 mV. Thus, the minimum supply voltage $(V_{s\min})$ is given by

$$V_{s\min} = \left(1+\frac{R_1}{R_2}\right)V_{\mathrm{GSn}}\text{ at }0\,^{\circ}\mathrm{C} + |V_{DS5(\mathrm{sat})}| \quad (7)$$

which is about 1.4 V in AMS 0.6-μm CMOS process. A sub-1-V supply operation can be achieved with low-threshold-voltage devices of about 0.65 V at 0 °C.

TABLE I
SUMMARY OF THE MEASUREMENT RESULTS

Number of samples	Total 15 samples from 3 separate runs		
Supply voltage	1.4 V to 3.0 V		
Supply current	9.7 μA (max.)		
Reference voltage	309.31±19.26 mV		
Temperature coefficient (0 to 100°C)	2.7 ppm/°C (min.)	36.9 ppm/°C (mean)	62.0 ppm/°C (max.)
Line regulation (25°C)	±0.012%/V (min.)	±0.083%/V (mean)	±0.225%/V (max.)
PSRR (V_s = 1.4 V, C_{OUT} = 0 and 25°C)			
@100 Hz	-47 dB		
@10 MHz	-20 dB		
Noise density (V_s = 1.5 V and 25°C)			
C_{OUT} = 100 nF	152 nV/$\sqrt{\text{Hz}}$@100 Hz and 1.6 nV/$\sqrt{\text{Hz}}$@100 kHz		
C_{OUT} = 470 nF	50 nV/$\sqrt{\text{Hz}}$@100 Hz and 1.2 nV/$\sqrt{\text{Hz}}$@100 kHz		
Chip area in 0.6-μm CMOS technology	0.055 mm^2		

C. Trimming Sensitivity

The sensitivity of the temperature coefficient to the variation of R_1 to R_2 ratio (due to doping gradient, nonoptimized layout and high stress area of die) is low. When the resistor ratio in (5) is increased by a small amount, a negative temperature coefficient appears in the first term of (4) due to the incomplete compensation of β_{vthn} and β_{vthp}. However, a positive temperature coefficient created by the mobility terms in the second term of (4) compensates the effect. The phenomenon is similar when the ratio is decreased by a small amount.

Moreover, when the error of the resistor ratio $(\Delta(R_1/R_2))$ is considered, the error of the scaling factor is reduced by the constant 1. Since R_1/R_2 is generally less than one ($R_1/R_2 = 0.357$ in this design and this value depends on the temperature coefficients of the threshold voltages), the normalized error of the scaling factor $(1 + (R_1/R_2))$ is smaller than that of the resistor ratio R_1/R_2.

Due to these effects, the sensitivity of the resistor ratio is reduced, and thus the resolution of the trimming circuit can be reduced substantially. Low-resolution trimming network or no trimming procedure is required for stable technologies.

D. Line Sensitivity

The line sensitivity of the proposed CMOS voltage reference can be studied from (3). When the supply voltage changes, I_B also changes due to the channel-length modulation effect of MOST. When I_B increases/decreases, V_{GSn} and $|V_{\text{GSp}}|$ also increase/decrease simultaneously. Although the increases and decreases on V_{GSn} and $|V_{\text{GSp}}|$ are not the same, the difference of these two voltages minimizes the variation of V_{REF}. Moreover, when (3) is expanded to

$$V_{\text{REF}} = \left[\left(1+\frac{R_1}{R_2}\right)V_{thn} - |V_{thp}|\right] + \sqrt{I_B} \cdot \left[\left(1+\frac{R_1}{R_2}\right)\sqrt{\frac{1}{\mu_n C_{\text{ox}}\left(\frac{W}{L}\right)_n}} - \sqrt{\frac{1}{\mu_p C_{\text{ox}}\left(\frac{W}{L}\right)_p}}\right] \quad (8)$$

it is shown that the effect of the change in I_B is small since $V_{\text{REF}} \propto \sqrt{I_B}$. The square root dependence reduces the I_B dependence of V_{REF} significantly.

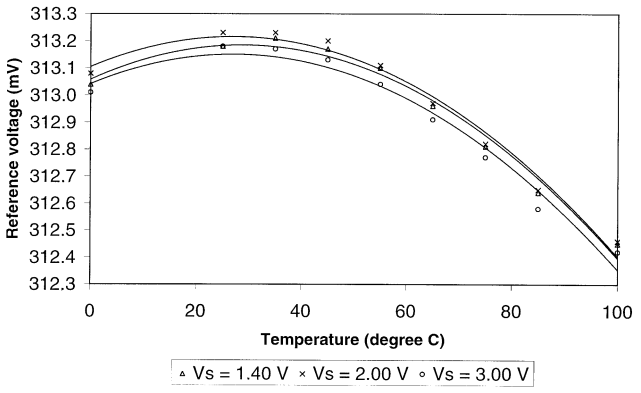
III. EXPERIMENTAL RESULTS

The proposed voltage reference shown in Fig. 1 has been successfully implemented in AMS 0.6-μm CMOS process ($V_{tn} \approx |V_{tp}| \approx 0.9$ V at 0 °C). Optional high-resistive poly resistor (about 1.2 kΩ/sq.) is used to reduce the chip area. The micrograph is shown in Fig. 2 and the occupied chip area is 0.055 mm^2, which is much smaller than the bandgap reference. A total of 15 samples from three separate fabrication runs have been measured and the performance is summarized in Table I. The minimum supply voltage is 1.4 V and the maximum supply current is 9.7 μA which occurs at the maximum supply voltage (3 V) and the maximum operational temperature (100 °C).

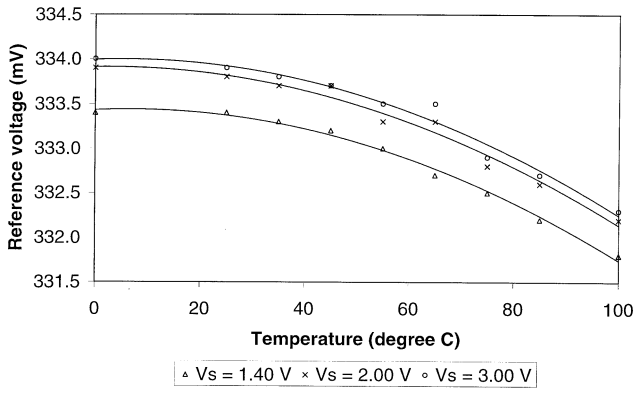
The typical mean reference voltage is 309.31 mV. When the proposed voltage reference is applied to CMOS LDOs, the output voltage can be adjusted by the feedback resistors of a LDO. This adjustment is a less expensive and less time-consuming trimming procedure compared with the temperature trimming in bandgap reference.

The typical mean and worst-case line regulations are $\pm 0.083\%/\text{V}$ and $\pm 0.225\%/\text{V}$, respectively. In addition, the typical mean uncalibrated temperature coefficient is 36.9 ppm/°C, and the minimum and maximum uncalibrated temperature coefficients are 2.7 and 62 ppm/°C, respectively. Fig. 3(a) shows a sample with temperature coefficient of about 24 ppm/°C at 1.4-, 2-, and 3-V supply voltages. An intentional variation in the resistor ratio by $+6.23\%$ is performed and is shown in Fig. 3(b). The change on the temperature coefficient is only from 24 to 50 ppm/°C. This verifies the previous theoretical analysis on the low sensitivity of the resistor ratio.

The measured PSRR at the minimum supply voltage of 1.4 V without a filtering capacitor to improve the high-frequency region is shown in Fig. 4. The PSRR at 100 Hz and



(a)



(b)

Fig. 3. Measured results on temperature effect. (a) Optimized resistor ratio. (b) Resistor ratio off by $+6.23\%$.

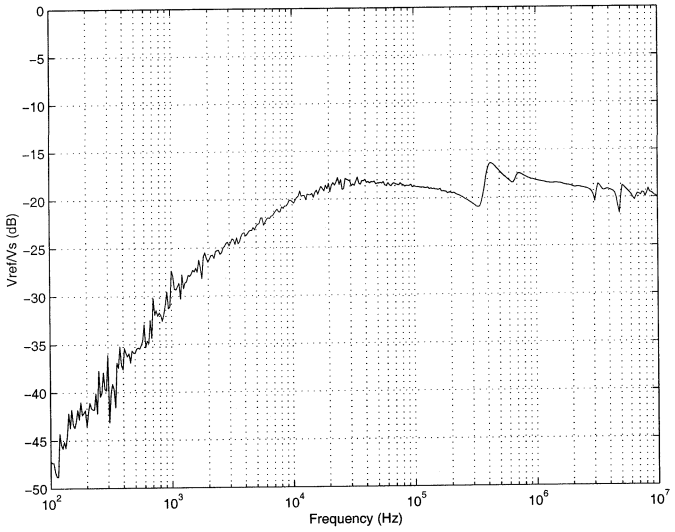


Fig. 4. Measured PSRR of the proposed CMOS voltage reference (V_s = 1.4 V, $C_{\rm OUT} = 0$ at 25 °C).

10 MHz are -47 and -20 dB, respectively. The PSRR is sufficient for typical LDOs that are used for post-regulation of a switching-mode power converter with a typical switching frequency of 100 kHz–1 MHz.

The measured spectral noise density is shown in Fig. 5. The measured noise densities with a 100-nF filtering capacitor at

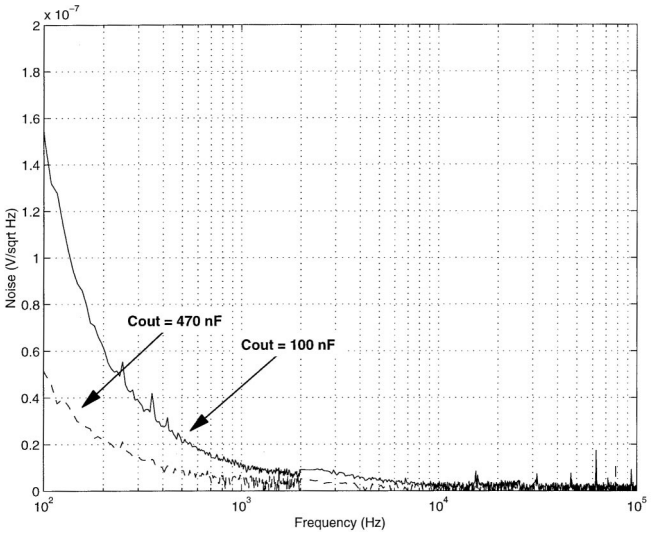


Fig. 5. Measured output spectral noise density of the proposed CMOS voltage reference with different filtering capacitors ($V_s = 1.5$ V at 25 °C): (a) solid line: $C_{\rm OUT} = 100$ nF and (b) dash line: $C_{\rm OUT} = 470$ nF.

100 Hz and 100 kHz are 152 and 1.6 nV/$\sqrt{\rm Hz}$, respectively. When a filtering capacitor of 470 nF is used, the noise density, as shown in Fig. 5, can be substantially reduced but the startup time will be increased.

IV. Conclusion

A CMOS voltage reference has been presented and the conditions for optimization have been stated. The proposed circuit is reproducible in any CMOS technology. Experimental results show that the proposed voltage reference provides a low-voltage low-power operation. Moreover, the small chip area, low-temperature coefficient, low-line sensitivity, and high-PSRR performances are well suited for CMOS LDOs. The proposed CMOS voltage reference can be further applied to CMOS switching-mode power converters and CMOS mixed-signal systems.

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