A Low Power CMOS Bandgap Voltage Reference with Enhanced Power Supply Rejection

Wenguan Li, Ruohe Yao * , and Lifang Guo

Abstract — *A low power low temperature-coefficient bandgap voltage reference features high power supply rejection (PSR) for low dropout regulators (LDOs) is presented in this paper. An optimized PSR enhance stage is inserted in opamp based CMOS bandgap voltage reference, which introduces supply spurious into the bandgap loop so as to maintain a constant gate-source voltage in the upper current mirror; this improves the PSR performance about 38dB. A prototype of the bandgap voltage reference is implemented in TSMC 0.6μm double poly, double metal, CMOS technology, occupying 0.07mm^2 active silicon areas. The measured PSR are -82.8dB@ 50 kHz and -70 dB@100 kHz, respectively; and, the supply current is 9μA, the temperature-coefficient is 15ppm/°C at 2~5V supply voltage, the line regulation is 54μV/V.* [1]

Index Terms — Bandgap voltage reference; Low power; High power supply rejection.

I. Introduction

Since supply voltage is scaling down with the reducing thickness of gate oxide in modem CMOS technology and the increasing demand for low power portable devices, the dynamic range of system is becoming much smaller. Spurious coming from the noisily power supply without adequately rejected will seriously degrade system performances, especially in RF applications [1]-[3]. So, LDOs with high accuracy low temperature-coefficient have been used widely in noise sensitive wireless transceivers [4] and ADCs [5]. The power supply rejection (PSR), which is a merit of LDOs' immunity against power spurious, is most important. The maximum achievable PSR of LDOs is mostly limited by the PSR of voltage reference. Thus, the design of low-power low temperature-coefficient high PSR bandgap voltage reference is becoming more and more important [2].

In this paper, the PSR of bandgap voltage reference is analyzed in detail based on the corresponding PSR small signal model in section Ⅱ. A low power, low temperature-coefficient bandgap voltage reference features high power supply rejection capability for LDOs application is demonstrated in sectionⅢ. The experiment results and conclusion are given in sectionⅣ and section Ⅴ, respectively.

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II. PSR Analysis of Bandgap Voltage Reference

The base-emitter junction voltage of bipolar transistor, in generally the forward voltage of a pn-junction, exhibits negatives temperature-coefficient, which is about -1.5mV/°C [6], [7]. The difference between the base-emitter junction voltages of two bipolar transistors operating at different current density is directly proportional to the absolute temperature, which exhibits positive temperature-coefficient [7]. A temperature stable bandgap voltage reference can be achieved by summing this two voltages having opposite temperature-coefficients with proper weighting.

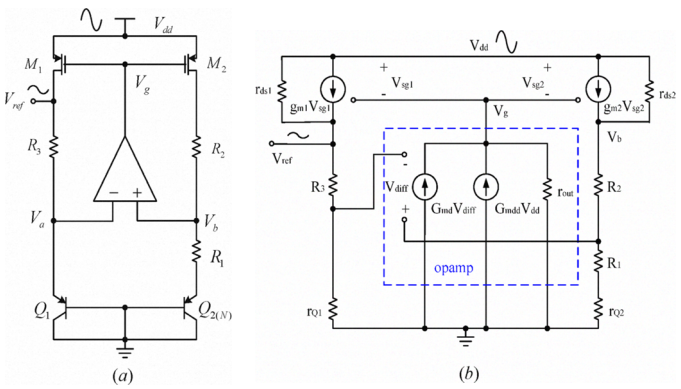

Fig. 1. (a) Circuits of conventional CMOS bandgap voltage reference. (b) PSR small signal analysis model of conventional CMOS bandgap voltage reference.

The conventional opamp based CMOS bandgap voltage reference is shown in Fig.1. (a). PSR analysis of conventional CMOS bandgap voltage reference can be performed based on its PSR analysis small signal model indicated in Fig. 1. (b). The output resistance of $M_{1,2}$ is omitted to neglect the channel length modulation of the current mirror pairs in order to gain more insight of the PSR performance. We can get the below equations from Fig.1. (b).

$$v_g = A\left(\beta_2 v_b - \beta_1 v_{ref}\right) + A_{dd} v_{dd} \tag{1}$$

$$g_{m1,2}\left(v_{dd} - v_g\right) r_{Q1} = \beta_1 v_{ref} \tag{2}$$

$$g_{m1,2}\left(v_{dd} - v_g\right)\left(r_{Q2} + R_1\right) = \beta_2 v_b \tag{3}$$

$$\beta_1 = \frac{r_{Q1}}{r_{Q1} + R_3} \tag{4}$$

$$\beta_2 = \frac{r_{Q2} + R_1}{r_{Q2} + R_1 + R_2} \tag{5}$$

Where, $A=v_g/v_{diff}=G_{md}r_{out}$, $A_{dd}=v_g/v_{dd}=G_{mdd}r_{out}$ are the gain and

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PSR of the opamp, respectively. $g_{m1,2}$ is the transconductance of $M_{1,2}$. And, r_{Q1}, r_{Q2} are the small signal on resistance of Q_1 and Q_2, respectively. The PSR of the bandgap voltage can be derived from (1) - (5), and it's given by (6).

$$\frac{v_{ref}}{v_{dd}} = g_{m1,2}\left(r_{Q1}+R_3\right)\frac{1-A_{dd}}{1+g_{m1,2}\left(r_{Q2}+R_1\right)A-g_{m1,2}r_{Q1}A}$$

$$\approx g_{m1,2}\left(r_{Q1}+R_3\right)\frac{1-A_{dd}}{1+g_{m1,2}R_1A} \qquad (6)$$

$$\approx\left(\frac{r_{Q1}+R_3}{R_1}\right)\left(\frac{1-A_{dd}}{A}\right)$$

In (6), we note that the PSR of the reference voltage mainly depends on the gain and PSR of the opamp. Increasing opamp's gain can improves the PSR of reference, which may also causes stability issues. As the gain of opamp decreases with the operating frequency, the PSR performance degrades in high frequency. So it's essential to increase opamp's gain band width product (GBW) in order to get a wide band high PSR capability. We also note from (6), if the PSR of opamp is 1 (eg. 0dB), the second term in (6) is zero; the reference will have a high PSR capability. That is to say, if the output of opamp v_g follows the ripple in the power supply, the gate-source voltages of M_1, M_2 maintain constant, since M_1 and M_2 is designed to have a long channel length in order to make the channel length modulation effect small enough to be neglected, which is usually the case in current mirror based CMOS bandgap voltage reference, thus, the drain current of M_1, M_2 remains constant even with supply ripple, so the bandgap voltage reference has a high PSR performance. In conclusion, it's desirable that v_g tracks the fluctuation in the supply voltage. The bandgap voltage reference shown in section Ⅱ, which features high PSR, follows the above principles.

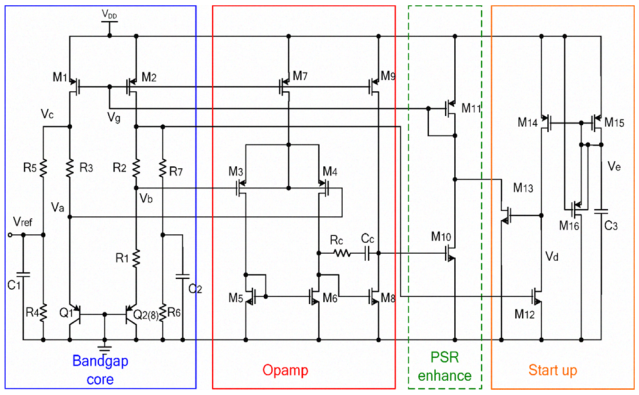

Fig. 2. High PSR bandgap reference circuit implementation

III. HIGH PSR BANDGAP VOLTAGE REFERENCE

The circuit implementation of the low power, low temperature-coefficient bandgap voltage reference with enhanced PSR is illustrated in Fig.2. The bandgap voltage reference consist of four sub-building blocks, including the bandgap core, opamp, PSR enhance stage and startup circuit.

A. Temperature Compensation

The bandgap core consist of Q_1, Q_2, M_1, M_2 and R_1~R_3. Q_1, Q_2 are parasitic vertical PNP, the emitter size of Q_2 is 8 times that of Q_1. R_2 equals R_3, M_1 and M_2 form a current mirror. M_3~M_9, Rc and Cc form a conventional two-stage opamp, whose bias current is directly mirrored from bandgap core. The high gain opamp forces the nodes A and B to have the same potential. Since Q_1 and Q_2, which have unequal sizes but equal emitter current, are biased at different current density. So a PTAT loop is formed in Q_1, Q_2 and R_1. The PTAT current I_{R1} is given as

$$I_{R1}=\frac{V_{be1}-V_{be2}}{R_1}=\frac{V_T\ln(8)}{R_1} \qquad (7)$$

Where, V_T=kT/q is the thermal voltage. This current flows through R_1 and R_3, and, the bandgap reference voltage is given by

$$V_c=V_{be1}+I_{R1}R_2=V_{be1}+\frac{R_2}{R_1}V_T\ln(8) \qquad (8)$$

This reference voltage equals to the silicon energy-gap voltage 1.2V [7]. In order to generate a suitable reference output for LDO application, which is capable of down to 1V output voltage, a resistance divider consist of R_4 and R_5 is added, C_1 is also added to reduce the noise of the reference, R_6, R_7, C_2 are used to balance the two branches in bandgap core. The output reference after potential divider is given by

$$V_{ref}=\frac{R_4}{R_4+R_5}\left[V_{be1}+\frac{R_2}{R_1}V_T\ln(8)\right] \qquad (9)$$

Temperature compensation is achieved by appropriate choosing R_1, R_2, R_3 resistances ratio, which give:

$$\frac{\partial V_{ref}}{\partial T}=\frac{R_4}{R_4+R_5}\left[\left.\frac{\partial V_{be1}}{\partial T}\right|_{T=T_r}+\frac{R_2}{R_1}\ln(8)\left.\frac{\partial V_T}{\partial T}\right|_{T=T_r}\right]=0 \qquad (10)$$

In this design, R_1~R_5 are implemented in high poly resistor (HpolyR), the resistor ratio in (10) is temperature independent. So the negative temperature-coefficient of HpolyR has no effect on the temperature-coefficient of the output reference voltage, if they are appropriately sizing in design and matching in layout.

B. PSR Enhance Mechanism

The PSR of the bandgap voltage reference is improved with the PSR enhance stage [1], [8] consist of M_{10} and M_{11}. The PSR enhance stage not only increase loop gain, but also effectively feed the supply ripple into the PTAT loop, which benefits for PSR improvement as it has been stated in section Ⅱ. Conventional PMOS input two-stage opamp exhibits an excellent positive PSR [7]. So the ripple at the output of the opamp can be neglected, thus the PSR at node V_g in mainly depends on the "diode-connected" PSR enhance stage, the "diode-connected" M11 has a low impedance of $1/g_{m11}$, where g_{m11} is the transconductance of M_{11}. The PSR at node v_g is given by

$$A_{dd} = \frac{v_g}{v_{dd}} = \frac{r_{ds10}}{1/g_{m11} + r_{ds10}} \approx 1 = 0dB \qquad (11)$$

As indicated in (11) that the ripple from the positive supply can injected in node v_g without being attenuated, so, v_g follows the supply ripple, the gate-source voltage of M_1 and M_2 maintain constant although there is noisily ripple in the supply. As it's mentioned in section Ⅱ, this can improve the PSR of reference voltage. The simulated PSR of the bandgap voltage reference comparing with conventional one are shown in Fig. 3. The PSR enhance stage improve PSR about -38dB.

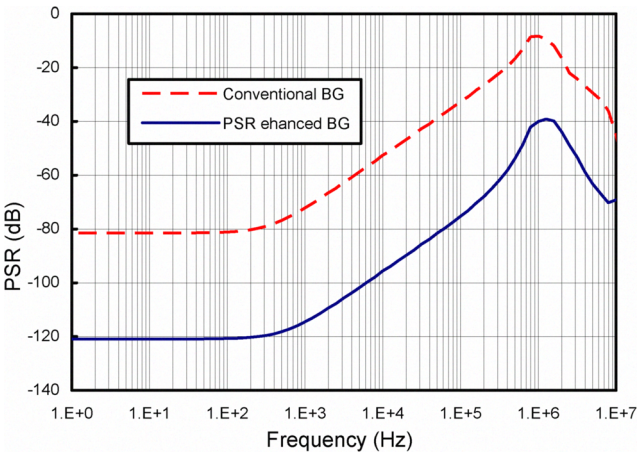

Fig. 3. Simulated PSR of the bandgap voltage reference

C. *Frequency Compensation*

Opamp based current mirror which has both positive and negative loops is used in PTAT loop, frequency compensation is required to make sure loop stability. As the output impendence of the PSR enhance stage is low, the pole at node v_g locate at high frequency which far beyond the unite gain frequency (UGF) of the feedback loop. C_c is utilized to achieve stability. The dominant pole locate at the output of the first stage, a nulling resistor R_c is utilized to move the RHP zero to LHP and locate it just beyond the UGF to improve phase margin [7]. The pole at the output of opamp becomes the first no-dominant pole. With the introduction of the PSR enhance stage, a smaller value of Cc is sufficient for stability, comparing the conventional one, due to the fact that the capacitor at opamp's output is much smaller comparing to the capacitor at node v_g. A smaller Cc is desirable respect to fast line transient response and startup time. The simulated loop gain is 84dB; GBW and phase margin are 5.62 MHz, 69 °, respectively.

D. *Startup Circuits*

A startup circuit is needed to driver the circuits to the desired operating condition during power on [7]. The startup circuit features zero power consumption is shown in Fig. 2. During power on, a current start to charge C_3, current mirror of M_{14} charges the gate of M_{13}, and turned M_{13} on to pull down node v_g, injecting current into the bandgap core to guarantee successfully startup. After startup, M_{12} is turned on then M_{13} cutoff. When C_3 is charged to a threshold voltage below the supply voltage, both M_{14} and M_{15} are cutoff, thus, the power consumption of the startup circuits is zero after startup. M_{16} is inserted to discharge C_3 when supply is turned down, in order to make sure properly startup next time.

IV. Experimental Result

A prototype of the bandgap voltage reference is fabricated in TSMC 0.6μm, double poly, double metal CMOS process. The N/PMOS threshold voltage in this technology is 0.78V and -0.98V, respectively. The microchip is illustrated in Fig. 4. The active silicon area is 0.07mm^2. The prototype is measured with HP4155A semiconductor parameter analyzer.

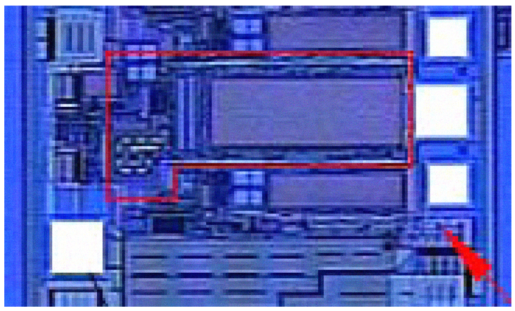

Fig. 4. Microchip of the bandgap voltage reference

The output characteristic of the bandgap voltage reference at different temperature is shown in Fig. 5. The result indicated that the reference output regulates at supply voltage down to 2V. The output voltage is 389.8mV at room temperature; and, the operating current at 100°C is 9μA, corresponds to 18μW power consumption at 2V supply voltage. The variation of output voltage for the supply voltage change from 2 to 5V is 0.16mV; the corresponding line regulation is 54μV/V.

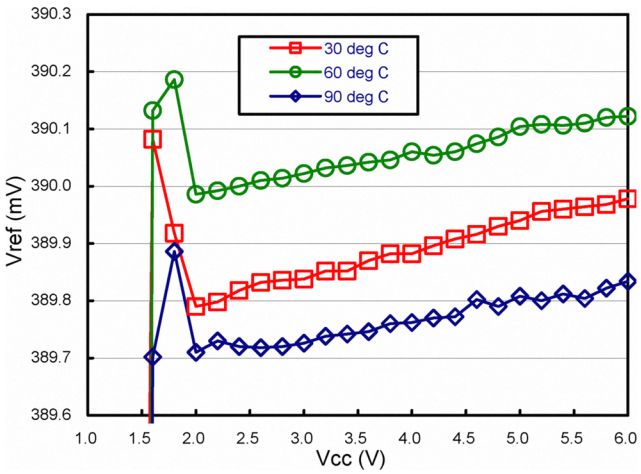

Fig. 5. Output characteristic of the bandgap reference

The temperature dependence of the bandgap reference is shown in Fig. 6. The output voltage variation in 0~100°C temperature range at different supply is less than 0.71mV. The temperature-coefficients at 2, 3, 4, 5V supply voltage are 15ppm/°C, 14.3ppm/°C, 13.4ppm/°C and 14.0ppm/°C, respectively.

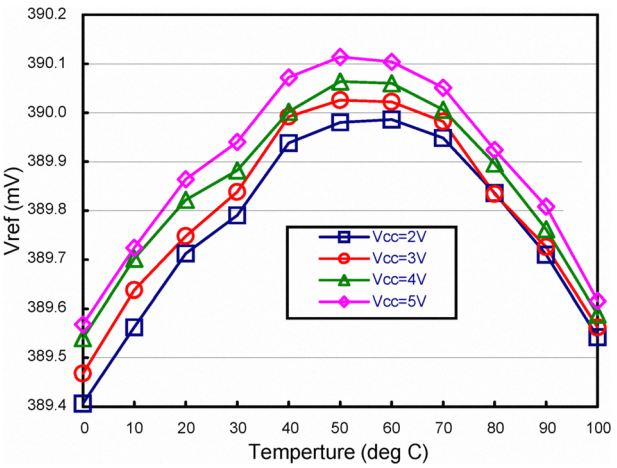

Fig. 6. Temperature dependence of the bandgap reference

The distribution of output reference voltage by measuring 25 samples without trimming @ 0°C, 30°C, 100°C temperature and @ 2V, 3V, 4V, 5V supply voltage respectively is shown in Fig. 7. The maximum, minimum, mean and standard deviation value of output reference voltage are 398.4mV, 378.0mV, 388.4mV and 4.1mV, respectively.

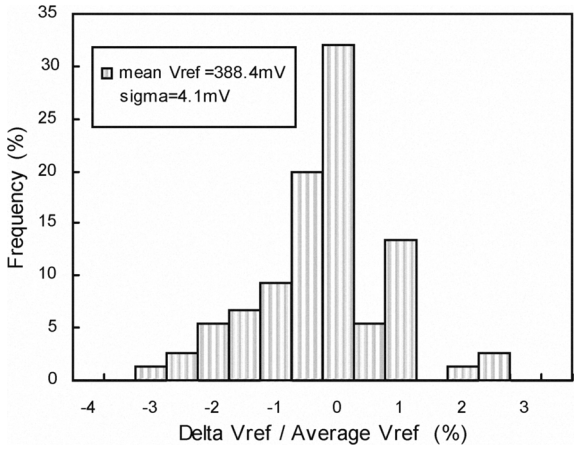

Fig. 7. Bandgap output voltage distribution

The PSR measurement result at room temperature is illustrated in Fig. 8. The upper tracks are 1V pick-to-pick sine supply ripple appending on a 4V DC power supply with the frequency of 100 kHz and 50 kHz, respectively; the lower tracks are the corresponded output reference ripple, which has been amplified by a 40dB low noise amplifier. The pick-pick ripple referred to the reference output is 304μV@ 100 kHz and 72μV@ 50 kHz, the corresponding PSR are -70.3dB @ 100 kHz and -82.8dB@ 50 kHz, respectively.

Summary performances of the bandgap voltage reference are tabulated in Table. 1.

V. CONCLUSION

A low power, low temperature-coefficient, high power PSR bandgap voltage reference is presented in this paper. It has been implanted in TSMC 0.6μm double poly double metal CMOS technology, occupying 0.07mm^2 active silicon areas. The maximum supply current is 9μA; temperature-coefficient is 15ppm/°C at 2-5V supply voltage; line regulation is 54μV/V, PSR are -70 dB@100 kHz and -82.8dB@ 50 kHz, respectively. The bandgap voltage reference is suitable for low power high PSR LDOs application.

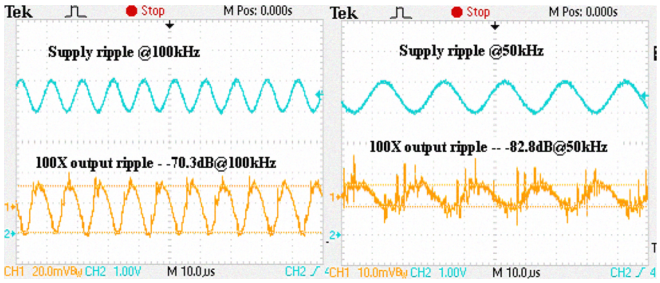

Fig. 8. Measured PSR at 100 kHz and 50 kHz

TABLE I
PERFORMANCE SUMMARY OF THE BANDGAP REFERENCE

Parameters	Symbol	Measured Result
technology	-	TSMC 0.6um DPDM CMOS
supply voltage	V_{dd}	2~5V
supply current	I_{dd}	9μA
output voltage	V_{ref}	389.8mV
TC@(0~100°C)	$\Delta V_{ref}/\Delta T$	15ppm/°C
line regulation	$\Delta V_{ref}/\Delta V_{dd}$	54μ/V
power supply rejection	PSR	-82.8dB@50kHz -70.3dB@100kHz
active silicon area	-	0.07mm^2

VI. ACKNOWLEDGMENT

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