A Curvature Compensated CMOS Bandgap Voltage Reference for High Precision Applications

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Abstract

This paper describes a high precision high order curvature compensated bandgap voltage reference in a 0.5-μm 2P3M n-well mixed signal CMOS technology. This newly proposed bandgap voltage reference utilizes a Buck's voltage transfer cell and a temperature independent current, to provide a high order compensation of the V_{BE}. Cascode structures are also introduced in this bandgap voltage reference to improve the power supply rejection ratio (PSRR). This circuit achieves 5.6 ppm/℃ of temperature coefficient with temperature ranging from -20 to 100℃ at 5V power supply. The variation in the output voltage of the bandgap voltage reference is 0.4mV when V_{DD} varies from 4V to 6V.

Index Terms — CMOS, analog integrated circuits, bandgap reference, low temperature coefficient, high order curvature compensation.

1. Introduction

Precision bandgap references (BGRs) are always in great needs in integrated analog, digital or mixed signal building blocks such as A/D converters, filters, DRAMs and flash memory controlling circuits for their high accuracy and temperature independence. There exists, however, a limit to improve the temperature coefficient (TC) of a first-order temperature compensated BGR[1] which exhibits TC limit typically between 20 and 100 ppm/℃[2][3], due to the non-linearity in the base-emitter voltage of the BJTs used in BGRs. To overcome this drawback, many high order temperature compensation techniques have been developed, such as quadratic temperature compensation by Song et al.[4][5], exponential temperature compensation by Lee et al. [6], piecewise linear curvature correction by Rincon-Mora et al.[7], and temperature dependent resistor ratio with high resistive poly resistor and a diffusion resistor by Leung et al.[8][9]. With these techniques, the temperature stability of the BGRs has been increased significantly. However, the above BGR structures require precision matching of current mirrors or a pre-regulated supply voltage to implement the advanced mathematical functions with high accuracy, as current mismatch will introduce an error voltage at the reference output. On the other hand, high resistive poly resistor cannot be fabricated under conventional standard CMOS processes.

A high order curvature compensated bandgap voltage reference based on a temperature independent current and a Buck's transfer cell [10][11] is presented in this paper. The proposed BGR utilizes a conventional BGR, a temperature independent current and an inverse function voltage transfer cell first proposed by A. E. Buck et al. to implement a very low TC bandgap reference. This circuit structure can effectively reduce the temperature drift of the bandgap voltage reference. Cascode current mirrors can help improve the high PSRR. The novel proposed BGR has a stable reference output V_{ref} of 1.196V and TC of 5.6 ppm/℃ over a temperature range of -20 to 100℃ under supply voltage 5V.

This paper starts with a brief introduction to conventional bandgap reference in Section 2. An analysis on the temperature dependence of the emitter-base voltage is given in Section 3. The proposed high precision high order curvature compensated CMOS bandgap voltage reference is introduced in Section 4. Simulation results and conclusion are presented in Sections 5 and 6, respectively.

2. Conventional Bandgap Voltage Reference

The conventional BGR is a weighted sum of a negative TC voltage V_{BE} which is the forward-bias voltage across a p-n junction, and a positive TC voltage V_T which is the thermal voltage kT/q, proportional to absolute temperature (PTAT), shown in Fig. 1, where M is the adjusted weighted factor. The output voltage reference should be insensitive to temperature changes and stable over the range of supply voltage change in the first-order compensation.

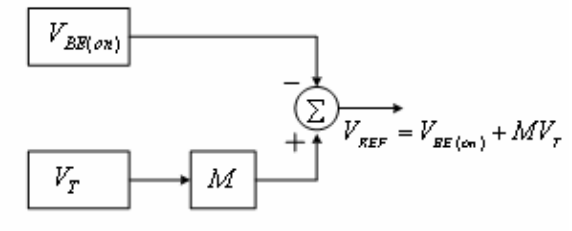

Fig. 1 Conventional BGR overview

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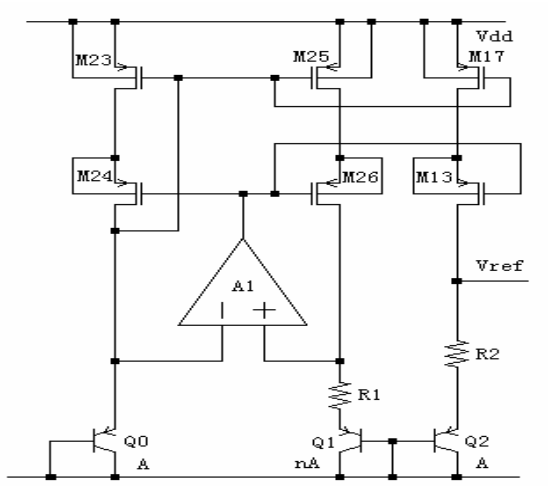

Fig.2 A typical implementation of conventional BGR

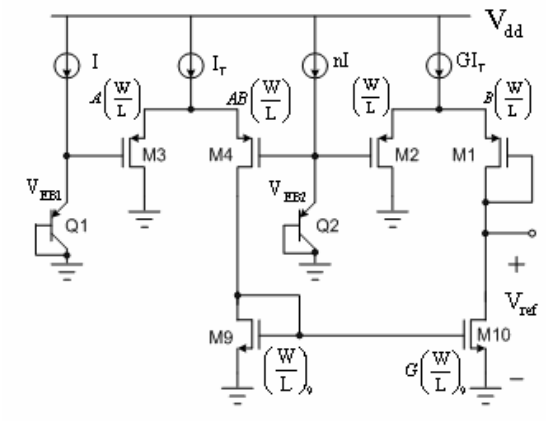

Fig. 3 Buck's voltage transfer cell.

A typical implementation of the conventional bandgap voltage reference in CMOS technology is shown in Fig. 2 [12]. A current which is proportional to the absolute temperature (PTAT) is generated and the voltage drop across the resistance R2 formed, and then added onto the base-emitter voltage of Q2. Thus, the output of V_{ref} is

$$V_{ref} = V_{EB2} + \frac{R_2}{R_1}\left(\frac{kT}{q}\right)\ln n \qquad (1)$$

where k is the Boltzmann's constant, q is electronic charge, and T is the absolute temperature in degrees Kelvin (K). The second item is proportional to the PTAT, which is used to compensate for the negative TC of V_{EB2}. The factor n is the emitter area ratio of transistors Q1 and Q0.

3. V_{EB} Temperature Dependence

The main goal of the first-order compensated BGR is to cancel the negative temperature dependence of the emitter base voltage V_{EB} (pnp) by adding a PTAT voltage, which is a fully linear function of T. The relationship between V_{EB} and T, however, is a nonlinear behavior, and V_{EB} is a complex function of T containing many higher order items. Therefore, even in the optimally compensated case, the output reference voltage V_{ref} has some temperature drift terms. Since this drawback is inherent, it is impossible to increase the temperature stability of the first order compensated BGR above a certain limit.

The temperature characteristic of V_{EB} is studied extensively and its analytical form can be expressed by the following [1][9][13][16].

$$V_{EB} = V_G(T_o) + \left[V_{EB}(T_o) - V_G(T_o)\right]\left(\frac{T}{T_o}\right) - (\eta - m)\left(\frac{kT}{q}\right)\ln\left(\frac{T}{T_o}\right) \qquad (2)$$

where V_G is the bandgap voltage of silicon extrapolated at 0 K, k is the Boltzmann's constant, η is a temperature constant depending on the technology, m is the order of the temperature dependence of the collector current, q is the charge of an electron, and T_o is the reference temperature.

From (2), there is a $T\ln T$ term, which is the high order nonlinear temperature dependence factor of V_{EB}. First order temperature compensation involves the cancellation of the T term while high order temperature compensation involves the cancellation of high order T terms. In this paper, we will cancel the second order term of V_{EB} by adding a voltage, which is proportional to the square of the absolute temperature ($PTAT^2$).

4. Proposed Precision Curvature compensated CMOS BGR

4.1 Buck's Voltage Transfer Cell

The principle in Buck's voltage transfer cell is shown in Fig.3. The parameter A is the ratio of the size of the differential pairs M3-M4 and M2-M1, and the parameter G is the current-mirror gain from M9 to M10 as well as the ratio of the tail currents of the two differential pairs. The required gain, i.e. the weighted factor M, is obtained by using ratio transistors and the inverse function technique—transconductance and transresistance [14]. The differential pair M3-M4 acts as a transconductance. The resulting current is multiplied by G using current mirror M9-M10 and is delivered to another differential pair M2-M1, which functions as a transresistance due to the negative feedback around M1.

The main idea in the inverse function technique is to apply a pair of functions—transconductance g_{mc} and transresistance g_{mr} to $\Delta V_{BE} = (V_{BE2}\text{-}V_{BE1})$ so that $g_{mr}[g_{mc}\Delta V_{BE}] = M\Delta V_{BE}$. g_{mc} (possibly nonlinear) maps ΔV_{BE} to

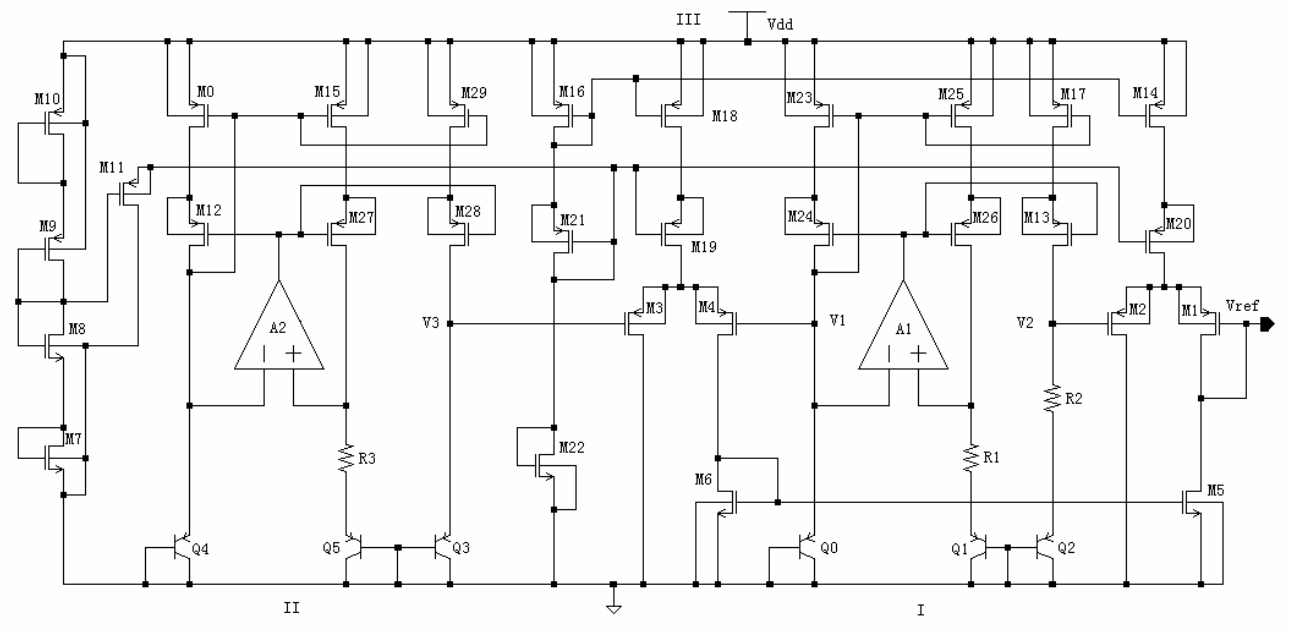

Fig. 4 The proposed complete schematic of the high order curvature compensated BGR

some current i, and then g_{mr} cancels the nonlinearity in i and provides the required gain M. The inverse function technique operates with any smooth nonlinearity [10][11][15].

The MOSFET transistors operate in the saturation region, and the channel length modulation effect of the transistors is neglected here because of their long channel lengths used in this circuit. From Fig.3, we have the following equations.

$$I_T = \frac{1}{2}\mu_p C_{OX}\left(\frac{W}{L}\right)\left[A\left(V_{GS3}-V_t\right)^2 + AB\left(V_{GS4}-V_t\right)^2\right] \quad (3)$$

$$GI_T = \frac{1}{2}\mu_p C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{GS2}-V_t\right)^2 + B\left(V_{GS1}-V_t\right)^2\right] \quad (4)$$

$$GI_4 = I_1 \quad (5)$$

Combining equations(3), (4) and (5) gives

$$V_{GS2}-V_t = \sqrt{AG}\left(V_{GS3}-V_t\right), \quad (6)$$

$$V_{GS1}-V_t = \sqrt{AG}\left(V_{GS4}-V_t\right). \quad (7)$$

Equation (7) minus equation (6) results in

$$V_{GS1}-V_{GS2} = \sqrt{AG}\left(V_{GS4}-V_{GS3}\right) \quad (8)$$

also

$$V_{GS4}-V_{GS3} = V_{EB2}-V_{EB1} = \Delta V_{EB} \quad (9)$$

Therefore, the output voltage reference is

$$V_{ref} = V_{EB2} + \sqrt{AG}\Delta V_{EB} \quad (10)$$

4.2 Implementation of High Order BGR

The proposed complete circuit which is mainly composed of three parts is shown in Fig. 4.

Part I of the BGR generates a voltage V_2 as following

$$V_2 = V_{EB2} + \frac{R_2}{R_1}\left(\frac{kT}{q}\right)\ln n \quad (11)$$

Part II of the BGR produces a temperature independent current injected into Q3. Q0 has the same emitter area as Q3, and the current of Q0 is proportional to T. According to equation (2), V_{EB0}-V_{EB3} can be expressed as following

$$V_1 - V_3 = V_{EB0} - V_{EB3} = \left(\frac{kT}{q}\right)\ln\left(\frac{T}{T_o}\right) \quad (12)$$

Part III of the BGR is the Buck's voltage transfer cell given in subsection 4.1. Combining equations (8), (11) and (12) yields

$$\begin{aligned} V_{ref} &= V_2 + \sqrt{AG}\left(V_1 - V_3\right) \\ &= V_{EB2} + \frac{R_2}{R_1}\left(\frac{kT}{q}\right)\ln n + \sqrt{AG}\left(\frac{kT}{q}\right)\ln\left(\frac{T}{T_o}\right) \end{aligned} \quad (13)$$

V_{EB2} can thus be compensated by both first order (linear) and second order (nonlinear) items in this proposed BGR. A precision curvature compensated BGR can be achieved by trimming the ratio of resistors R1 and R2, and parameters A and G..

4.3 V_{DD} Variation Effect on Bandgap Reference

The bandgap reference is required to be stable over the change of the power supply voltage. Therefore, the less the effect of power supply V_{DD} on the bandgap reference is, the better the performance of the bandgap reference is. We use cascode current mirror structures, which is supply voltage independent to a certain extent and may greatly reduce the variation of the power supply V_{DD}, to bias the bipolar transistors in order to improve the PSRR in this proposed BGR circuit.

5. Simulation Results

The temperature behavior of the proposed BGR output is shown in Fig. 5. The output voltage V_{ref} of the proposed BGR is 1.196±0.0004V with temperature ranging from -20 to 100℃ and supply voltage 5V. Its temperature coefficient is 5.6 ppm/℃. Fig. 6 shows that the reference voltage variation of the proposed BGR is 1.196 ± 0.0004V when the power supply varies from 4 to 6V.

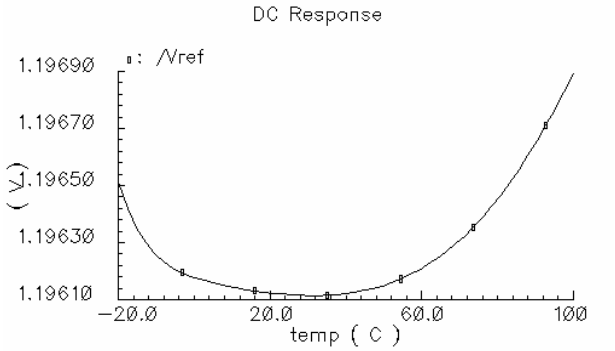

Fig. 5 Output reference V_{ref} vs. temperature.

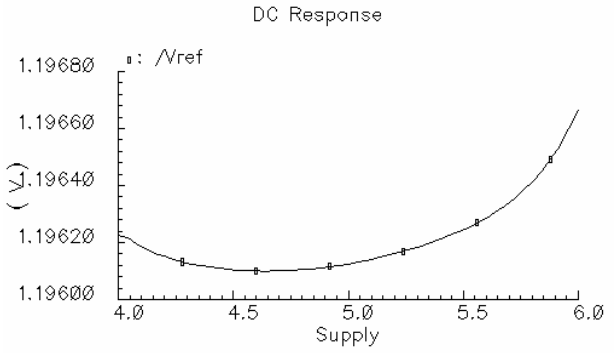

Fig. 6 Output reference V_{ref} vs. power supply V_{DD}.

6. Conclusion

A high precision high order curvature compensated CMOS bandgap voltage reference has been proposed. The temperature compensation is achieved by a Buck's voltage transfer cell and a temperature independent current which introduces a voltage proportional to $T\ln T$, giving a high order compensation of V_{BE}. The TC of this proposed circuit is only 5.6 ppm/℃ with temperature ranging from -20 to 100℃ at power supply 5V in a 0.5-μm 2P3M n-well mixed signal CMOS technology. The variation of the BGR output is only 0.4mV when V_{DD} varies from 4V to 6V because it can be immune from the supply voltage variation by the cascoded current mirror. The proposed BGR is well suited for many mixed signal systems which require high precision.

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