A CMOS Transconductance Amplifier Architecture With Wide Tuning Range for Very Low Frequency Applications

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***Abstract*—A pseudodifferential CMOS operational transconductance amplifier (OTA) with wide tuning range and large input voltage swing has been designed for very small G_M's (of the order of a few nanoamperes per volt). The OTA is based on a modified four-quadrant multiplier architecture with current division. A common-mode feedback circuit (CMFB) structure has been proposed and designed using floating-gate transistors to handle large differential signals. Large on-chip capacitors are emulated through impedance scaling circuits. The circuits, fabricated in a 1.2-μm CMOS process, have been used to design a fourth-order bandpass filter and a relaxation oscillator. Experimental results are in good agreement with the theoretical results.**

***Index Terms*—CMFB, current division, floating gate, low-frequency circuits, OTA, small G_m.**

I. Introduction

FOR BIOMEDICAL electronics, active filters with very low cutoff frequencies are often found necessary due to the relatively slow electrical activity of the human body [1], [2]. A key application area for low-frequency signal processing is ramp generation for testing the static characteristics of analog-to-digital converters [3], [4]. An on-chip ramp generator allows the designer to make histogram and monotonic tests. Thus, there is a strong motivation for creating integrated solutions for circuits that are capable of operating at very low frequencies. For an operational transconductance amplifier-capacitor (OTA-C) filter implementation, such low frequencies imply large capacitors and very low transconductances [5]. There are two independent aspects to the problem. One involves OTA design with very low transconductance and high linearity, while the other is the realization of very large capacitors (typically of the order of several hundred picofarads) on chip. Frequently, OTAs designed for low-frequency applications operate in weak inversion, reducing further their linear range and making current mirrors sensitive to parameter variations. The proposed OTA employs transistors operating in the triode and saturation regions.

II. Pseudodifferential OTA and CMFB Circuit

The transconductance amplifier's topology is based on the pseudodifferential $V_{\rm GS}V_{\rm DS}$-type four-quadrant multiplier [6]. The basic idea behind this topology, using n-type devices, is shown in Fig. 1. Each branch implements a single-quadrant multiplier. Transistors M_1 operate in triode region and M_2 operate in saturation with proper bias voltages V_X and V_Y. M_2 operates as a source follower and injects the small-signal v_y into the drain

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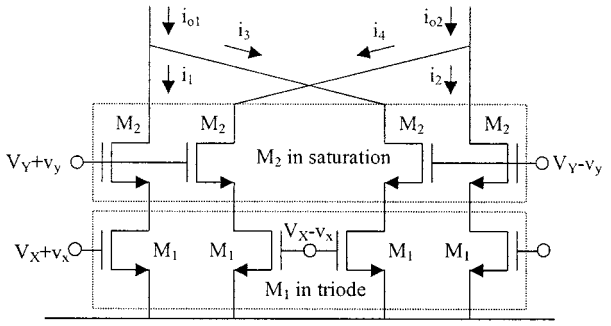

Fig. 1. Basic topology of the four-quadrant multiplier.

of M_1, thus modulating its drain current. The total differential output current $i_{\rm od}(i_{\rm od}=i_{\rm o1}-i_{\rm o2})$ is proportional to the product v_xv_y. This architecture has been modified to include the current division scheme [7] in order to reduce the transconductance gain of the multiplier even further. The complete schematic of the transconductance multiplier is shown in Fig. 2.[1] Basically, M_2 is split into two nonequal halves, M_2 and kM_2, thus splitting the current through them in the ratio 1:k. The current through M_2, which is smaller than the current before splitting by the factor $k+1$, is mirrored to the output, thus reducing the transconductance by the same factor. Transistors M_3 are simple current mirrors that are used to produce the differential output currents. The differential output current of the multiplier [6] is

$$i_{\rm od}=i_{\rm op}-i_{\rm on}=\left(\frac{8\mu C_{\rm ox}W}{L}\right)_{M1}\left(\frac{1}{k+1}\right)v_xv_y \qquad (1)$$

where $i_{\rm od}$ is the small-signal differential output current and the suffix M_1 indicates transistor M_1, and k is the scaling constant. If one of the signals v_x or v_y is kept constant, the other is varied, thus the multiplier can be used as a programmable transconductance amplifier whose G_M can be varied. For this application, it is more convenient to choose v_y as the input signal because the common-mode input voltage can be larger. The nominal v_x value for our design is 100 mV, V_X is -1 V for a supply of $\pm$1.5 V, and nominal G_M is 1 nA/V ($k=49$). The maximum input swing $2v_y$ is 1 $V_{\rm pp}$ and v_x can be varied in the range $\{$5–500 mV$\}$, thus yielding two decades of transconductance tuning range. There is a tradeoff between signal swing v_y and tuning range v_x; larger v_y implies smaller v_x and vice versa. From (1), the effective differential $G_{M_{\rm d}}$ of the OTA is

$$G_{M_{\rm d}}(v_x)\equiv\frac{i_{\rm od}}{2v_y}=\left[\left(\frac{4\mu C_{\rm ox}W}{L}\right)_{M_1}\left(\frac{1}{k+1}\right)\right]v_x. \qquad (2)$$

[1]Note that in Fig. 2 the driving transistors M_1, M_2, kM_2 are p-type in order to reduce flicker noise.

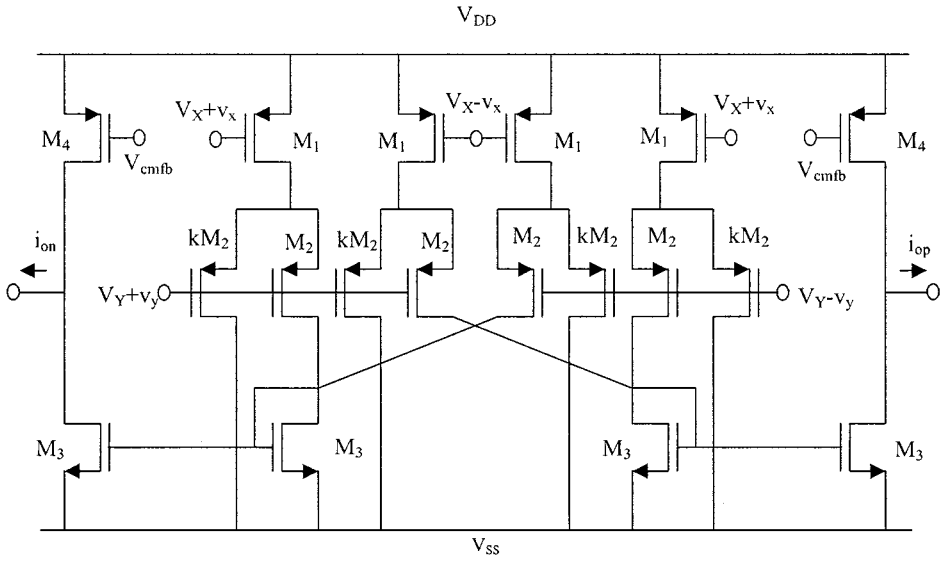

Fig. 2. Multiplier-based OTA.

TABLE I
TRANSISTOR SIZES FOR MULTIPLIER-BASED OTA

OTA	M_1	M_2	kM_2	M_3	M_4
Width (μm)	3.6	3.6	(49) 3.6	3.6	3.6
Length (μm)	120.0	120.0	120.0	124.8	300.0

CMFB	$M_{1,2,3,4}$	$M_{5,6}$	$M_{7,8}$	$M_{9,10,11}$
Width (μm)	3.6	3.6	3.6	3.6
Length (μm)	90.0	28.2	300.0	3.6

$G_{M_{\rm d}}$ is linearly programmable with the tuning voltage v_x, which can be theoretically varied from 50 pA/V ($v_x = 5$ mV) to 5 nA/V ($v_x = 500$ mV).

Noise is dominated by the flicker components due to both the very low-frequency application and the use of large equivalent capacitors. This last fact allows us to increase the overal OTA small-signal transconductance and to reduce the thermal noise components. Noise components generated by transistors M_1 and kM_2 are further reduced by the current divider, therefore, noise is dominated by the flicker noise components due to M_2, M_3, and M_4. Input-referred noise density is approximated as

$$v_{\rm eq-in}^2 \approx 4\left(\frac{g_{m2}}{G_m}\right)^2 v_{M_2}^2 + 4\left(\frac{g_{m3}}{G_m}\right)^2 v_{M_3}^2 + 2\left(\frac{g_{m4}}{G_m}\right)^2 v_{M_4}^2 \quad (3)$$

where $v_{M_{2,3,4}}^2$ ($= K_{\rm f} I_{\rm DRAIN}/WLf$, $K_{\rm f}$ being the flicker coefficient) is the noise contribution of $M_{2,3,4}$. The overall OTA transconductance is very small, usually g_{m2}, g_{m3}, and g_{m4} are greater than G_m. The gate areas (around 120×3.6 μm^2) in (3) and bias current (around 0.5 nA for $G_m = 1$ nA/V) are optimized to reduce their flicker noise contributions. Transistor mismatches produce differential and common-mode offset voltages. While common-mode offsets are reduced by the common-mode feedback circuitry, differential offsets are not accumulated by the fourth-order bandpass filter, since dc signals are inherently reduced by the overall (bandpass) transfer function. In addition, the most critical transistors are laid out using known matching techniques. Table I lists the OTA transistor sizes.

Since this topology is differential, a common-mode feedback circuit (CMFB) is required to stabilize the common-mode output levels of both branches. Several CMFB structures are discussed in [8]. Since the OTA was designed for high input/output swing (1 $V_{\rm pp}$), it was necessary for the input stage of the CMFB circuit to have a high input-swing handling capability. Although the proposed OTA could also be used for the CMFB, we decided to investigate the floating-gate OTA as an alternative approach. A simple circuit model used for simulating floating-gate transistors [9] is shown in Fig. 3. For SPICE to calculate dc operating points correctly, very large resistors (of the order of $10^{15}\Omega$) are added in parallel to the capacitors. In practice, these resistors are not required since the dc voltage is fixed by both CMFB and initial conditions of the floating gate. If the control-gate capacitors are designed such that they are sufficiently larger than the parasitic capacitors $C_{\rm fgs}$, $C_{\rm fgd}$ and $C_{\rm fgb}$ and assuming that the fixed charge on the floating gate is very small, then the floating-gate voltage yields

$$V_{\rm fg} \approx \left(\frac{C_1}{C_1 + C_2}\right) V_{\rm cg1} + \left(\frac{C_2}{C_1 + C_2}\right) V_{\rm cg2}. \quad (4)$$

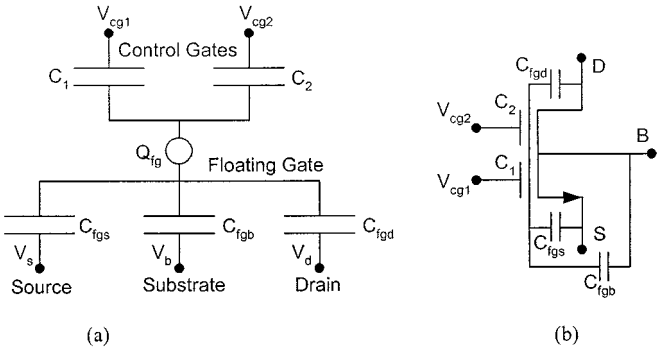

Fig. 3. (a) Equivalent circuit model for a two-input floating-gate transistor. (b) Floating-gate transistor symbol.

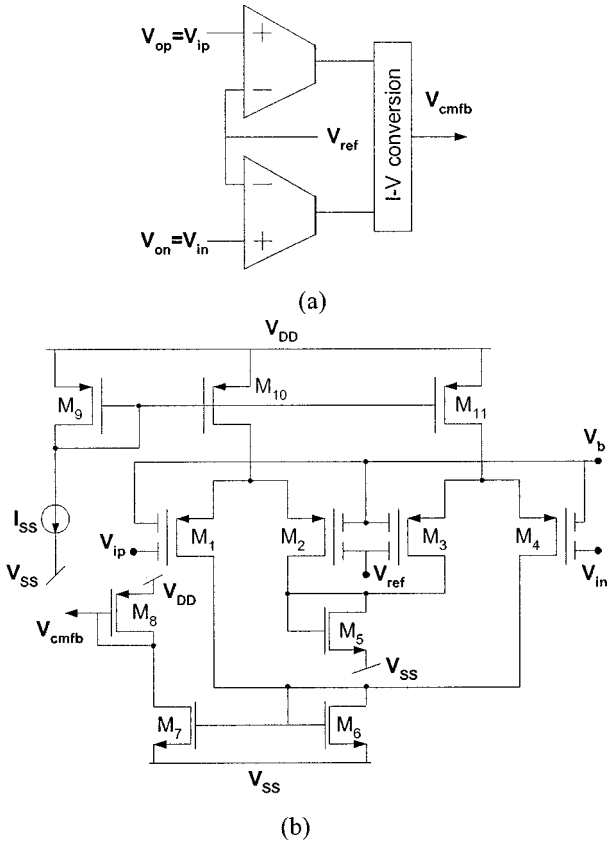

Fig. 4. Common-mode feedback circuit. (a) Block diagram. (b) Circuit using floating gates.

This voltage attenuation factor allows us to apply larger signals to the control gate. The concept behind CMFB and the schematic of the CMFB circuit are shown in Fig. 4. The input stage M_1–M_4 performs the task of both common-mode detection and comparison at the same time. If the common mode of the input signal $V_{\rm cm}$ equals the desired common-mode $V_{\rm ref}$, then the total current through M_6 remains constant at I_{SS} and the output voltage $V_{\rm cmfb}$ remains fixed. On the other hand, if $V_{\rm cm}$ is not the same as $V_{\rm ref}$, then an ac current $i_{\rm cm} = g_{m1}(V_{\rm cm} - V_{\rm ref})$ flows through M_6 which causes $V_{\rm cmfb}$ to change accordingly. $V_{\rm cmfb}$ is injected into the main OTA at a node $V_{\rm cmfb}$ in Fig. 2 such that the direction of change of $V_{\rm cmfb}$ makes the output common mode come back to the desired value $V_{\rm ref}$. The voltage $V_{\rm b}$ allows us to set the dc level

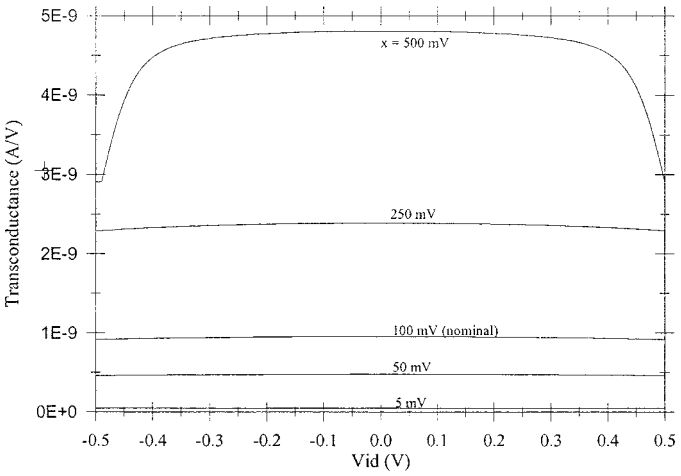

Fig. 5. Simulated small-signal transconductance for different tuning voltages.

of the floating gate for optimal operation. The bias current for the CMFB is about 0.1 μA, and the nominal value for $V_{\rm b}$ is -0.75 V. One attractive feature of the circuit of Fig. 4 is that it is fairly insensitive to the trapped charge on the floating gate. This is because all the four input transistors are similar floating-gate devices, and it is reasonable to assume that the trapped process charge would be about the same on all devices, provided they are laid out close to each other. After the voltage comparison, this leads to cancellation of the effect of trapped charges due to the nature of the differential-pair-based CMFB. The various transistor sizes for the CMFB cell are also listed in Table I. The simulated dc transfer characteristics of the OTA, including the CMFB, for different tuning voltages is shown in Fig. 5. The tuning voltage v_x has been varied in the range $\{\pm 5$ mV, ± 50 mV, ± 100 mV, ± 250 mV, ± 500 mV$\}$, while the small-signal transconductance changes by two decades, 0.05–5 nA/V. Additional simulations performed for the OTA with $G_m = 1$ nA/V show us that the harmonic distortion component $\rm HD_3$ is less than 1% for a differential input signal of 2 $\rm V_{pp}$. Input-referred noise integrated from dc up to 1 Hz is around 110 $\mu \rm V_{rms}$, leading to a signal-to-noise ratio (SNR) of around 75 dB.

III. Fourth-Order Bandpass Filter

A 0.8-Hz fourth-order bandpass filter has been designed using the proposed OTA. The filter is realized here as a cascade of two identical second-order blocks. In order to set $\omega_0 = 2\pi \times 0.8$ rad/s with $g_{m1} = 1$ nA/V, we need capacitors in the range of 180 pF. Techniques to scale grounded impedances up or down are discussed in [10]. The basic idea behind scaling impedance down and the circuit are illustrated in Fig. 6. If the transconductance of the diode-connected transistor is large enough, the ac current $i_1 = v_i/Z$. This current is gained up by the factor N of transistor sizing and added to i_1 to generate the total ac current i_i. For the case of capacitors, this translates to an increase in the effective capacitance $C_{\rm eq}$, which is given by

$$C_{\rm eq} = (N+1)C. \tag{5}$$

For the design of the impedance multipliers, mainly two factors need to be considered: noise and accuracy. Notice in Fig. 6 that

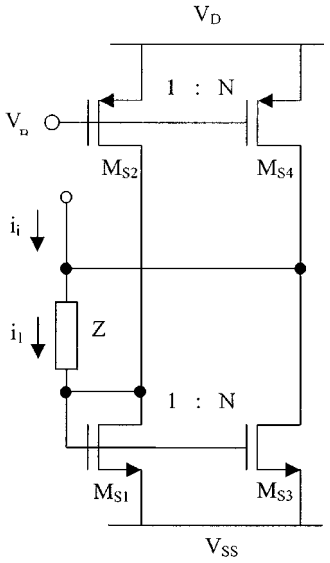

Fig. 6. Impedance scaling scheme, simplified circuit implementation.

the noise contributions of the diode-connected transistor and its bias current source are the most critical ones. The input referred noise becomes

$$v_{\mathrm{eq-in}}^2 \approx N^2 \left[\left(\frac{g_{ms1}}{G_m} \right)^2 v_{MS1}^2 + \left(\frac{g_{ms2}}{G_m} \right)^2 v_{MS2}^2 \right]. \quad (6)$$

Therefore, the transconductance of the transistors used for the impedance multiplier implementation should be minimized. Similar to the main OTA, increasing gate areas and limiting the bias current reduces flicker noise contributions. The bias current for the multiplier is about 1 nA and the basic unit transistor size is about 3.6 μm/300 μm. Transistor mismatches are minimized using replicas of unit transistor size and doing a careful layout. The two-integrator loop filter is shown in Fig. 7. The voltage transfer function for the V_{bp} node is given by

$$\frac{V_{\mathrm{bp}}(s)}{V_{\mathrm{id}}(s)} = \frac{\left(\frac{g_{m3}}{C_1} \right) s}{s^2 + \left(\frac{g_{m2}}{C_2} \right) s + \frac{g_{m1}^2}{C_1 C_2}}. \quad (7)$$

The filter's ω_0, Q, and peak gain can be set by g_{m1}, g_{m2}, and g_{m3}, respectively. Since the small-signal OTA transconductance is linearly dependent on the tuning voltage v_x, the appropriate tuning voltages can control these parameters. The tuning voltage v_x was varied from 50 to 500 mV to yield a variation of the center frequency of the filter from 0.6 to 6 Hz.

IV. Relaxation Oscillator

The OTA has also been used for the design of the fully differential relaxation oscillator [11], shown in Fig. 8. The circuit is essentially an integrator in series with a Schmitt trigger in a positive feedback loop. The comparator's outputs and resistors R_1 and R_2 fix the threshold levels of the Schmitt trigger. The comparator is a two-stage amplifier with an inverter at its output to boost the output driving capabilities. A differential comparator

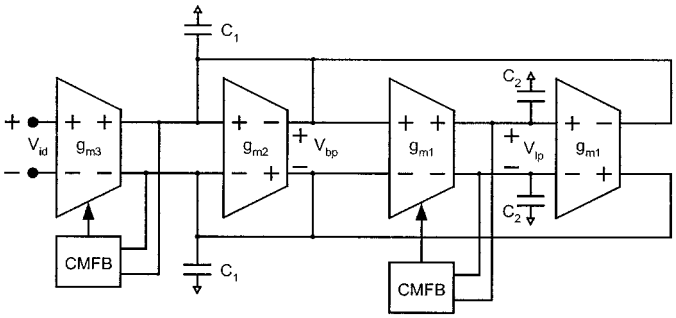

Fig. 7. Block diagram of the second-order OTA-C filter.

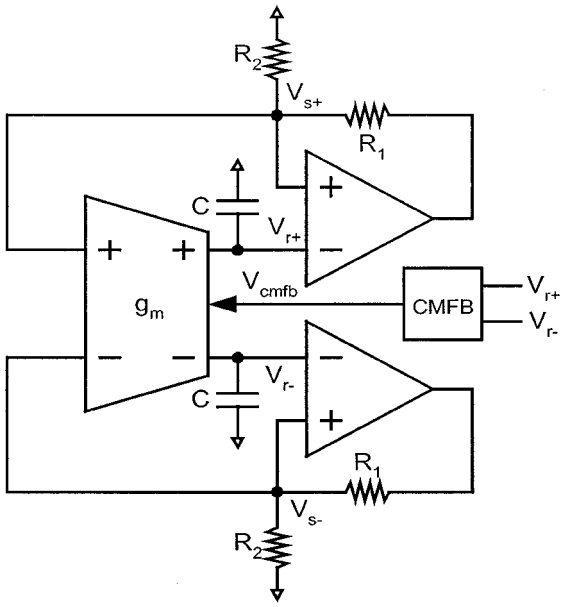

Fig. 8. Relaxation oscillator.

could be used, but the emphasis here is more on the OTA itself with the oscillator being used as a test vehicle. The comparator operates at a quiescent current of 0.1 μA. The voltage across the capacitors V_{r+} and V_{r-} of Fig. 8 linearly change with time, and when they cross the threshold voltages V_{s+} and V_{s-}, the comparators trip and the voltage across the capacitors then changes linearly with time in the opposite direction. Thus, we have square-wave oscillations at the nodes V_{s+} and V_{s-} and triangular-wave oscillations at the nodes V_{r+} and V_{r-}. The frequency of the oscillations and the slope of the triangular wave are given by

$$f_{\mathrm{o}} = \frac{g_m}{4C} \quad (8)$$

$$\left(\frac{dV}{dt} \right) = \frac{g_m}{C} \left(\frac{R_2}{R_1 + R_2} \right) (V_{DD} - V_{SS}) \quad (9)$$

where g_m is the differential transconductance of the OTA, C is the effective integrating capacitor, and R_1 and R_2 are the external Schmitt trigger resistors. The oscillation frequency is controlled only by the integration constant (g_m/C) while the slope of the triangular wave depends on the integration constant, the resistor ratio (R_1/R_2), and the supply voltages V_{DD} and V_{SS}.

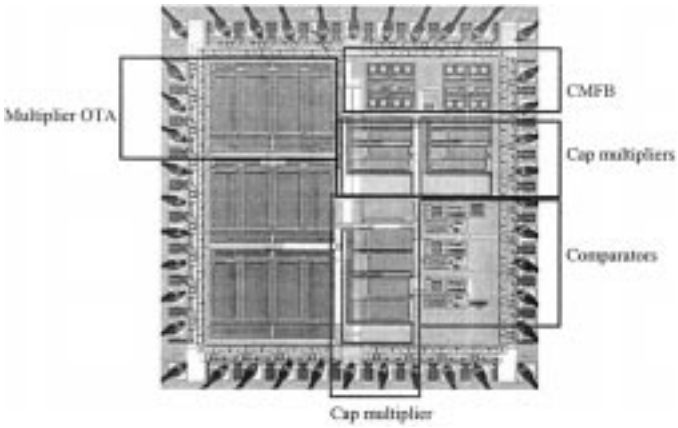

Fig. 9. Relaxation oscillator chip microphotograph.

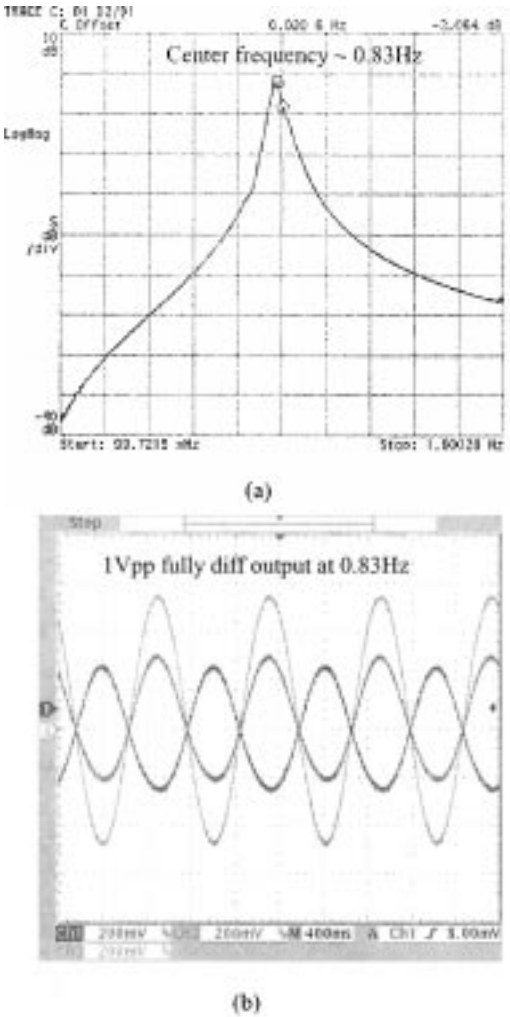

Fig. 10. (a) Measured magnitude response of the fourth-order bandpass filter. (b) Transient outputs.

V. Experimental Measurements

The above-described circuits have all been fabricated in a 1.2 μm CMOS process available through MOSIS. The total available die area is 1.9 mm $\times$ 1.9 mm. The chip microphotograph of the oscillator die is shown in Fig. 9. The measured frequency response for the differential output of the fourth-order bandpass filter is shown in Fig. 10(a). The integrated output noise within the -3 dB passband of the filter is about 210 $\mu V_{\rm rms}$. The single-ended and differential outputs are depicted in Fig. 10(b). A differential offset of around 20 mV can be observed in this figure. Notice that the common-mode offset is of the same order of magnitude, showing that the common-mode feedback system is properly controlling the dc output voltages. The measured results for the fourth-order filter are summarized in Table II.

TABLE II
Summary of Measured Results for the Fourth-Order Filter

PARAMETER	VALUE
Center frequency f_0	0.83 Hz
g_m tuning voltage V_x	100mV
Center frequency range	0.1-5.0 Hz
-3dB bandwidth	0.04 Hz
Peak gain	3.8 dB
IM3 @ V_{in}=1Vpp	-40 dB
Total in-band input noise	210 μVrms
SNR (dB)@ *IM3*= -40dB	64.6 dB
Power consumption	27.86 μW
Power supply	±1.50 V

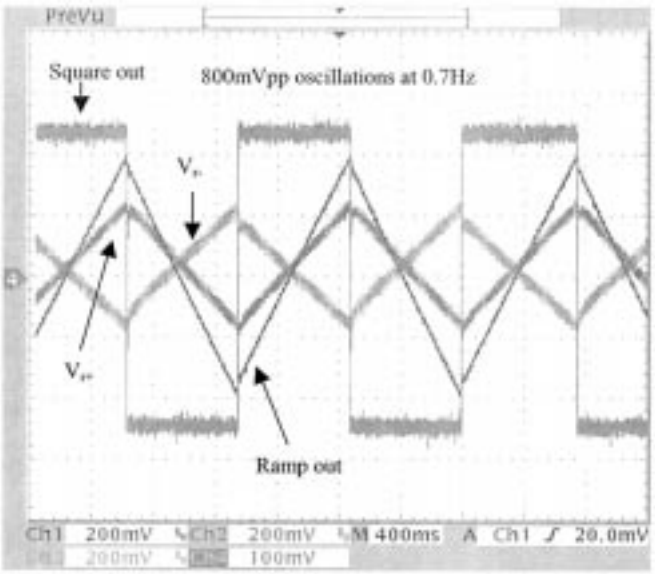

Fig. 11. Square and triangular oscillations at 0.7 Hz.

The transient performance of the relaxation oscillator was also tested, and Fig. 11 shows the square and triangular oscillations. The power supply is $\pm$1.5 V, the power consumption is 5.57 μW, and the total oscillator area is 2.16 mm^2. The frequency of oscillation is 0.7 Hz and it can be programmed in the range of 0.2–5 Hz. The measured slope deviation is about 4.5%, mainly due to process parameter tolerances. The error may also be attributable to the nonlinearity of the capacitor multiplier and the finite output impedance of the OTA. Better linearity may be

possible with the use of cascode stages for the capacitor multiplier and for the OTA at the cost of signal swing. The measurements shown in Fig. 11 were susceptible to 60-Hz ac noise components in our measurement equipment which could not be filtered out completely.

VI. Conclusion

This paper has presented a wide-tuning OTA based on a four-quadrant $V_{GS}V_{DS}$-type multiplier architecture with the topology modified to include current division yielding very small transconductances. The main features of this OTA are the wide input signal range and wide transconductance gain tuning range (theoretically, two decades) with nonweak inversion operation. Practical impedance scaling techniques to emulate large on-chip capacitors have also been discussed. The OTA along with the impedance scalers have been used to design an integrated fourth-order bandpass filter and a relaxation oscillator. Theoretical and experimentally measured results are in good agreement.

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