Status of the VME-based electronics for the JLab GEM tracker

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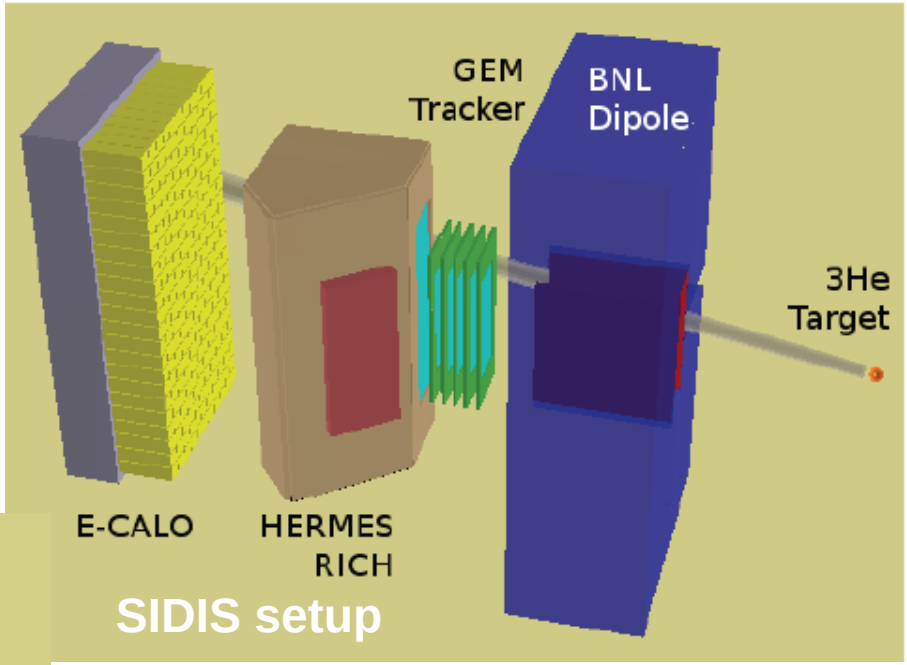
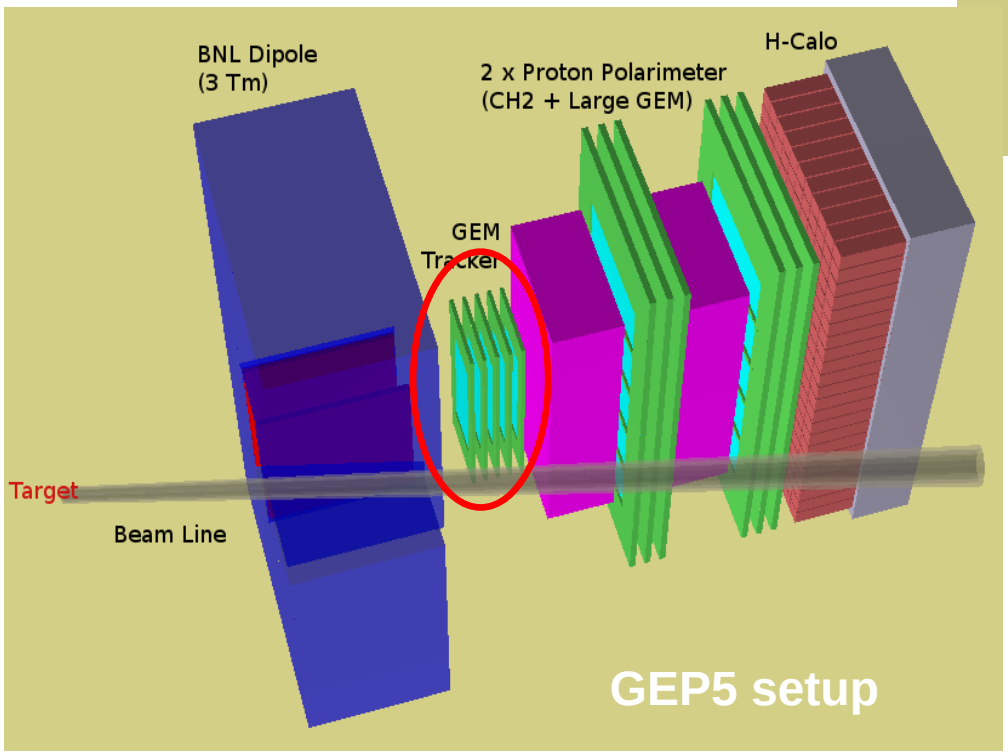
RD51 Collaboration Meeting

New SBS Spectrometer @ JLab

- High Luminosity (10^{38} /cm^2/s) (bg 400 kHz/cm^2)
- Forward angle
- Large acceptance
- Good angular and momentum resolutions (0.2 mrad, 0.5% @ 4-8 GeV/c)
- Flexibility (use the same detectors in different experimental setup)





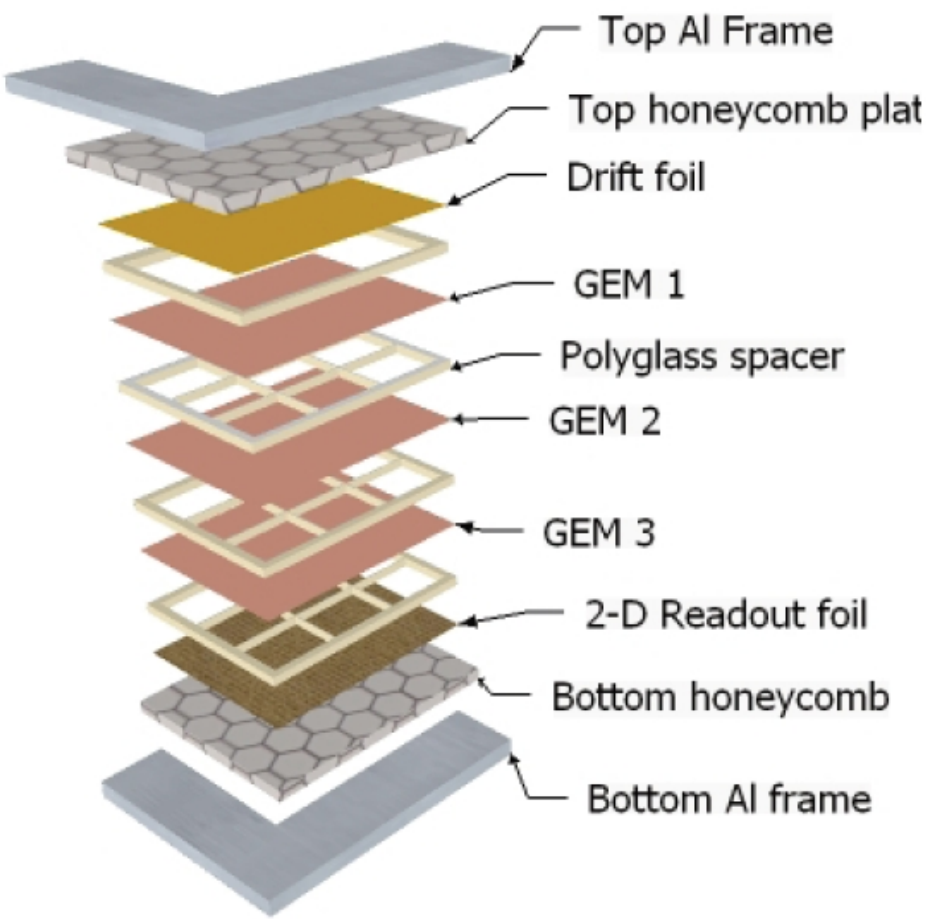
hallaweb.jlab.org/12GeV/SuperBigBite/

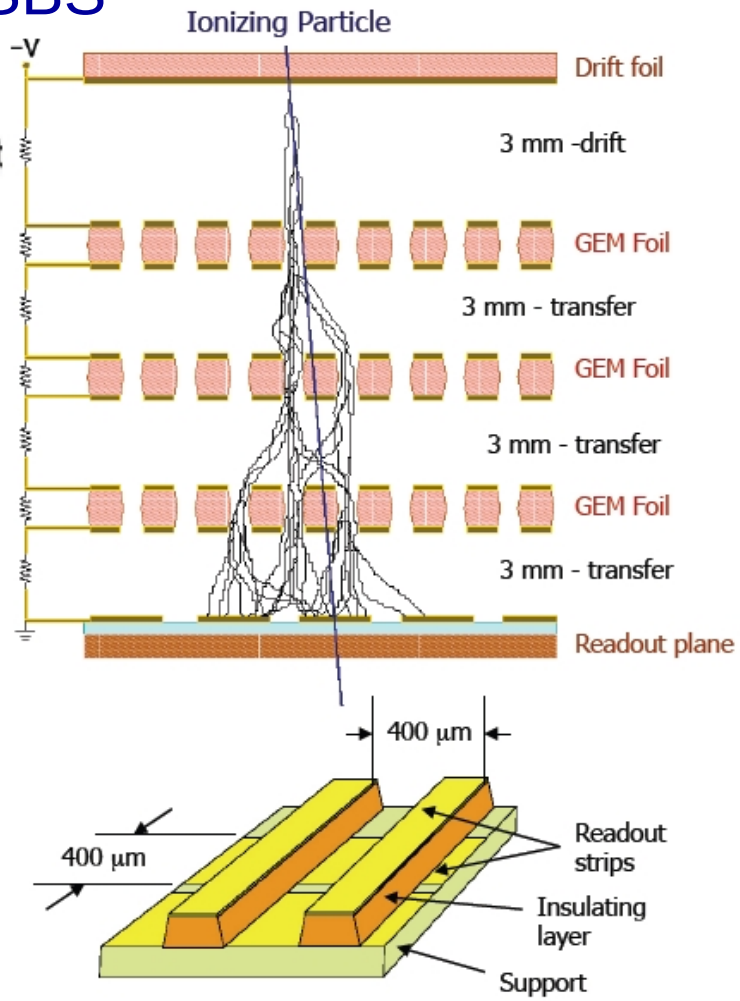
Two tracker geometries:

1. front tracker
2. second and third tracker

will use the same “base unit”

GEM for SBS

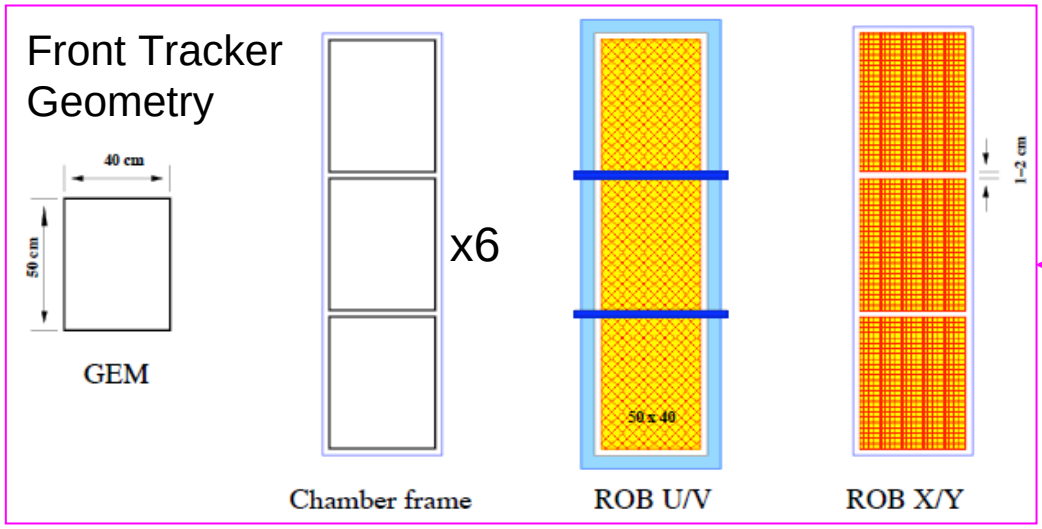


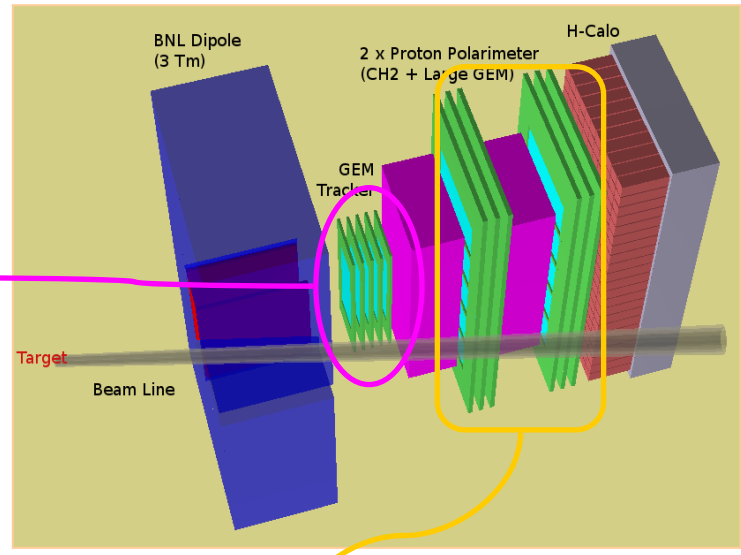


- **Standard 3 GEM foils**
- **2D Readout plane, 0.4 mm pitch**
- **Approx. 50000 channels**
- **40x150 cm² chambers made by 40x50 cm² adjacent modules**

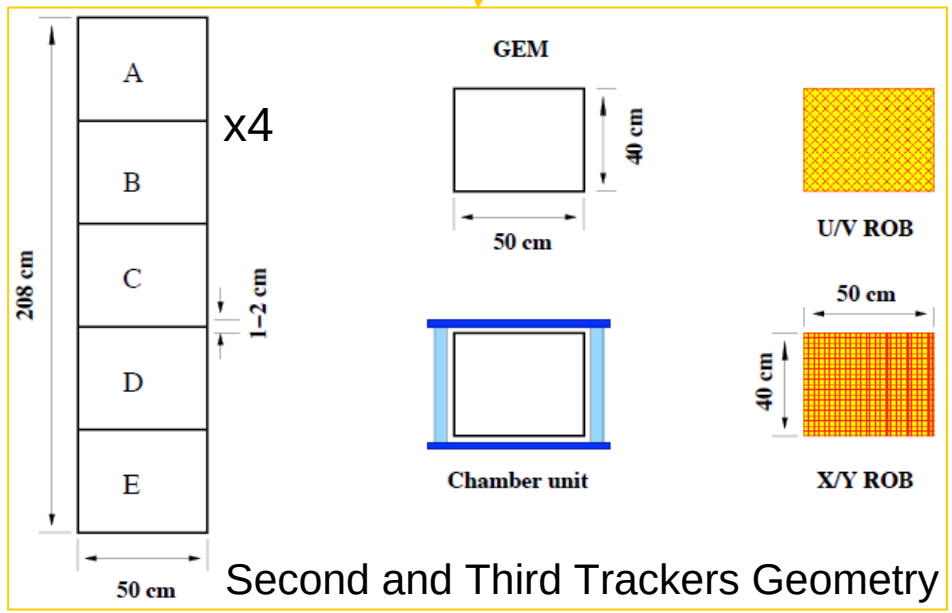
- **Minimize frames (8 mm width)**
- **Minimize front-end electronics size**
- **Minimize cabling**
- **Optimize HV distribution**

GEM Tracker Chamber Geometries

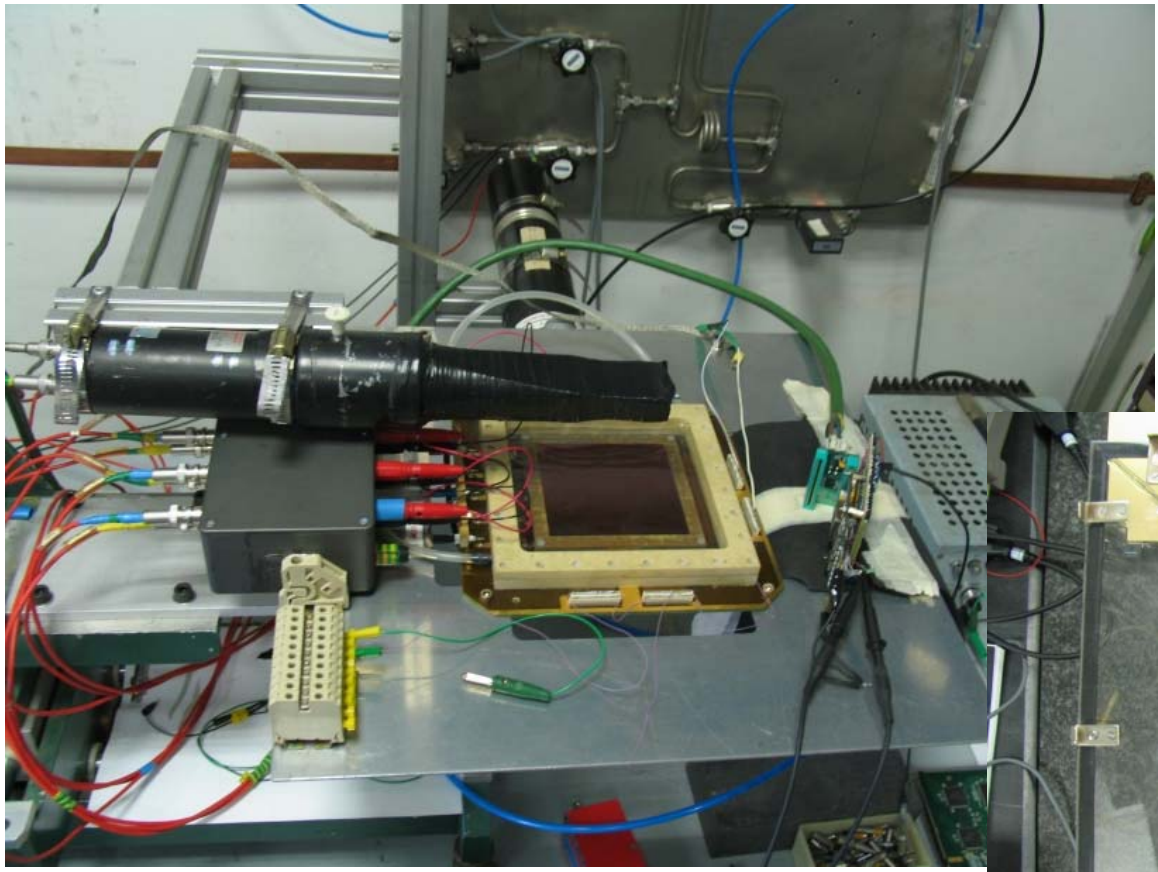




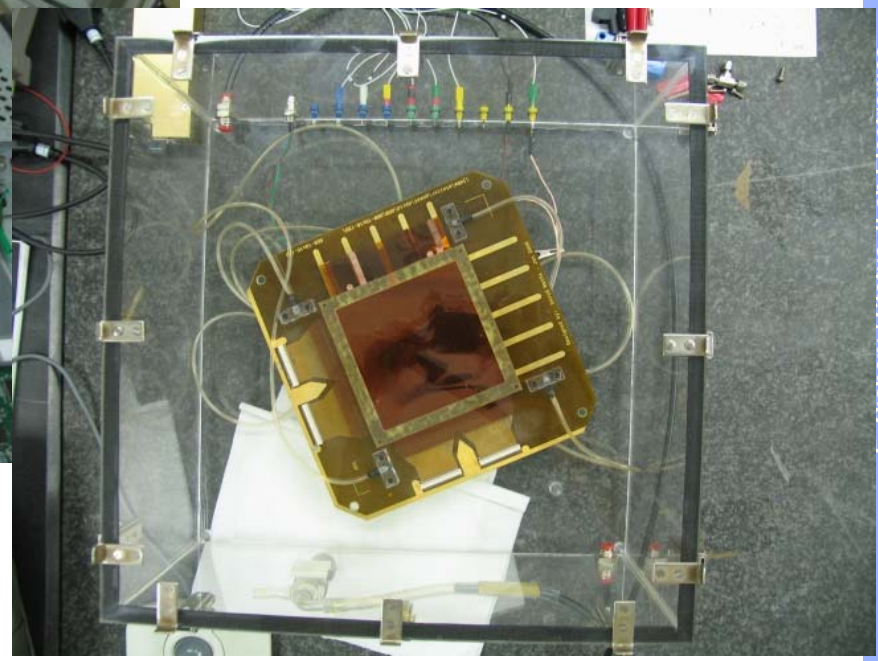
1. Single Module: 40x50 cm^2
2. Chamber combination of 3 or 5 adjacent modules
3. Both x/y and u/v 2D (a la COMPASS) readout strips
4. Electronics on the side (cyan) or beyond the dead areas (blue) at 90° degree



GEM: Prototype 0 and 1



- First 10x10 prototypes under cosmic test
- Using 70/30 Ar/CO_2 gas mixture
- 7 Independent HV levels up to ~ 5000 V



Assembling the GEM chambers parts require a careful quality control at several check points and specific tools for gluing, heating, testing, cleaning

Final 40x50 cm^2 module finalized; GEM foils ordered @ CERN

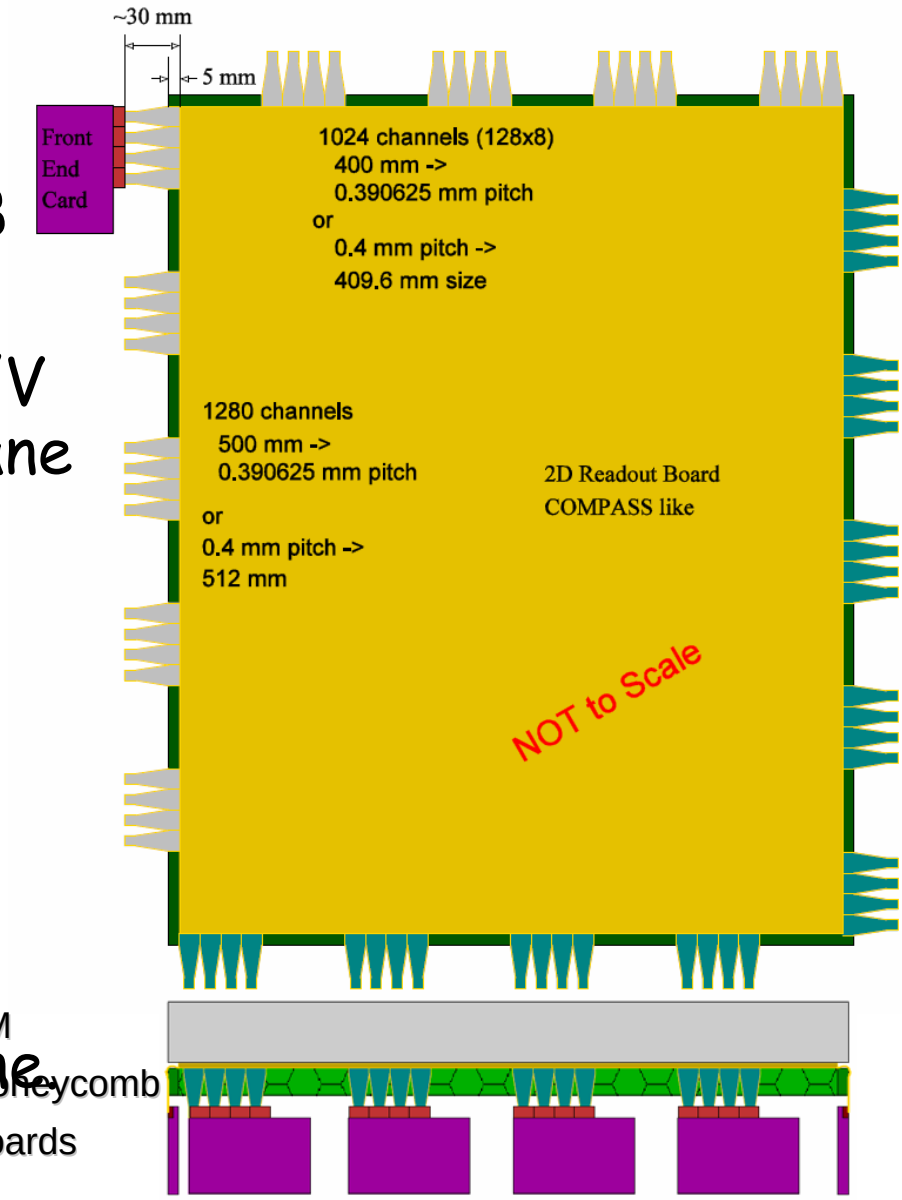
The Detector

2D readout strips layers:
pitch = 0.4 mm, multiple of 128

1024 + 1280 =2304 strips per module X/Y, little more for U/V module. 3 modules for each plane for GEM front tracker.

In total about 50000 channels for GEM front tracker. About 25000 more for GEM polarimeter tracker.

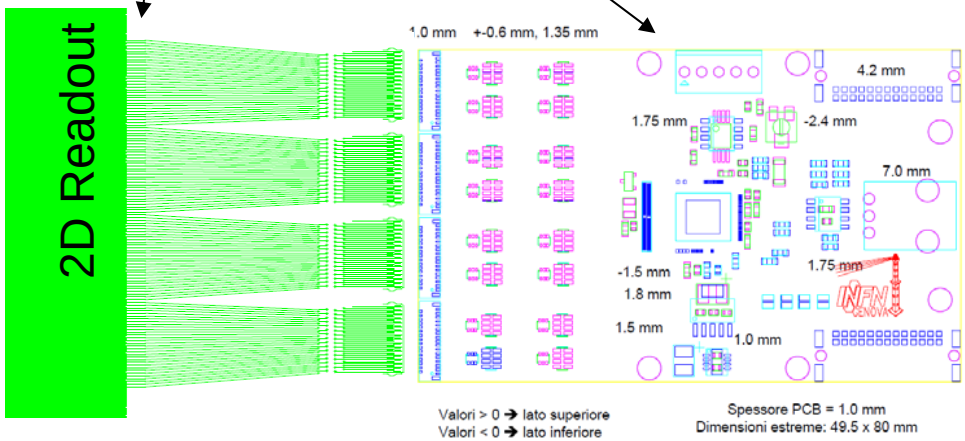
Use of Panasonic FPC connectors, 0.3 mm pitch, avoid soldering on readout plane

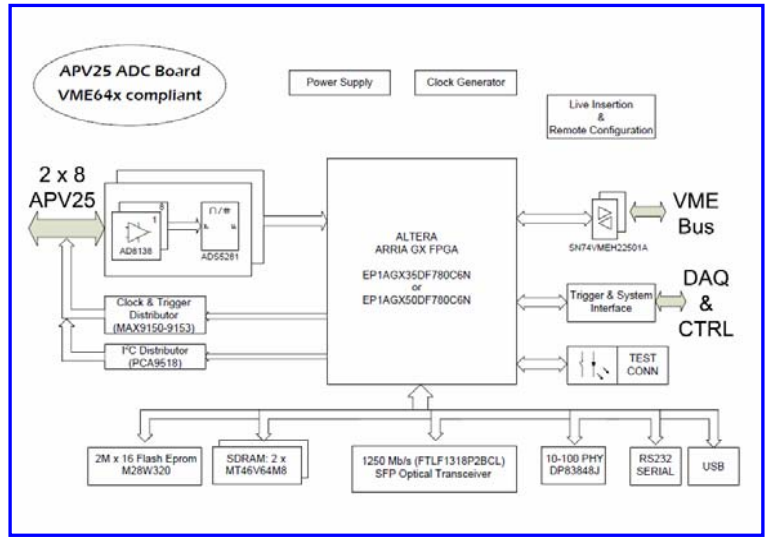


Readout on both sides

Electronics Components

GEM ⇒ **FEC** ⇒ **ADC+VME Controller** ⇒ DAQ





General Criteria:

- Minimize development time
- Minimize material of FECs (which are partially along the particle path)
- Be compliant to JLab DAQ
- Maximize flexibilty (at least during prototyping)

Thanks to Michael Böhmer and Igor Konorov

Electronics Components

Front-End Card

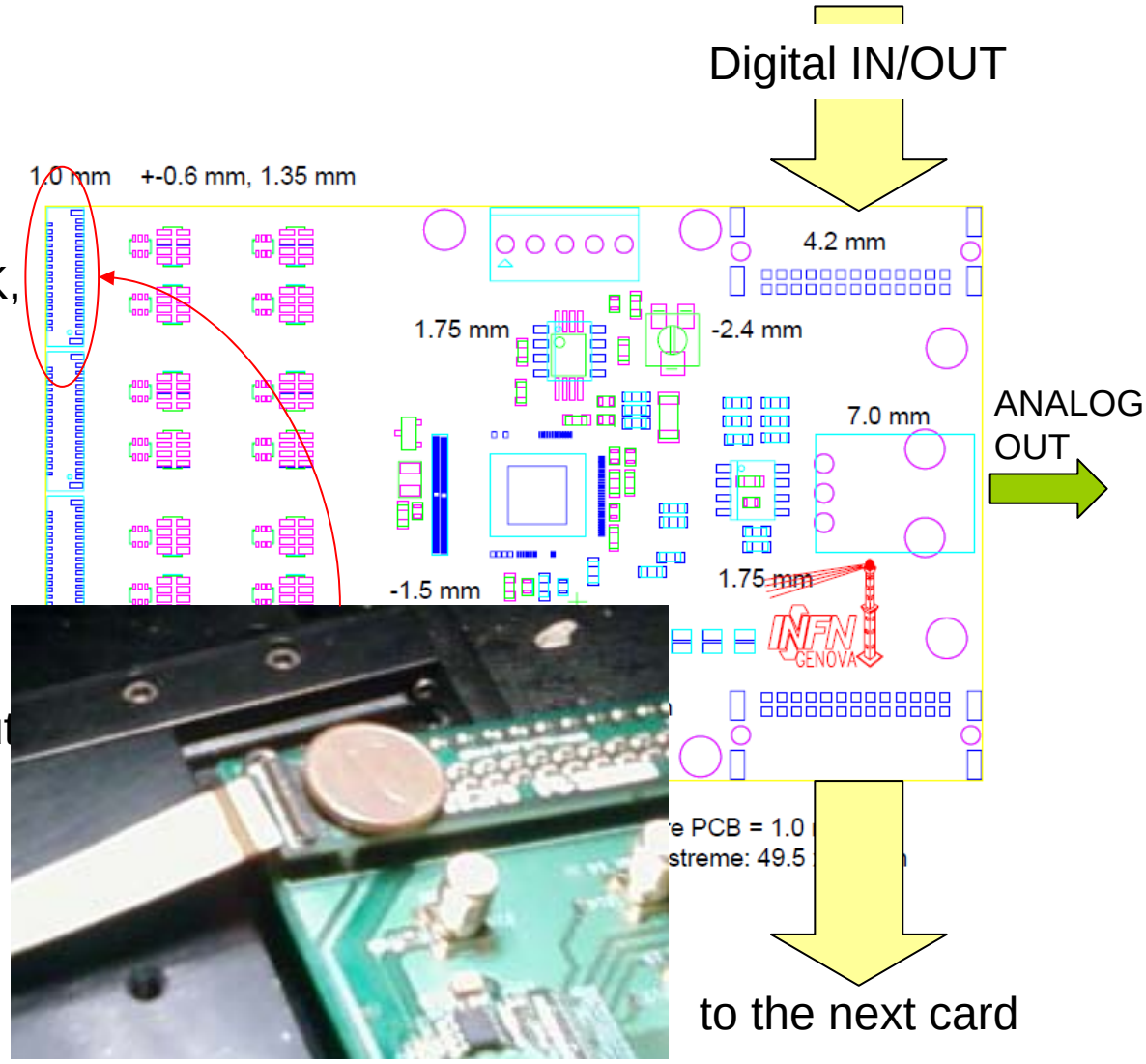
Front End card based on The APV25 chip (originally developed for SiD in CMS)

Bus like digital lines (CLOCK, trigger and I2C) & Low Voltages

Single differential line for the ANALOG out

ZIF connectors on the GEM side (no soldering on readout foil)

First front-end prototypes available beginning of December 09 ??

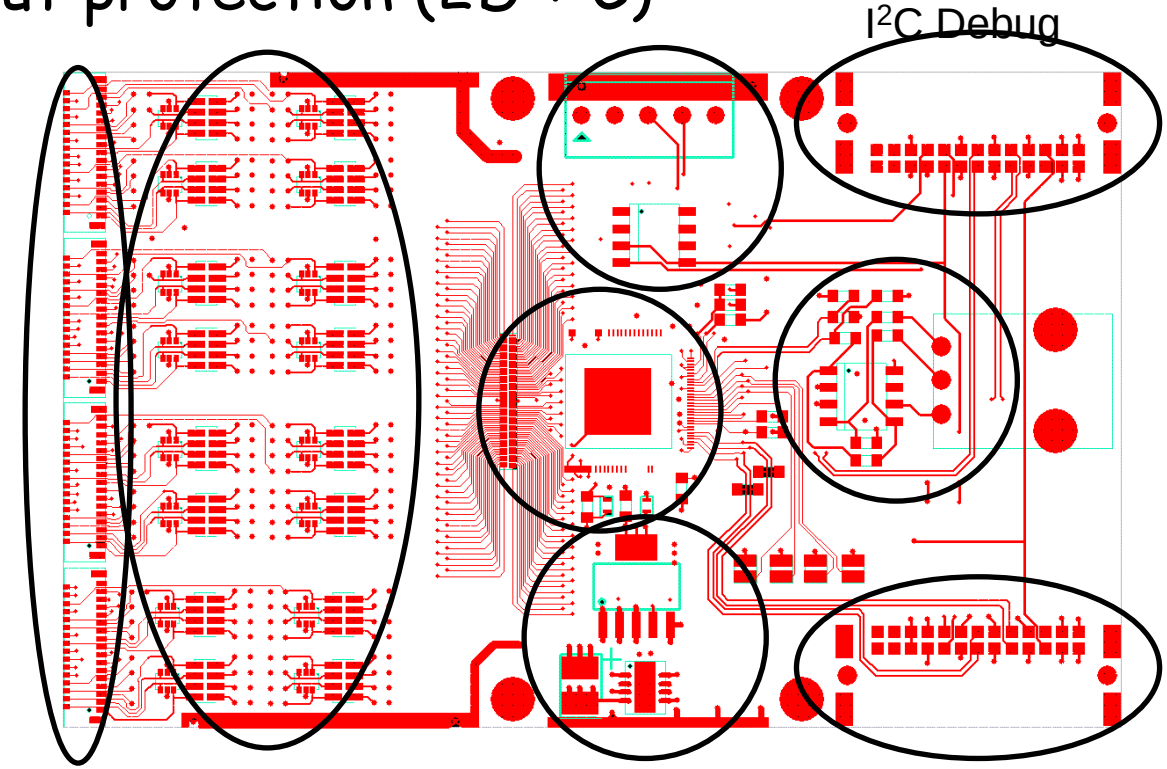


Front End (2)

Based on APV25 chip. We bought ≈ 600 naked chips.

128 channels per card (1 APV). Dimensions: 50 x 90 mm^2

Discrete input protection (2D + C)



Front End (3)

Prototype cards in production (waiting for Panasonic connectors)

Some issues regarding output analog signal transmission and radiation tolerance (quite hot zone). Testing needed.

Double check with GEM readout plane needed.

SMD assembly using external fab.

APV wire bonding using internal facility (ATLAS pixel modules).

Standard assembly (through hole) in house, after wire bonding.

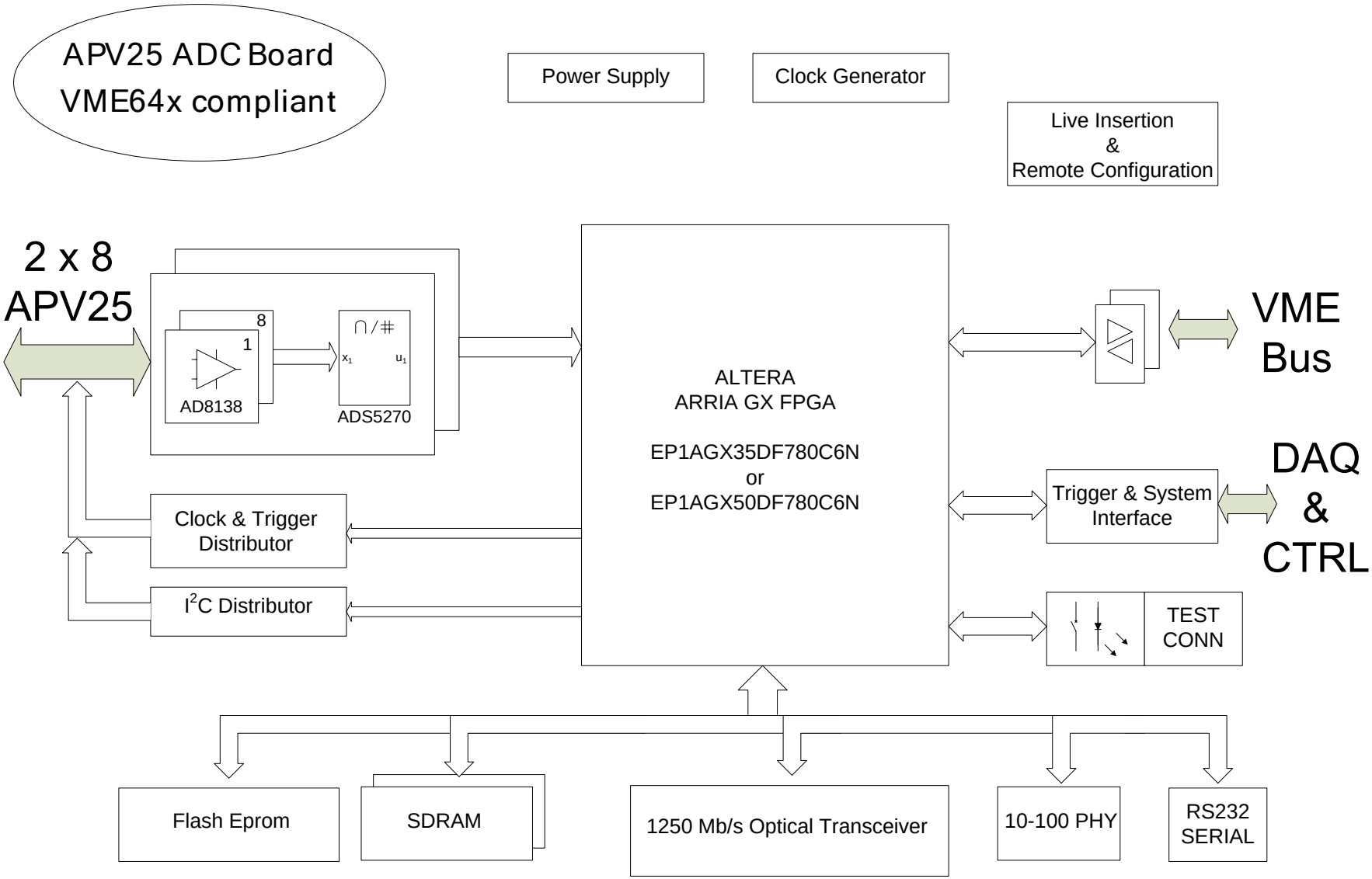
First prototype ready soon.

Readout VME module(1)

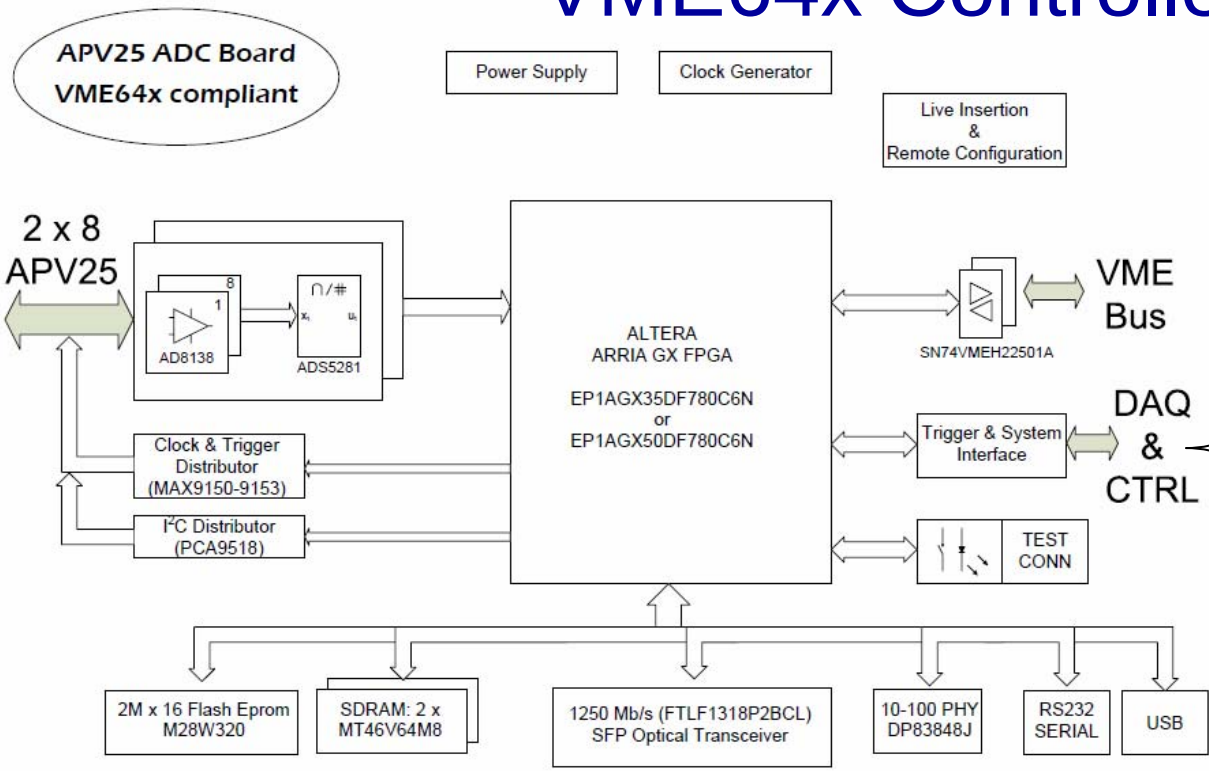
Main features:

- Digitization of 16 APVs (2048 channels)
- APV serial stream decoding
- Zero suppression
- Big memory buffer, multi event
- Possibility to implement SOC:
  - Flash, Ethernet, Serial
- Remote logic reconfiguration, hot swappable
- Dual configuration:
  - goal: VME64x compliant
  - backup: Stand Alone (with optical link)

Readout VME module(2)



VME64x Controller



From the VXS backplane:

1. Trigger L1/L2
2. Synch
3. Clock
4. Busy (OUT)

(duplicated on front panel)

- VME controller hosts the digitization of the analog signals coming from the front-end card.
- It handle all control signals required by the front end card
- Compliant to the new JLab/12 VME64x VITA 41 (VXS) standard
- We intend to make it accessible by standard VME as well (with reduced functionality)
- Design with the possibility to detach the ADC subcomponent to extend FEC-VME64x distance (expected to be ~7 m)

Readout VME module (3)

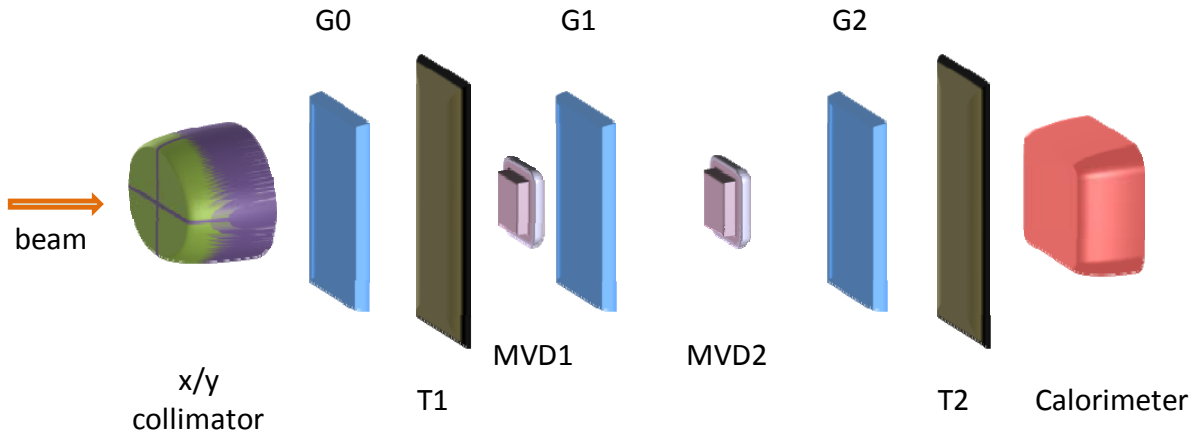
Status:

- Almost all components chosen
  - FPGA: Altera Arria GX
  - ADC: Texas ADS5270
- Schematic drawing done
- PCB design well advanced
  - Footprint checking in progress
- Quotation for manufacturing already asked
  - Ready for production by beginning of next year
  - Available February/March 2010

Development of FPGA code well underway:

- APV deserialization and decoding
- VME interface
- I^2C controller
- Trigger handling
- High speed serial interface (optical)

Start beam test next week and continuig next year as soon as test beam availability at DESY is resumed (February 22nd).



- Tests in a hard radiation environment -> CERN or JLab ?
- Front end prototypes testing will teach a lot regarding output analog signal integrity and radiation tolerance.
- All should be tested by summer next year.